TEXAS INSTRUMENTS

CSD75208W1015

SLPS512 – JULY 2014

CSD75208W1015 Dual 20-V Common Source P-Channel NexFET™ Power MOSFET

1 Features

- Dual P-Channel MOSFETs
- Common Source Configuration
- Small Footprint 1 mm × 1.5 mm
- Gate-Source Voltage Clamp
- Gate ESD Protection –3 kV
- Pb Free
- RoHS Compliant
- Halogen Free

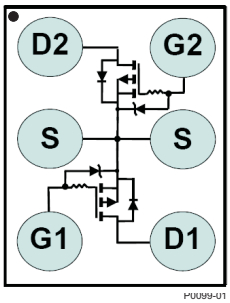
2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This device is designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on-resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	1.9		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.23		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	100	mΩ
		V_{GS} = –2.5 V	70	mΩ
		V_{GS} = –4.5 V	56	mΩ
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	V_{GS} = –1.8 V	190	mΩ
		V_{GS} = –2.5 V	120	mΩ
		V_{GS} = –4.5 V	90	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.8		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD75208W1015	3000	7-Inch Reel	1.0 mm × 1.5 mm Wafer Level Package	Tape and Reel
CSD75208W1015T	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

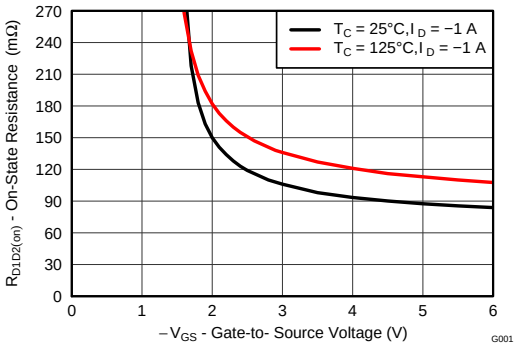
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–6	V
I_{D1D2}	Continuous Drain-to-Drain Current, T_C = 25°C	–1.6	A
	Pulsed Drain-to-Drain Current, T_C = 25°C(1)	–22	A
I_S	Continuous Source Pin Current	–3	A
	Pulsed Source Pin Current(1) (2)	–39	A
I_G	Continuous Gate Clamp Current	–0.5	A
	Pulsed Gate Clamp Current(1)	–7	A
P_D	Power Dissipation	0.75	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

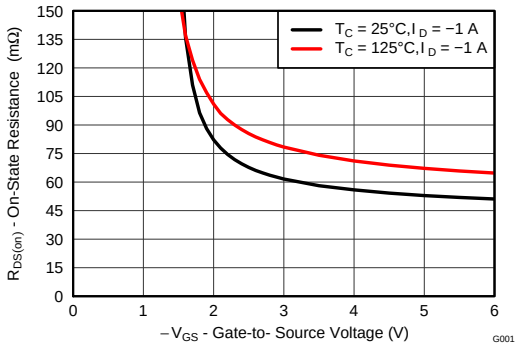
(1) Max $R_{\theta JA}$ = 165°C/W, pulse duration ≤100 µs, duty cycle ≤1%

(2) Both devices in parallel

$R_{D1D2(on)}$ vs V_{GS}



$R_{DS(on)}$ vs V_{GS}



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4 Revision History

DATE	REVISION	NOTES
July 2014	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

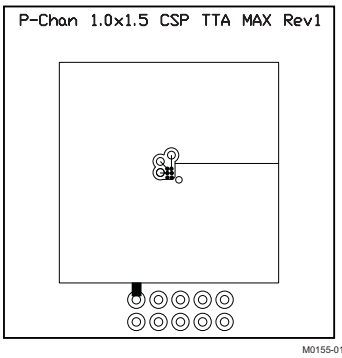
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
BV_{GSS}	Gate-to-Source Voltage	V_{DS} = 0 V, I_G = –250 µA	–6.1		–7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.5	–0.8	–1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_D = –1 A		100	150	mΩ
		V_{GS} = –2.5 V, I_D = –1 A		70	88	mΩ
		V_{GS} = –4.5 V, I_D = –1 A		56	68	mΩ
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	V_{GS} = –1.8 V, I_{D1D2} = –1 A		190	285	mΩ
		V_{GS} = –2.5 V, I_{D1D2} = –1 A		120	150	mΩ
		V_{GS} = –4.5 V, I_{D1D2} = –1 A		90	108	mΩ
g_{fs}	Transconductance	V_{DS} = –2 V, I_D = –1 A		7.5		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		315	410	pF
C_{OSS}	Output Capacitance			132	172	pF
C_{RSS}	Reverse Transfer Capacitance			7.7	10	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –1 A		1.9	2.5	nC
Q_{gd}	Gate Charge, Gate-to-Drain			0.23		nC
Q_{gs}	Gate Charge, Gate-to-Source			0.48		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.31		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		2.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –1 A, R_G = 0 Ω		9		ns
t_r	Rise Time			5		ns
$t_{d(off)}$	Turn Off Delay Time			29		ns
t_f	Fall Time			11		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = –1 A, V_{GS} = 0 V		–0.75	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = –10 V, I_F = –1 A, di/dt = 200 A/µs		4.3		nC
t_{rr}	Reverse Recovery Time			9		ns

5.2 Thermal Information

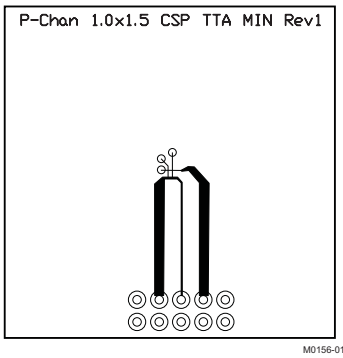
T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1) (2)		165		°C/W
	Junction-to-Ambient Thermal Resistance (2) (3)		95		

(1) Device mounted on FR4 material with minimum Cu mounting area
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Typ $R_{\theta JA}$ = 95°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Typ $R_{\theta JA}$ = 165°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

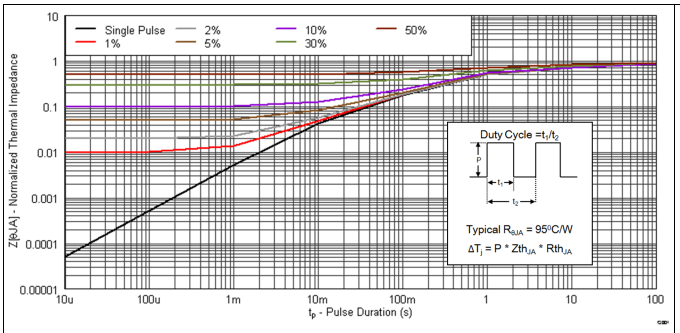


Figure 1. Transient Thermal Impedance

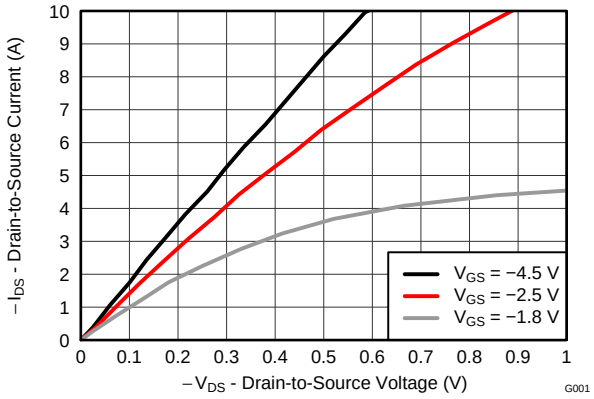


Figure 2. Saturation Characteristics

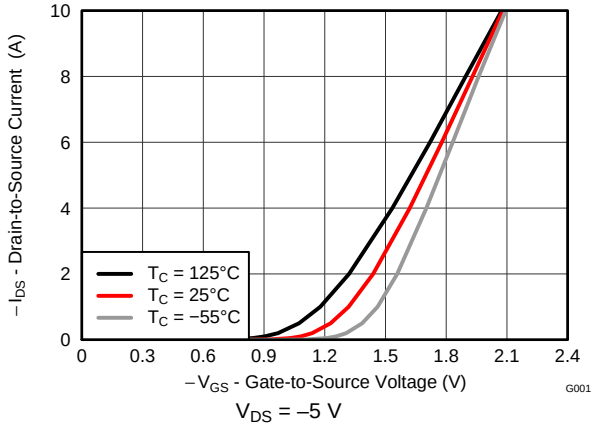


Figure 3. Transfer Characteristics

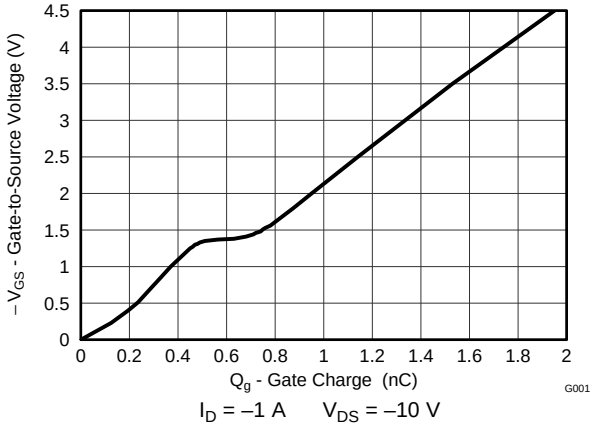


Figure 4. Gate Charge

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

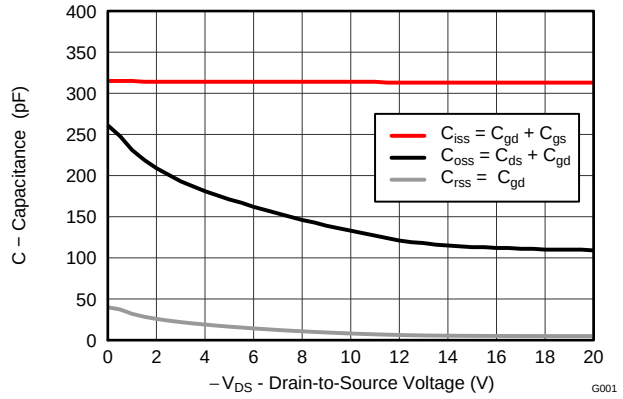


Figure 5. Capacitance

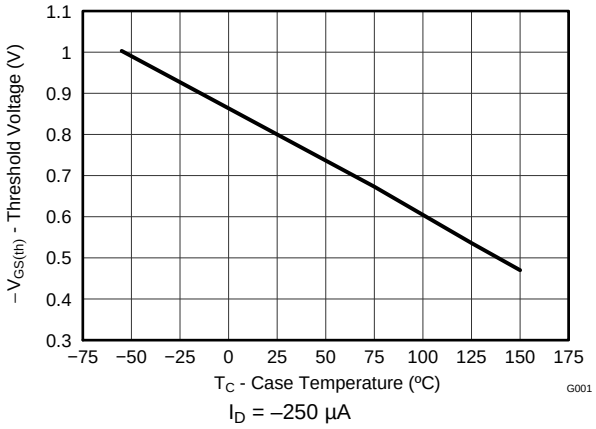


Figure 6. Threshold Voltage vs Temperature

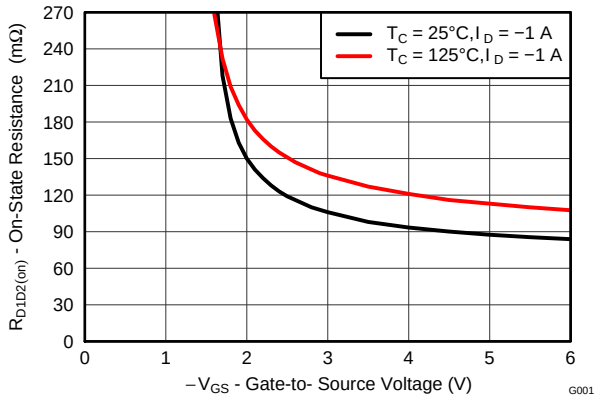


Figure 7. On-State Drain-to-Drain Resistance vs Gate-to-Source Voltage

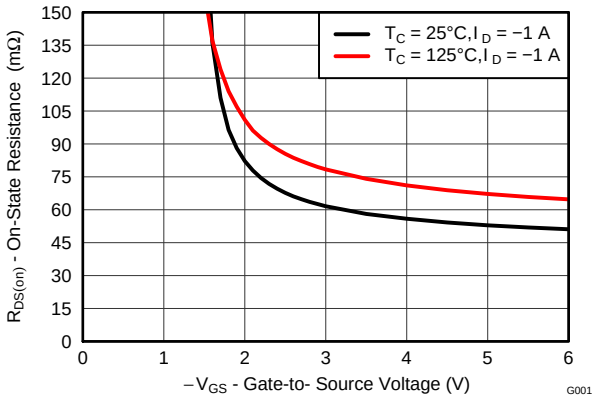


Figure 8. On-State Drain-to-Source Resistance vs Gate-to-Source Voltage

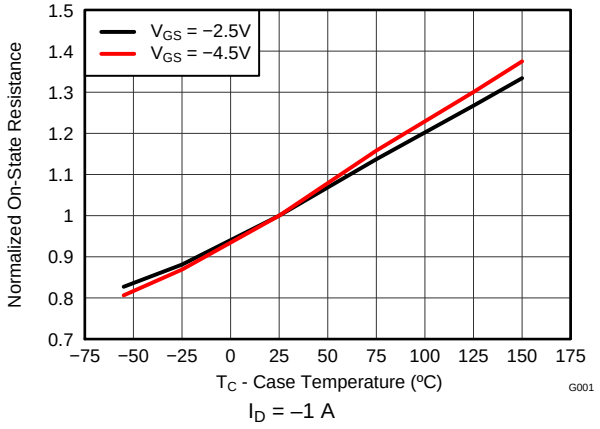


Figure 9. Normalized On-State Resistance vs Temperature

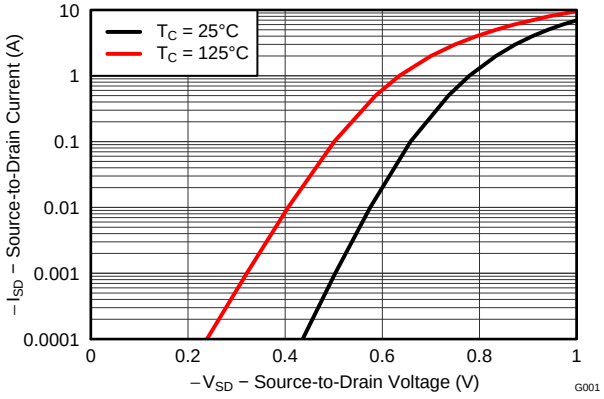


Figure 10. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

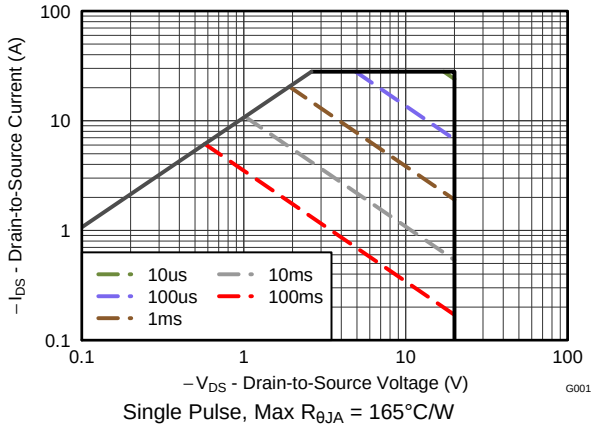


Figure 11. Maximum Safe Operating Area

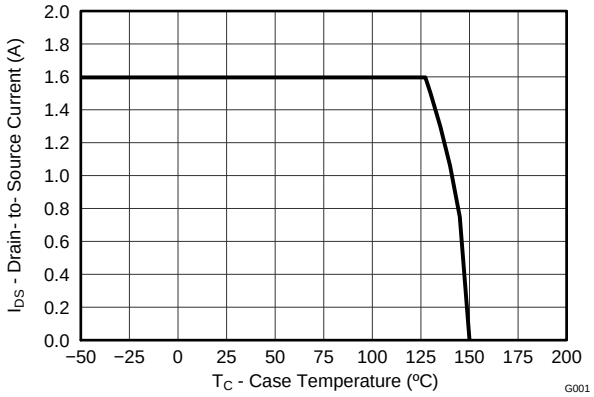


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

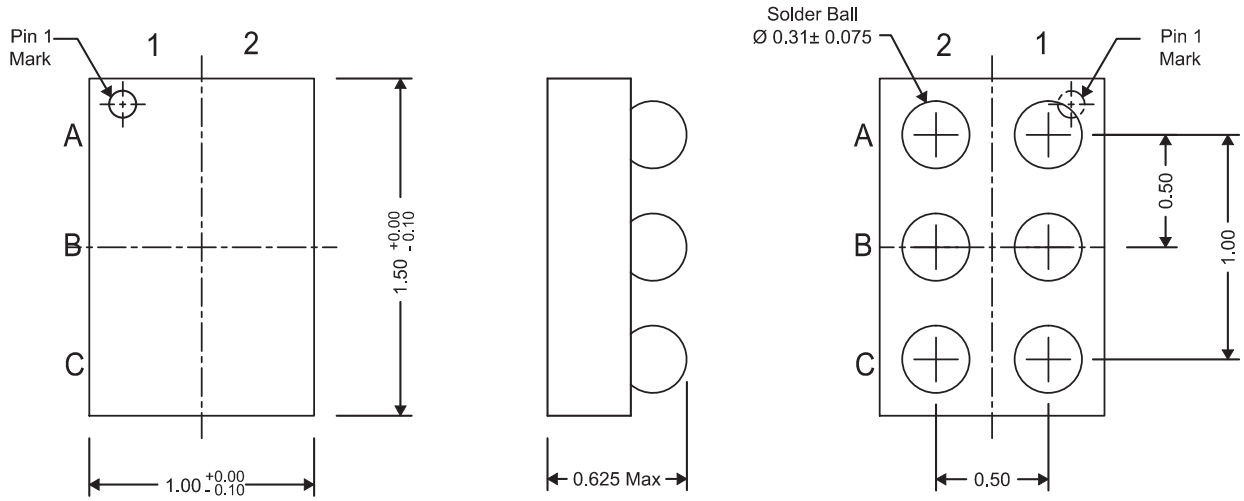
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

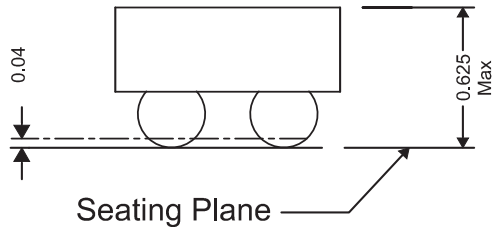
7.1 CSD75208W1015 Package Dimensions



Top View

Side View

Bottom View



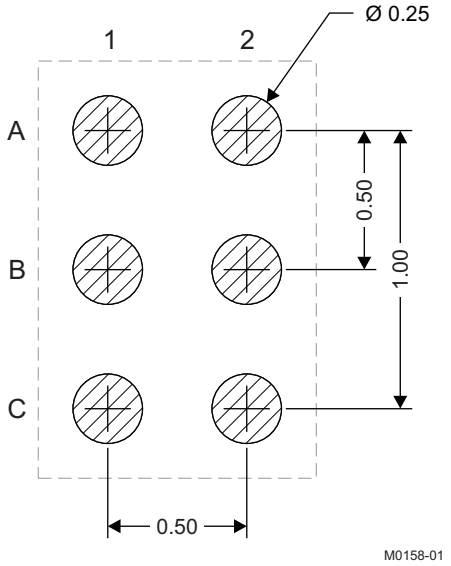
Front View

NOTE: All dimensions are in mm (unless otherwise specified).

Pinout

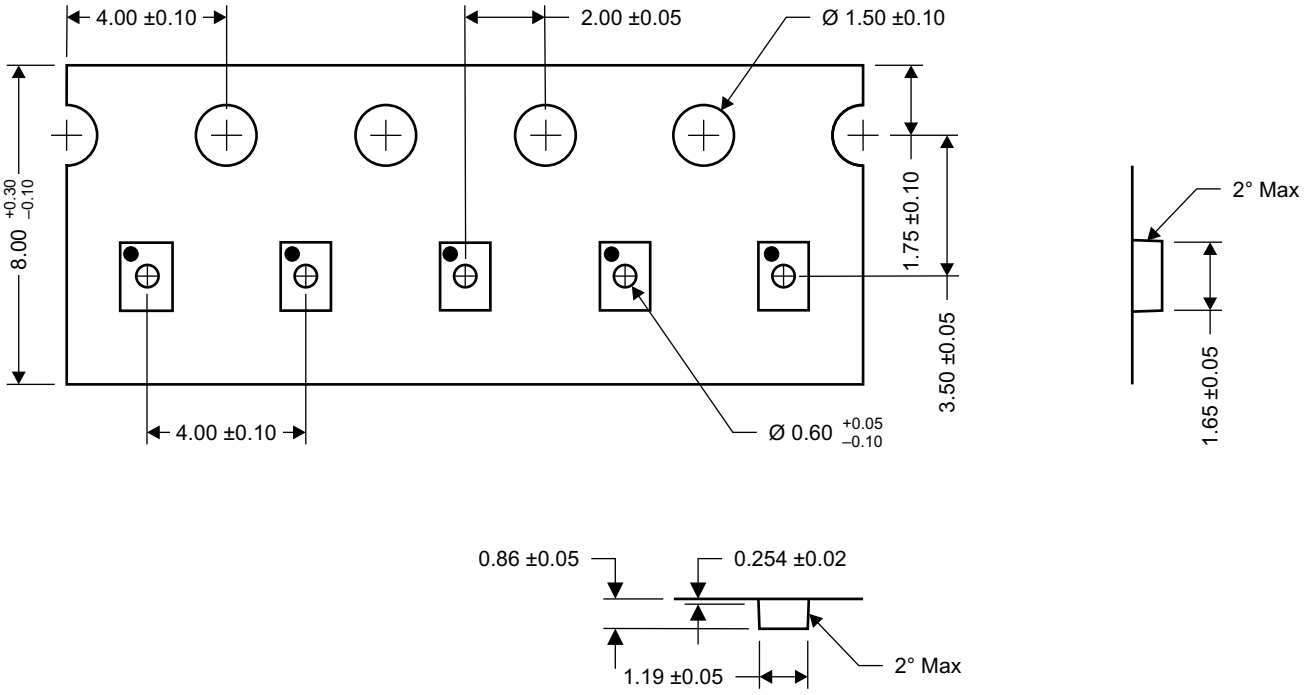
POSITION	DESIGNATION
B1, B2	Source
C1	Gate1
C2	Drain1
A2	Gate2
A1	Drain2

7.2 Recommended PCB Land Pattern



NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD75208W1015	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	75208	Samples
CSD75208W1015T	ACTIVE	DSBGA	YZC	6	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	75208	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

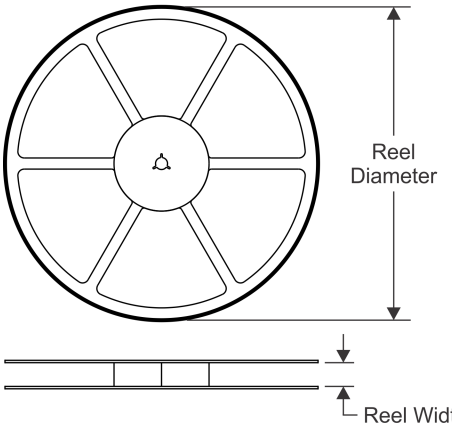
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

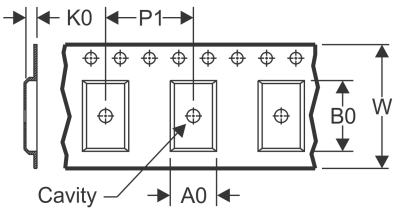
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

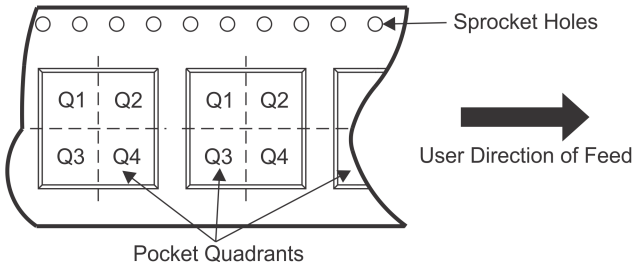


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

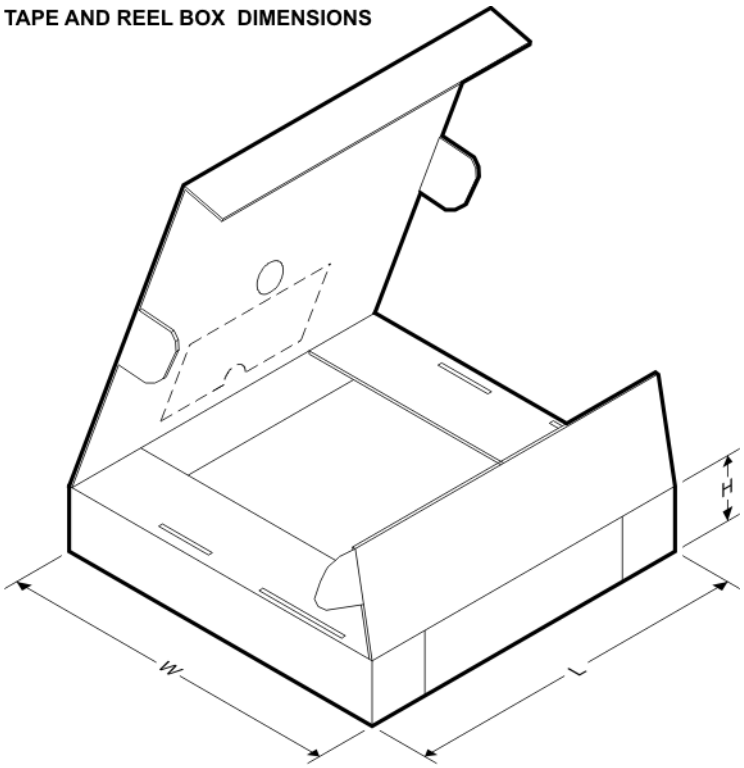
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD75208W1015	DSBGA	YZC	6	3000	180.0	9.0	1.18	1.68	0.83	4.0	8.0	Q1
CSD75208W1015T	DSBGA	YZC	6	250	180.0	9.0	1.18	1.68	0.83	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD75208W1015	DSBGA	YZC	6	3000	195.0	210.0	39.0
CSD75208W1015T	DSBGA	YZC	6	250	195.0	210.0	39.0

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