



1% Accurate, Low-Voltage, Quad Window Voltage Detector

MAX16063

General Description

The MAX16063 is a 1% accurate, adjustable, quad window voltage detector in a small thin QFN package. This device is designed to provide a higher level of system reliability by monitoring multiple supply voltages and providing a fault signal when any of the voltages exceed their overvoltage thresholds or fall below their undervoltage thresholds.

The MAX16063 offers user-adjustable voltage thresholds that allow voltages to be monitored down to 0.4V. This allows the upper and lower trip thresholds of each window detector to be set externally with the use of three external resistors.

Each monitored threshold has an independent open-drain output for signaling a fault condition. The outputs can be wire-ORed together to provide a single fault output. The open-drain outputs are internally pulled up with a 30μA current, but can be externally driven to other voltage levels for interfacing to other logic levels.

Features include a margin input to disable the outputs during margin testing or any other time after power-up operations. Also featured is a reset output that deasserts after a reset timeout period after all voltages are within their threshold specifications. The reset timeout is internally set to 140ms (min), but can be externally adjusted to other reset timeouts using an external capacitor. In addition, the MAX16063 offers a manual reset input.

This device is offered in a 4mm x 4mm thin QFN package and is fully specified from -40°C to +125°C.

Applications

Storage Equipment
Networking/Telecommunications Equipment
Multivoltage ASICs
Servers
Automotive

Pin Configuration appears at end of data sheet.

Features

- ◆ Monitor Four Undervoltage/Overvoltage Conditions
- ◆ 1% Accuracy Over Temperature
- ◆ User-Adjustable Voltage Thresholds (Down to 0.4V)
- ◆ Open-Drain Outputs with Internal Pullups Reduce the Number of External Components
- ◆ Manual Reset Input
- ◆ Margin Enable Input
- ◆ Fixed or Adjustable RESET Timeout
- ◆ Guaranteed to Remain Asserted Down to $V_{CC} = 1V$
- ◆ Fully Specified from -40°C to +125°C
- ◆ Small, 4mm x 4mm Thin QFN Package

Ordering Information

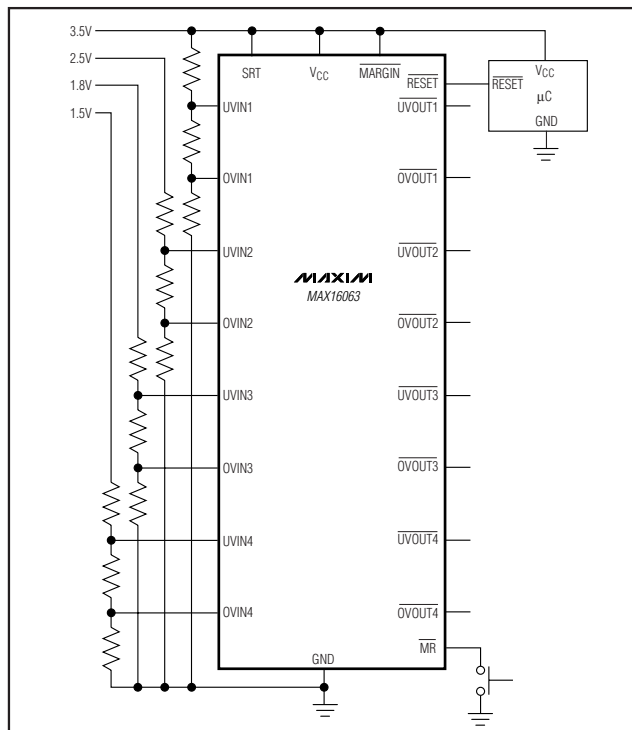
PART	TEMP RANGE	PIN-PACKAGE
MAX16063TG+	-40°C to +125°C	24 TQFN-EP*

+ Denotes a lead-free package.

*EP = Exposed pad.

For tape-and-reel, add a "T" after the "+." Tape-and-reel are offered in 2.5k increments.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

V_{CC} , $\overline{OVOUT_}$, $\overline{UVOUT_}$, $\overline{RESET}$,
 $\overline{UVIN_}$, $\overline{OVIN_}$ to GND-0.3V to +6V
 $\overline{MARGIN}$, $\overline{MR}$, SRT to GND-0.3V to (V_{CC} + 0.3V)
 Input/Output Current
 ($\overline{RESET}$, $\overline{MARGIN}$, SRT, $\overline{MR}$, $\overline{UVOUT_}$, $\overline{OVOUT_}$)±20mA

Continuous Power Dissipation (T_A = +70°C)
 24-Pin Thin QFN (derate 16.9mW/°C above +70°C)1666mW
 Operating Temperature Range-40°C to +125°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	(Note 2)	1.0		5.5	V
Supply Current (Note 3)	I_{CC}	V_{CC} = 3.3V, outputs deasserted		45	65	μA
		V_{CC} = 5V, outputs deasserted		50	70	
UVLO (Undervoltage Lockout)	V_{UVLO}	V_{CC} rising	1.62	1.80	1.98	V
UVLO Hysteresis	V_{UVLO_HYS}			65		mV
UVIN_/OVIN_						
Adjustable Threshold ($\overline{UVIN_}$ Falling/ $\overline{OVIN_}$ Rising)	V_{TH}		0.390	0.394	0.398	V
$\overline{UVIN_}/\overline{OVIN_}$ Hysteresis	V_{TH_HYS}	$\overline{UVIN_}$ falling/ $\overline{OVIN_}$ rising (percentage of the threshold)		0.5		% V_{TH}
$\overline{UVIN_}/\overline{OVIN_}$ Input Current	I_{IB}		-100		+100	nA
RESET						
Reset Timeout	t_{RP}	SRT = V_{CC}	140	200	280	ms
		CSRT = 1500pF (Note 4)	2.43	3.09	3.92	
		CSRT = 100pF		0.206		
		CSRT = open		0.05		
SRT Ramp Current	I_{SRT}	V_{SRT} = 0V	460	600	740	nA
SRT Threshold			1.173	1.235	1.293	V
SRT Hysteresis				100		mV
$\overline{UVIN_}/\overline{OVIN_}$ to Reset Delay	t_{RD}	$\overline{UVIN_}$ falling/ $\overline{OVIN_}$ rising		20		μs

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 2.0V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise specified. Typical values are at $V_{CC} = 3.3V$, $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$ Output-Voltage Low	V_{OL}	$V_{CC} = 3.3V$, $I_{SINK} = 10mA$, $\overline{RESET}$ asserted			0.3	V
		$V_{CC} = 2.5V$, $I_{SINK} = 6mA$, $\overline{RESET}$ asserted			0.3	
		$V_{CC} = 1.2V$, $I_{SINK} = 50\mu A$, $\overline{RESET}$ asserted			0.3	
$\overline{RESET}$ Output-Voltage High	V_{OH}	$V_{CC} \geq 2.0V$, $I_{SOURCE} = 6\mu A$, $\overline{RESET}$ deasserted	$0.8 \times V_{CC}$			V
$\overline{MR}$ Input-Voltage Low	V_{IL}				$0.3 \times V_{CC}$	V
$\overline{MR}$ Input-Voltage High	V_{IH}		$0.7 \times V_{CC}$			V
$\overline{MR}$ Minimum Pulse Width			1			μs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to $\overline{RESET}$ Delay				200		ns
$\overline{MR}$ Pullup Resistance			12	20	28	$k\Omega$
OUTPUTS ($\overline{UVOUT}$/$\overline{OVOUT}$)						
$\overline{UVOUT}$, $\overline{OVOUT}$ Output-Voltage Low	V_{OL}	$V_{CC} = 3.3V$, $I_{SINK} = 2mA$			0.3	V
		$V_{CC} = 2.5V$, $I_{SINK} = 1.2mA$			0.3	
$\overline{UVOUT}$, $\overline{OVOUT}$ Output-Voltage High	V_{OH}	$V_{CC} \geq 2.0V$, $I_{SOURCE} = 6\mu A$	$0.8 \times V_{CC}$			V
$\overline{UVIN}$ / $\overline{OVIN}$ to $\overline{UVOUT}$ / $\overline{OVOUT}$ Propagation Delay	t_D	($V_{TH} - 100mV$) to ($V_{TH} + 100mV$)		20		μs
DIGITAL LOGIC						
$\overline{MARGIN}$ Input-Voltage Low	V_{IL}				$0.3 \times V_{CC}$	V
$\overline{MARGIN}$ Input-Voltage High	V_{IH}		$0.7 \times V_{CC}$			V
$\overline{MARGIN}$ Pullup Resistance		Pulled up to V_{CC}	12	20	28	$k\Omega$
$\overline{MARGIN}$ Delay Time	t_{MD}	Rising or falling (Note 5)		50		μs

Note 1: Devices are tested at $T_A = +25^{\circ}C$ and guaranteed by design for $T_A = T_{MIN}$ to T_{MAX} .

Note 2: The outputs are guaranteed to remain asserted down to $V_{CC} = 1V$.

Note 3: Measured with $\overline{MR}$ and $\overline{MARGIN}$ unconnected.

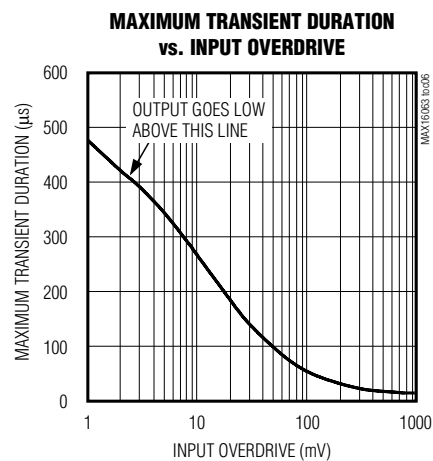
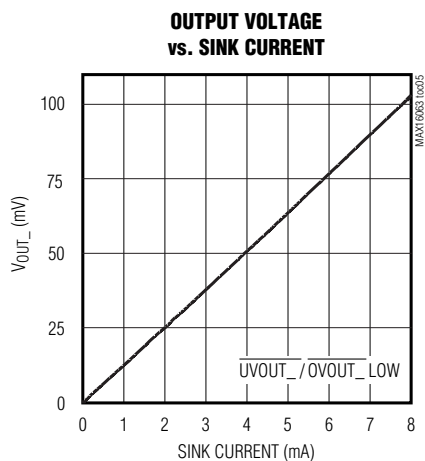
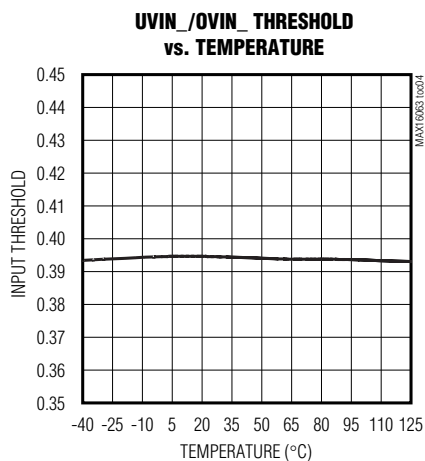
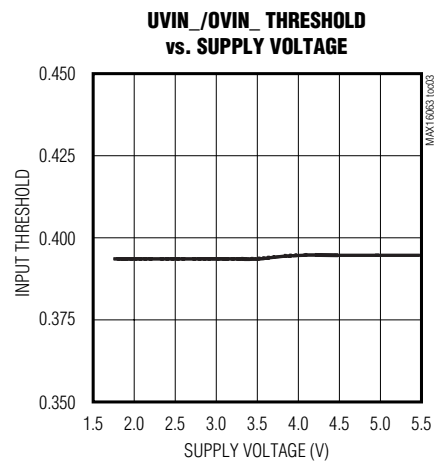
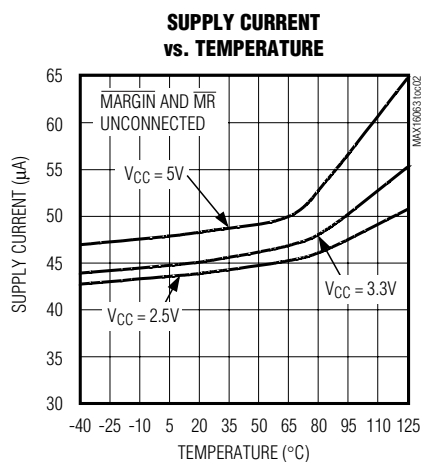
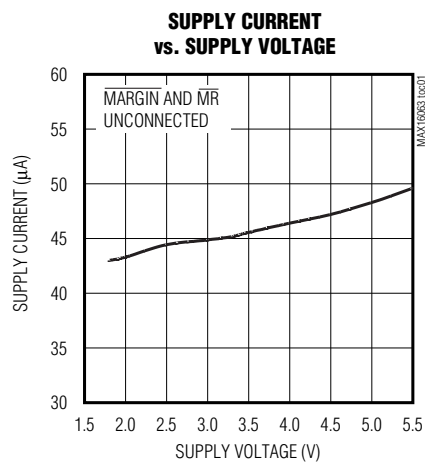
Note 4: The minimum and maximum specifications for this parameter are guaranteed by using the worse case of the SRT current and SRT threshold specifications.

Note 5: Amount of time required for logic to lock/unlock outputs from margin testing.

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Typical Operating Characteristics

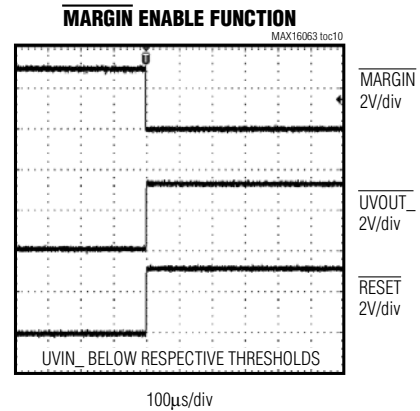
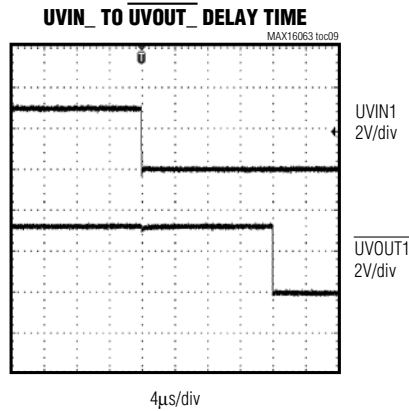
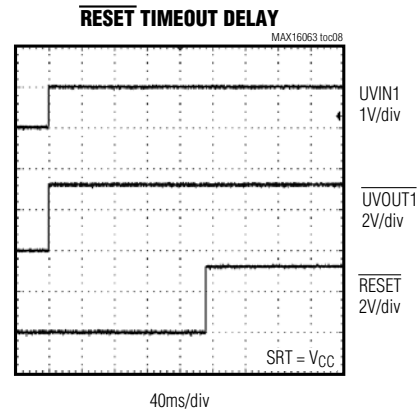
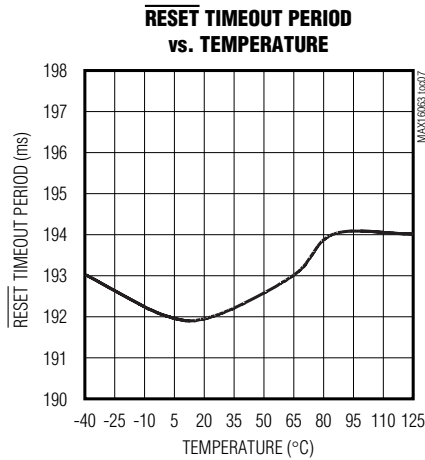
($V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_{CC} = 3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



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Pin Description

PIN	NAME	FUNCTION
1	UVIN3	Undervoltage Threshold Input 3. When the voltage on UVIN3 falls below its threshold, $\overline{\text{UVOUT3}}$ asserts low.
2	OVIN3	Overvoltage Threshold Input 3. When the voltage on OVIN3 rises above its threshold, $\overline{\text{OVOUT3}}$ asserts low.
3	UVIN4	Undervoltage Threshold Input 4. When the voltage on UVIN4 falls below its threshold, $\overline{\text{UVOUT4}}$ asserts low.
4	OVIN4	Overvoltage Threshold Input 4. When the voltage on OVIN4 rises above its threshold, $\overline{\text{OVOUT4}}$ asserts low.
5	N.C.	No Connection. Not internally connected.
6	GND	Ground
7, 24	V _{CC}	Unmonitored Power to the Device
8	$\overline{\text{UVOUT3}}$	Active-Low Undervoltage Output 3. When the voltage at UVIN3 falls below its threshold, $\overline{\text{UVOUT3}}$ asserts low and stays asserted until the voltage at UVIN3 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} .
9	$\overline{\text{OVOUT3}}$	Active-Low Overvoltage Output 3. When the voltage at OVIN3 rises above its threshold, $\overline{\text{OVOUT3}}$ asserts low and stays asserted until the voltage at OVIN3 falls below its threshold. The open-drain output has a 30μA internal pullup to V _{CC} .
10	$\overline{\text{UVOUT4}}$	Active-Low Undervoltage Output 4. When the voltage at UVIN4 falls below its threshold, $\overline{\text{UVOUT4}}$ asserts low and stays asserted until the voltage at UVIN4 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} .
11	$\overline{\text{OVOUT4}}$	Active-Low Overvoltage Output 4. When the voltage at OVIN4 rises above its threshold, $\overline{\text{OVOUT4}}$ asserts low and stays asserted until the voltage at OVIN4 falls below its threshold. The open-drain output has a 30μA internal pullup to V _{CC} .
12	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Pull $\overline{\text{MR}}$ low to assert $\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ remains low for the reset timeout period after $\overline{\text{MR}}$ is deasserted. $\overline{\text{MR}}$ is pulled up to V _{CC} through a 20kΩ resistor.
13	SRT	Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{\text{SRT}} (\text{F})$. For the internal timeout period of 140ms (min), connect SRT to V _{CC} .
14	$\overline{\text{MARGIN}}$	Active-Low Margin Enable Input. Pull $\overline{\text{MARGIN}}$ low to deassert all outputs (go into high state) regardless of the voltage at any monitored input.

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Pin Description (continued)

PIN	NAME	FUNCTION
15	$\overline{\text{OVOUT2}}$	Active-Low Overvoltage Output 2. When the voltage at OVIN2 rises above its threshold, $\overline{\text{OVOUT2}}$ asserts low and stays asserted until the voltage at OVIN2 falls below its threshold. The open-drain output has a 30 μ A internal pullup to V _{CC} .
16	$\overline{\text{UVOUT2}}$	Active-Low Undervoltage Output 2. When the voltage at UVIN2 falls below its threshold, $\overline{\text{UVOUT2}}$ asserts low and stays asserted until the voltage at UVIN2 exceeds its threshold. The open-drain output has a 30 μ A internal pullup to V _{CC} .
17	$\overline{\text{OVOUT1}}$	Active-Low Overvoltage Output 1. When the voltage at OVIN1 rises above its threshold, $\overline{\text{OVOUT1}}$ asserts low and stays asserted until the voltage at OVIN1 falls below its threshold. The open-drain output has a 30 μ A internal pullup to V _{CC} .
18	$\overline{\text{UVOUT1}}$	Active-Low Undervoltage Output 1. When the voltage at UVIN1 falls below its threshold, $\overline{\text{UVOUT1}}$ asserts low and stays asserted until the voltage at UVIN1 exceeds its threshold. The open-drain output has a 30 μ A internal pullup to V _{CC} .
19	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ asserts low when the voltage on any of the UVIN_ inputs falls below their respective thresholds, the voltage on any of the OVIN_ inputs goes above its respective threshold, or $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for at least the minimum reset timeout after all monitored UVIN_ inputs exceed their respective thresholds, all OVIN_ inputs fall below their respective thresholds, and $\overline{\text{MR}}$ is deasserted. This open-drain output has a 30 μ A internal pullup.
20	UVIN1	Undervoltage Threshold Input 1. When the voltage on UVIN1 falls below its threshold, $\overline{\text{UVOUT1}}$ asserts low.
21	OVIN1	Overvoltage Threshold Input 1. When the voltage on OVIN1 rises above its threshold, $\overline{\text{OVOUT1}}$ asserts low.
22	UVIN2	Undervoltage Threshold Input 2. When the voltages on UVIN2 falls below its threshold, $\overline{\text{UVOUT2}}$ asserts low.
23	OVIN2	Overvoltage Threshold Input 2. When the voltage on OVIN2 rises above its threshold, $\overline{\text{OVOUT2}}$ asserts low.
—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the only electrical connection to GND.

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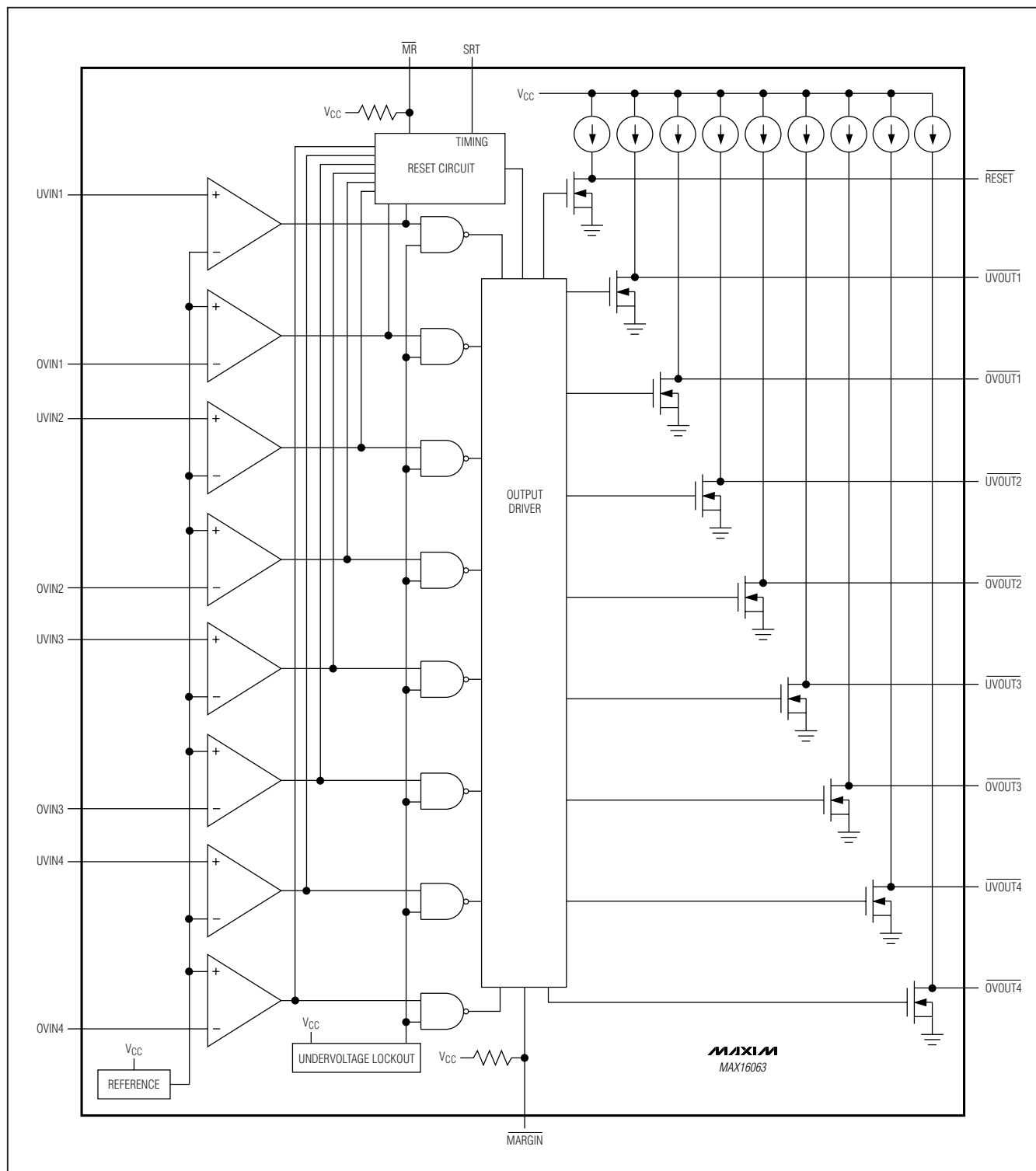


Figure 1. Functional Diagram

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Detailed Description

The MAX16063 is an adjustable quad window voltage detector in a small thin QFN package. This device is designed to provide a higher level of system reliability by monitoring multiple supply voltages and providing a fault signal when any of the voltages exceeds its overvoltage threshold or falls below its undervoltage threshold.

This device offers user-adjustable thresholds that allow voltages to be monitored down to 0.4V. It allows the upper and lower trip thresholds of each window detector to be set externally with the use of three external resistors.

Each monitored threshold has an independent open-drain output for signaling a fault condition. The outputs can be wire-ORed together to provide a single fault output. The open-drain outputs are internally pulled up with a 30μA current, but can be externally driven to other voltage levels for interfacing to other logic levels.

The MAX16063 features a margin input to disable the outputs during margin testing or any other time after power-up operations and a reset output that deasserts after a reset timeout period after all voltages are within their threshold specification. The reset timeout is internally set to 140ms (min), but can be externally adjusted to other reset timeouts using an external capacitor. In addition, a manual reset input is offered.

Applications Information

Voltage Monitoring

The MAX16063 features undervoltage and overvoltage comparators for window detection (see Figure 2). $\overline{\text{UVOUT}}$ / $\overline{\text{OVOUT}}$ deassert high when the monitored voltage is within the "selected window." When the monitored voltage falls below the lower limit of the window (V_{TRIPLOW}), $\overline{\text{UVOUT}}$ asserts low; or if the monitored voltage exceeds the upper limit (V_{TRIPHIGH}), $\overline{\text{OVOUT}}$ asserts low. The application in Figure 2 shows the MAX16063 enabling the DC-DC converter when the monitored voltage is in the selected window.

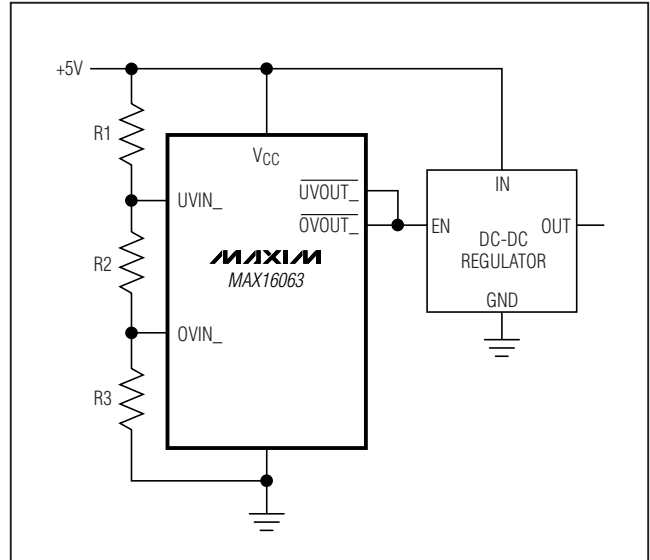


Figure 2. MAX16063 Monitor Circuit

The resistor values R1, R2, and R3 can be calculated as shown:

$$V_{\text{TRIPLOW}} = V_{\text{TH}} \left(\frac{R_{\text{TOTAL}}}{R_2 + R_3} \right)$$

$$V_{\text{TRIPHIGH}} = V_{\text{TH}} \left(\frac{R_{\text{TOTAL}}}{R_3} \right)$$

where $R_{\text{TOTAL}} = R_1 + R_2 + R_3$.

Use the following steps to determine the values for R1, R2, and R3:

- 1) Choose a value for R_{TOTAL} , the sum of R1, R2, and R3. Because the MAX16063 has very low input bias current (2nA typ), R_{TOTAL} can be up to 2MΩ. Large-value resistors help minimize power consumption. Lower-value resistors can be used to maintain overall accuracy.

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Use the following formulas to calculate the error:

$$E_{UV}(\%) = \frac{I_B \left(R1 + \frac{R1 R3}{R2 + R3} \right)}{V_{TRIPLOW}} \times 100$$

$$E_{OV}(\%) = \frac{I_B (R2 + (2 \times R1))}{V_{TRIPHIGH}} \times 100$$

where E_{UV} and E_{OV} are the undervoltage and overvoltage error (in %), respectively.

- Calculate $R3$ based on R_{TOTAL} and the desired upper trip point:

$$R3 = \frac{V_{TH} \times R_{TOTAL}}{V_{TRIPHIGH}}$$

- Calculate $R2$ based on R_{TOTAL} , $R3$, and the desired lower trip point:

$$R2 = \frac{V_{TH} \times R_{TOTAL}}{V_{TRIPLOW}} - R3$$

- Calculate $R1$ based on R_{TOTAL} , $R3$, and $R2$:

$$R1 = R_{TOTAL} - R2 - R3$$

Overvoltage Shutdown

The MAX16063 is ideal for overvoltage-shutdown applications. Figure 3 shows a typical circuit for this application using a pass p-channel MOSFET. The MAX16063 is

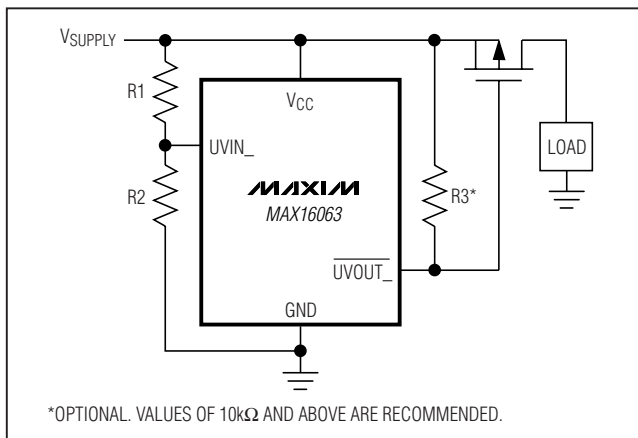


Figure 3. Overvoltage Shutdown Circuit (with External Pass MOSFET)

powered directly from the system voltage supply. Select $R1$ and $R2$ to set the trip voltage. When the supply voltage remains below the selected threshold, a low logic level on $UVOUT_$ turns on the p-channel MOSFET. In the case of an overvoltage event, $UVOUT_$ goes high turning off the MOSFET, and shuts down the power to the load.

Figure 4 shows a similar application using a fuse and a silicon-controlled rectifier (SCR). An overvoltage event turns on the SCR and shorts the supply to ground. The surge of current through the short circuit blows the fuse and terminates the current to the load. Select $R3$ so that the gate of the SCR is properly biased when $UVOUT_$ goes high.

Unused Inputs

Any unused $UVIN_$ inputs must be connected to V_{CC} , and any unused $OVIN_$ inputs must be connected to GND.

UVOUT_/OVOUT_ Outputs

$UVOUT_$ and $OVOUT_$ outputs assert low when $UVIN_$ and $OVIN_$, respectively, drop below or exceed their specified thresholds. The undervoltage/overvoltage outputs are open-drain with a (30μA) internal pullup to V_{CC} . For many applications, no external pullup resistor is required to interface with other logic devices. An external pullup resistor to any voltage up to 5.5V overdrives the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to V_{CC} (Figure 5). When choosing the external pullup resistor, the resistance value should be large enough to ensure that the output can sink the necessary current during a logic-low condition and small enough to be able to overdrive the internal pullup current and meet output high specifications (V_{OH}). Resistor values of 50kΩ to 200kΩ can generally be used.

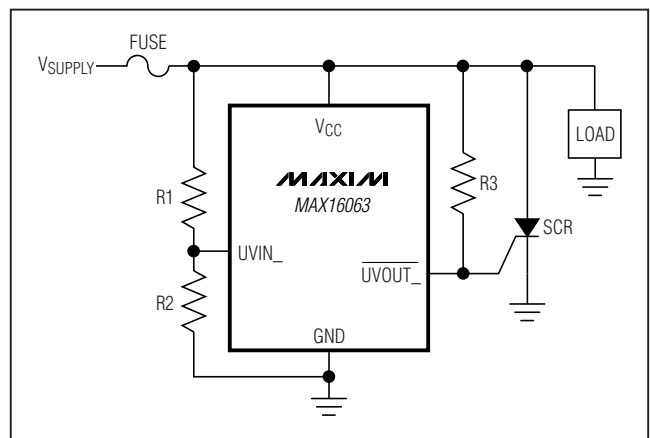


Figure 4. Overvoltage Shutdown Circuit (with SCR Fuse)

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RESET Output

$\overline{\text{RESET}}$ asserts low when the voltage on any of the UVIN_ inputs falls below its respective threshold, the voltage on any of the OVIN_ inputs goes above its respective threshold, or $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for the reset timeout period after all monitored UVIN_ inputs exceed their respective thresholds, all OVIN_ inputs fall below their respective thresholds, and $\overline{\text{MR}}$ is deasserted (see Figure 6). This open-drain output has a 30 μA internal pullup.

Reset Timeout Capacitor

The reset timeout period can be adjusted to accommodate a variety of microprocessor (μP) applications. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and GND. Calculate the reset timeout capacitor as follows:

$$C_{\text{SRT}} (\text{F}) = \frac{t_{\text{RP}} (\text{s})}{\left(\frac{V_{\text{TH_SRT}}}{I_{\text{SRT}}} \right)}$$

Connect SRT to V_{CC} for a factory-programmed reset timeout of 140ms (min).

Manual Reset Input ($\overline{\text{MR}}$)

Many μP -based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic-low on $\overline{\text{MR}}$ asserts $\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ remains asserted while $\overline{\text{MR}}$ is low, and during the reset timeout period (140ms min) after $\overline{\text{MR}}$ returns high. The $\overline{\text{MR}}$ input has an internal 20k Ω pullup resistor to V_{CC} , so it can be left open if it is not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1 μF capacitor from $\overline{\text{MR}}$ to GND provides additional noise immunity.

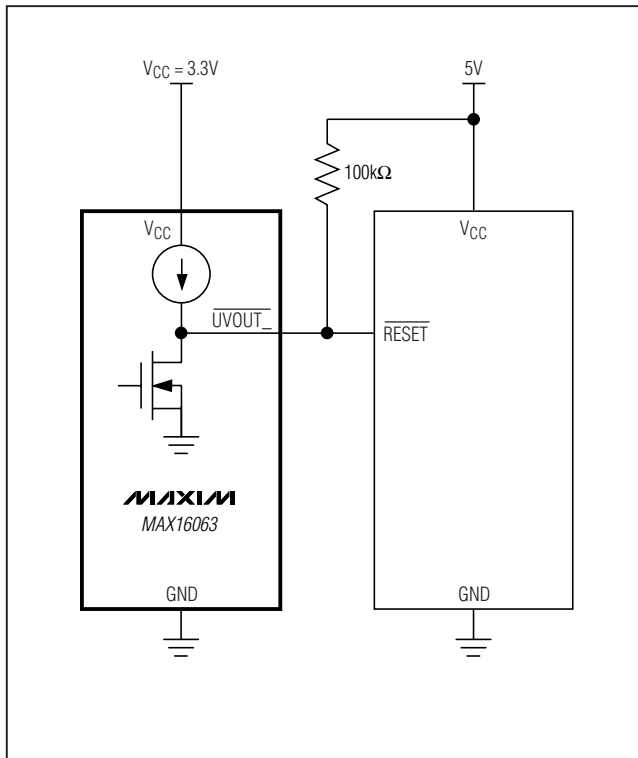


Figure 5. Interfacing to a Different Logic Supply Voltage

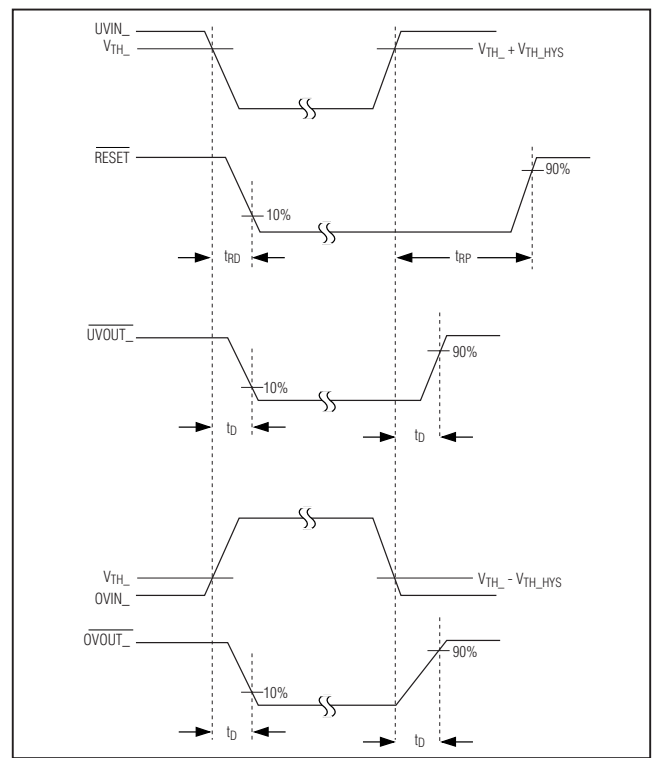


Figure 6. Output Timing Diagram

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Margin Output Disable (MARGIN)

MARGIN allows system-level testing while power supplies are adjusted from their nominal voltages. Drive MARGIN low to deassert all outputs (UVOUT_, OVOUT_, and RESET) regardless of the voltage at any monitored input. The state of each output does not change while MARGIN = GND. While MARGIN is low, the IC continues to monitor all voltages. When MARGIN is deasserted, the outputs go to their monitored states after a short propagation delay. The MARGIN input is internally pulled up to VCC. Leave unconnected or connect to VCC if unused.

Undervoltage Lockout (UVLO)

The MAX16063 features a VCC undervoltage lockout (UVLO) that preserves a reset status even if VCC falls as low as 1V. The undervoltage lockout circuitry monitors the voltage at VCC. If VCC falls below the UVLO falling threshold (typically 1.735V), RESET is asserted and all

detector outputs are asserted low. This eliminates an incorrect RESET or detector output state as VCC drops below the normal VCC operational voltage range of 1.98V to 5.5V.

During power-up as VCC rises above 1V, RESET is asserted and all detector outputs are asserted low until VCC exceeds the UVLO threshold. As VCC exceeds the UVLO threshold, all inputs are monitored and the correct output state appears at all the outputs. This also ensures that RESET and all detector outputs are in the correct state once VCC reaches the normal VCC operational range.

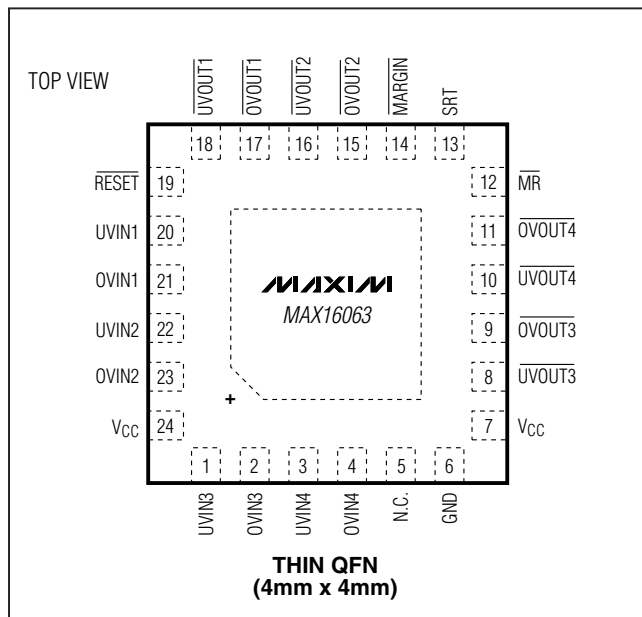
Power-Supply Bypassing

In noisy applications, bypass VCC to ground with a 0.1μF capacitor as close to the device as possible. In addition, the additional capacitor improves transient immunity. For fast-rising VCC transients, additional capacitance may be required.

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Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to
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PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN	T2444-4	21-0139

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Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 13

AMEYA360

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Website :

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Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com