

September 2014

#### FDZ1323NZ

# Common Drain N-Channel 2.5 V PowerTrench® WL-CSP MOSFET 20 V, 10 A, 13 m $\Omega$

#### **Features**

- Max  $r_{S1S2(on)} = 13 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_{S1S2} = 1 \text{ A}$
- Max  $r_{S1S2(on)} = 13 \text{ m}\Omega$  at  $V_{GS} = 3.8 \text{ V}$ ,  $I_{S1S2} = 1 \text{ A}$
- Max  $r_{S1S2(on)} = 16 \text{ m}\Omega$  at  $V_{GS} = 3.1 \text{ V}$ ,  $I_{S1S2} = 1 \text{ A}$
- Max  $r_{S1S2(on)} = 18 \text{ m}\Omega$  at  $V_{GS} = 2.5 \text{ V}$ ,  $I_{S1S2} = 1 \text{ A}$
- Occupies only 3 mm<sup>2</sup> of PCB area
- Ultra-thin package: less than 0.35 mm height when mounted to PCB
- High power and current handling capability
- HBM ESD protection level > 3.6 kV (Note 3)
- RoHS Compliant

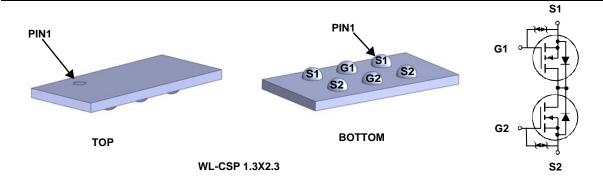


#### **General Description**

This device is designed specifically as a single package solution for Li-lon battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench® process with state of the art "low pitch" WLCSP packaging process, the FDZ1323NZ minimizes both PCB space and  $r_{\rm S1S2(on)}$ . This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge and low  $r_{\rm S1S2(on)}$ .

#### **Applications**

- Battery management
- Load switch
- Battery protection



#### **MOSFET Maximum Ratings** T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Paramete	er		Ratings	Units
V <sub>S1S2</sub>	Source1 to Source2 Voltage			20	V
$V_{GS}$	Gate to Source Voltage		±12	V	
	Source1 to Source2 Current -Continuous	T <sub>A</sub> = 25°C	(Note 1a)	10	۸
IS1S2	-Pulsed			40	— A
Б	Power Dissipation	T <sub>A</sub> = 25°C	(Note 1a)	2	10/
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25°C	(Note 1b)	0.5	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	62	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	257	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
EC	FDZ1323NZ	WL-CSP 1.3X2.3	7 "	8 mm	5000 units

Units

Max

#### **Electrical Characteristics** T<sub>J</sub> = 25 °C unless otherwise noted

**Parameter** 

Off Charac	Off Characteristics					
I <sub>S1S2</sub>	Zero Gate Voltage Source1 to Source2 Current	V <sub>S1S2</sub> = 16 V, V <sub>GS</sub> = 0 V			1	μА
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 12 \text{ V}, V_{S1S2} = 0 \text{ V}$			±10	μΑ

**Test Conditions** 

#### **On Characteristics**

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{S1S2}, I_{S1S2} = 250 \mu A$	0.4	0.9	1.2	V
「S1S2(on)		$V_{GS} = 4.5 \text{ V}, I_{S1S2} = 1 \text{ A}$	4.5	9.7	13	
		$V_{GS} = 3.8 \text{ V}, I_{S1S2} = 1 \text{ A}$	5.5	10	13	
	Static Source1 to Source2 On Resistance	V <sub>GS</sub> = 3.1 V, I <sub>S1S2</sub> = 1 A	7	11	16	$m\Omega$
		V <sub>GS</sub> = 2.5 V, I <sub>S1S2</sub> = 1 A	8	13	18	
		$V_{GS} = 4.5 \text{ V}, I_{S1S2} = 1 \text{ A}, T_J = 125 ^{\circ}\text{C}$		13	20	
g <sub>FS</sub>	Forward Transconductance	V <sub>S1S2</sub> = 5 V, I <sub>S1S2</sub> = 1 A		9		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 40.V V 0.V	1545	2055	pF
C <sub>oss</sub>	Output Capacitance	V <sub>S1S2</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	269	405	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 101112	252	380	pF

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		12	22	ns
t <sub>r</sub>	Rise Time	V <sub>S1S2</sub> = 10 V, I <sub>S1S2</sub> = 1 A,	13	23	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$	34	54	ns
t <sub>f</sub>	Fall Time		13	23	ns
$Q_q$	Total Gate Charge		17	24	nC
$Q_{gs}$	Gate to Source1 Gate Charge	$V_{S1S2} = 10 \text{ V}, I_{S1S2} = 1 \text{ A},$ $V_{G1S1} = 4.5 \text{ V}, V_{G2S2} = 0 \text{ V}$	1.9		nC
$Q_{gd}$	Gate to Source2 "Miller" Charge	VG1S1 = 4.5 V, VG2S2 = 0 V	5.4		nC

#### **Source1 to Source2 Diode Characteristics**

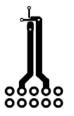
fss	Maximum Continuous Source1 to Source2 Diode Forward Current			1	Α
	Source1 to Source2 Diode Forward	$V_{G1S1} = 0 \text{ V}, V_{G2S2} = 4.5 \text{ V},$	0.6	1.2	V
<sup>V</sup> fss	Voltage	$I_{fss} = 1 A$ (Note 2)	0.6	1.2	V

#### Notes:

1. R<sub>BJA</sub>. Is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>BJC</sub> is guaranteed by design while R<sub>BCA</sub> is determined by the user's board design.



a. 62 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 257 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 us, Duty cycle < 2.0%.
- 3. The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

#### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

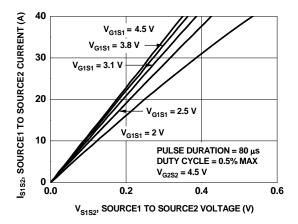


Figure 1. On-Region Characteristics

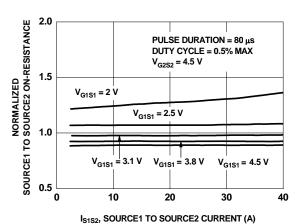


Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

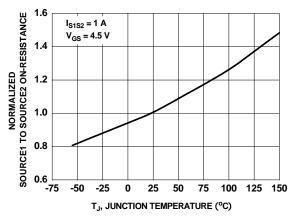


Figure 5. Normalized On Resistance vs Junction Temperature

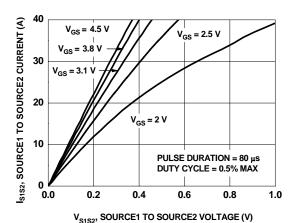


Figure 2. On-Region Characteristics

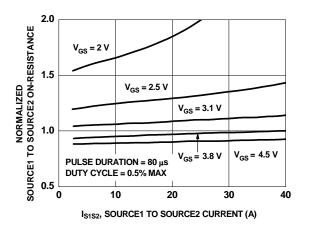


Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

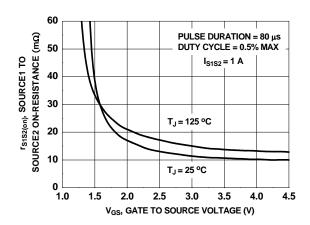


Figure 6. On Resistance vs Gate to Source Voltage

### Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

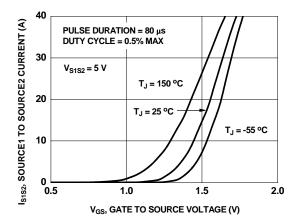


Figure 7. Transfer Characteristics

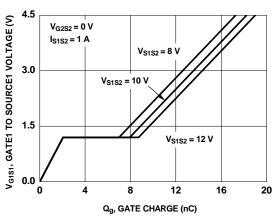


Figure 9. Gate Charge Characteristics

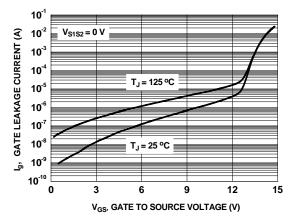
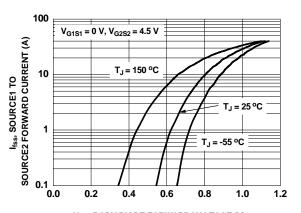


Figure 11. Gate Leakage Current vs Gate to Source Voltage



 $V_{fss}$ , BODY DIODE FORWARD VOLTAGE (V)

Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current

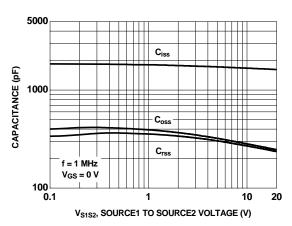
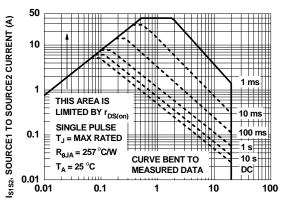


Figure 10. Capacitance vs Source1 to Source2 Voltage



V<sub>S1S2</sub>, SOURCE1 TO SOURCE2 VOLTAGE (V)

Figure 12. Forward Bias Safe Operating Area



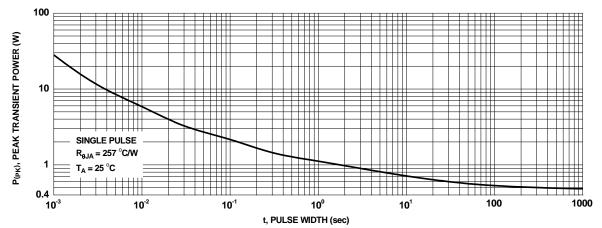


Figure 13. Single Pulse Maximum Power Dissipation

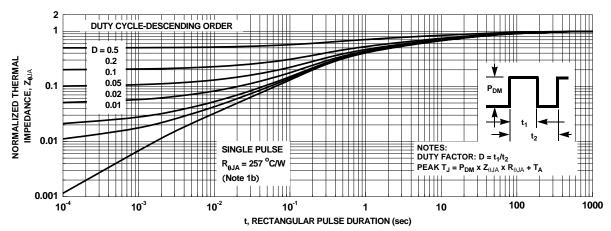
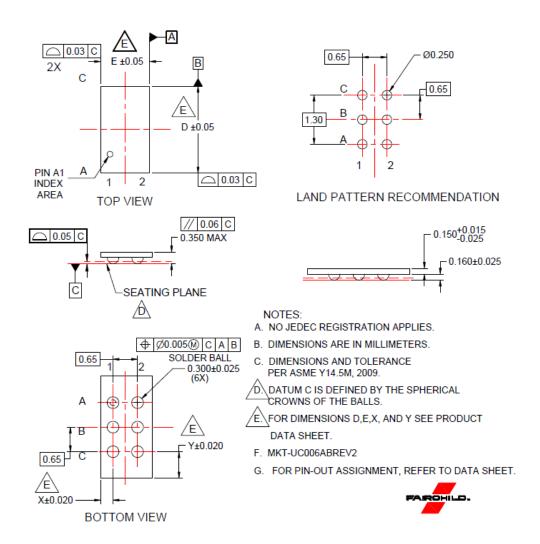


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

#### **Dimensional Outline and Pad Layout**



#### **Pin Definations:**

Gate	Source1	Source2
B1, B2	A1, C1	A2, C2

#### **Product Specific Dimensions:**

D	Е	X	Y
2.3 mm	1.3 mm	0.315 mm	0.49 mm

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