FAIRCHILD SEMICONDUCTOR®

August 2011

FMS6346E
Six-Channel, Selectable SD / HD Video Filter Driver with Disable

Features

- Three Selectable 8/30MHz (SD/HD) Filters
- Three Fixed 8MHz (SD) Filters
- Enable / Disable Pin
- Input Clamp and Bias
- Single Video Load Drive ($2V_{PP}$, 150Ω, A_V = 6dB)
- AC- or DC-Coupled Inputs
- AC- or DC-Coupled Outputs
- Robust Output ESD Protection: 9kV HBM

Applications

- Cable and Satellite Set-Top Boxes
- DVD Players
- HDTV
- Portable Media Players (PMP)
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

FMS6346E VoltagePlus™ video filter is intended to replace passive LC filters and drivers with a cost-effective integrated device. Six Butterworth filters improve image quality compared to typical passive solutions. The combination of low-power Standard-Definition (SD) and High-Definition (HD) filters greatly simplifies DVD video output circuitry. Three channels offer fixed SD 6th-order filters, while the other three are selectable between SD and HD 7th-order filters.

The FMS6346E offers a fixed gain of 6dB.

The FMS6346E may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required *(see the Applications Information section for details)*.

The outputs can drive AC- or DC-coupled single (150Ω) video loads. DC-coupling the outputs remove the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output.

Ordering Information

Part Number	Operating Temperature Range	Gain Setting	Package	Packing Method
FMS6346EMTC20X	-40°C to +85°C	6dB	20-Lead, Thin-Shrink Small-Outline Package (TSSOP)	2500 Units per Reel

Functional Block Diagram

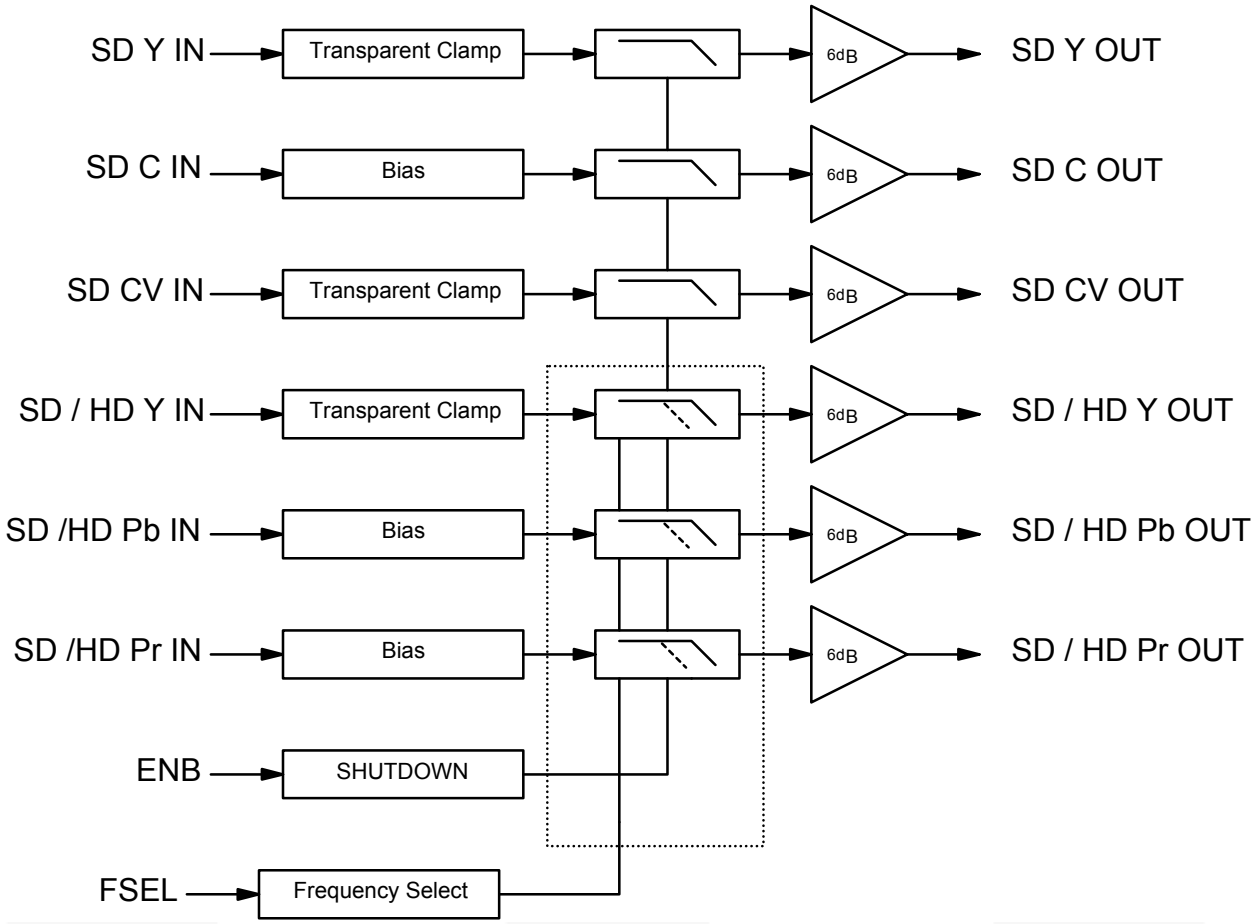


Figure 1. Block Diagram

Pin Configuration

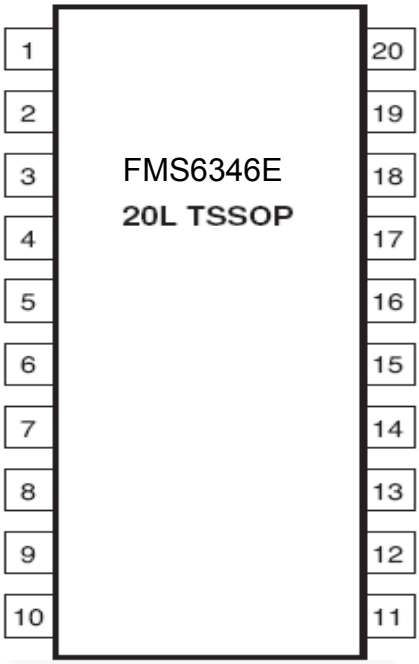


Figure 2. Pin Layout

Pin Definitions

Pin#	Name	Type	Description
1	SD Y IN1	Input	SD Y Video Input, Channel 1
2	SD C IN2	Input	SD C Video Input, Channel 2
3	SD CV IN3	Input	SD CV Video Input, Channel 3
4	ENB	Input	Enable / Disable, ENB = GND (0): Device Enabled; ENB = HIGH (1): Device Disabled
5	V_{CC}	Input	+3.3V or 5.0V Supply
6	F_{cSEL}	Input	Selects Filter Corner Frequency for Pins 7, 8, and 9: “0” = SD, “1” = HD
7	SD/HD Y IN1	Input	Selectable SD or HD Y Video Input, Channel 1
8	SD/HD Pb IN2	Input	Selectable SD or HD Pb Video Input, Channel 2
9	SD/HD Pr IN3	Input	Selectable SD or HD Pr Video Input, Channel 3
10	N/C	Input	No Connection
11	N/C	Input	No Connection
12	SD/HD Pr OUT3	Output	Filtered SD or HD Pr Video Output, Channel 3
13	SD/HD Pb OUT2	Output	Filtered SD or HD Pb Video Output, Channel 2
14	SD/HD Y OUT1	Output	Filtered SD or HD Y Video Output, Channel 1
15	N/C	Input	No Connection
16	GND	Input	Must Be Tied to Ground
17	GND	Input	Must Be Tied to Ground
18	SD CV OUT3	Output	Filtered SD CV Video Output, Channel 3
19	SD C OUT2	Output	Filtered SD C Video Output, Channel 2
20	SD Y OUT1	Output	Filtered SD Y Video Output, Channel 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
I_{OUT}	Output Current, Any One Channel, Do Not Exceed		50	mA

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Reflow Temperature			+260	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard Multi-Layer Test Boards, Still Air		74		°C/W

Electrostatic Discharge Information

Symbol	Parameter	Max.	Unit
ESD	Human Body Model, JESD22-A114	9	kV
	Charged Device Model, JESD22-C101	2	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	Supply Voltage Range	3.135	3.300	5.250	V

DC Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{CC}=3.3V, R_{SOURCE}=37.5Ω, inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads, and referenced to 400kHz.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current(1)	V_{CC} = 3.3V, No Load, EN=LOW		50	62	mA
		V_{CC} = 5.0V, No Load, EN = LOW		60	70	mA
I_{CC_SD}	Shutdown Supply Current	V_{CC} = 3.3V or 5.0V, No Load, EN = HIGH		10	200	µA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC Coupled		1.2		V_{PP}
V_{IL}	Digital Input Low(1)	EN = LOW, Device Enabled	0		0.8	V
V_{IH}	Digital Input High(1)	EN = HIGH, Device Disabled	2.4		V_{CC}	V
I_{EN_Low}	Input Current	V_{IL} = 0.8V		0.01	1.00	µA
I_{EN_HIGH}	Input Current	V_{IH} = 2.4V		0.01	1.00	µA
PSRR	Power Supply Rejection Ratio			-50		dB

Note:
1. 100% tested at TA=25°C.

Standard-Definition (480i) Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{IN}=1V_{PP}, V_{CC}=3.3V, R_{SOURCE}=37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads, and referenced to 400kHz.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{SD}	Channel Gain(2)	All SD Channels, DC	5.8	6.0	6.2	dB
f_{01dBSD}	-0.1dB Flatness	All SD Channels		5.5		MHz
f_{1dBSD}	-1dB Flatness(2)	All SD Channels	5.50	7.15		MHz
f_{cSD}	-3dB Bandwidth(2)	All SD Channels	6.5	8.0		MHz
f_{SBSD}	Attenuation (Stopband Reject)(2)	All SD Channels at f = 27MHz	50	60		dB
DG	Differential Gain	All SD Channels		0.2		%
DP	Differential Phase	All SD Channels		0.4		°
THD	Total Harmonic Distortion, Output	V_{OUT} = 1.4V_{PP}, 3.58MHz		0.4		%
X_{TALKSD}	Crosstalk (Channel-to-Channel)	1MHz		-70		dB
SNR	Signal-to-Noise Ratio(3)	NTC-7 Weighting, 100kHz to 4.2MHz		72		dB
t_{pdSD}	Propagation Delay	Delay from Input to Output, 4.5MHz		84		ns
CLG_{SD}	Chroma Luma Gain	f = 3.58MHz *(Refer to SD_{IN} at 400kHz)*		100		%
CLD_{SD}	Chroma Luma Delay	f = 3.58MHz *(Refer to SD_{IN} at 400kHz)*		6		ns

Notes:
2. 100% tested at T_A=25°C.
3. SNR=20 • log (714mV / rms noise).

High-Definition Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{IN}=1V_{PP}, V_{CC}=3.3V, R_{SOURCE}=37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads, and referenced to 400kHz.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV_{HD}	Channel Gain(4)	All HD Channels, DC	5.8	6.0	6.2	dB
$BW_{0.5dB}$	+/-0.5dB Bandwidth(4)	All HD Channels		28		MHz
BW_{-1dB}	-1dB Bandwidth(4)	All HD Channels	28	31		MHz
BW_{-3dB}	-3dB Bandwidth(4)	All HD Channels	30	32		MHz
$Att_{37.125M}$	Normalized Stopband Attenuation(4)	R_{SOURCE} = 75Ω, f = 37.325MHz		6.5		dB
$Att_{44.25M}$		R_{SOURCE} = 75Ω, f = 44.25MHz		14.5		dB
$Att_{74.25M}$		R_{SOURCE} = 75Ω, f = 74.25MHz	40	44		dB
Att_{78M}		R_{SOURCE} = 75Ω, f = 78MHz	42	46		dB
THD1	Output Distortion (All Channel)	f = 10MHz; V_{OUT} = 1.4V_{PP}		0.4		%
THD2		f = 15MHz; V_{OUT} = 1.4V_{PP}		0.4		%
THD2		f = 30MHz; V_{OUT} = 1.4V_{PP}		0.4		%
X_{TALKHD}	Crosstalk (Channel-to-Channel)	f = 1.0MHz; V_{OUT} = 1.4V_{PP}		-60		dB
SNR	Signal-to-Noise Ratio(5)	Weighted; 100kHz to 30MHz		72		dB
t_{pdHD}	Propagation Delay	Delay from Input to Output, 10MHz		24		ns

Notes:
4. 100% tested at 25°C.
5. SNR=20 • log (714mV / rms noise).

Typical Performance Characteristics

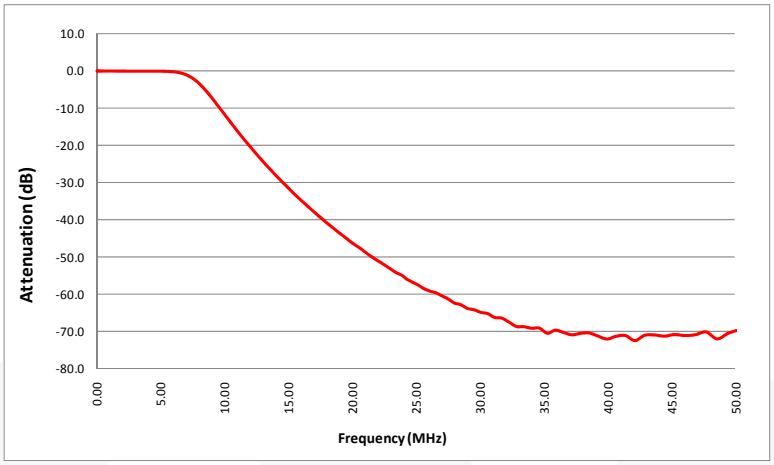


Figure 3. SD Frequency Response

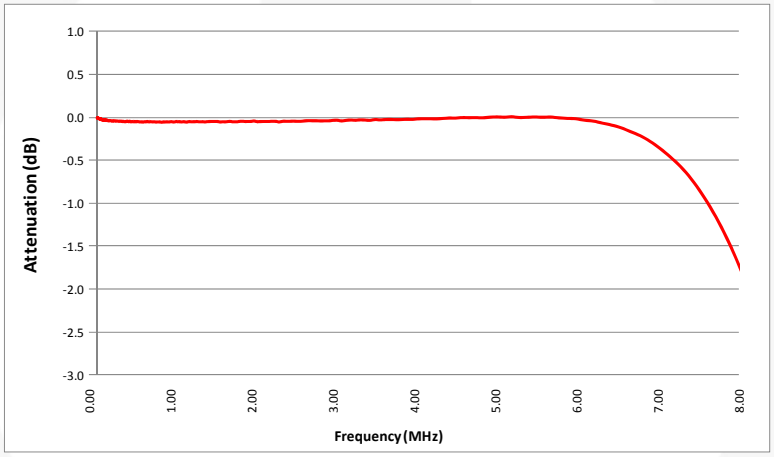


Figure 4. SD Frequency Response (Flatness)

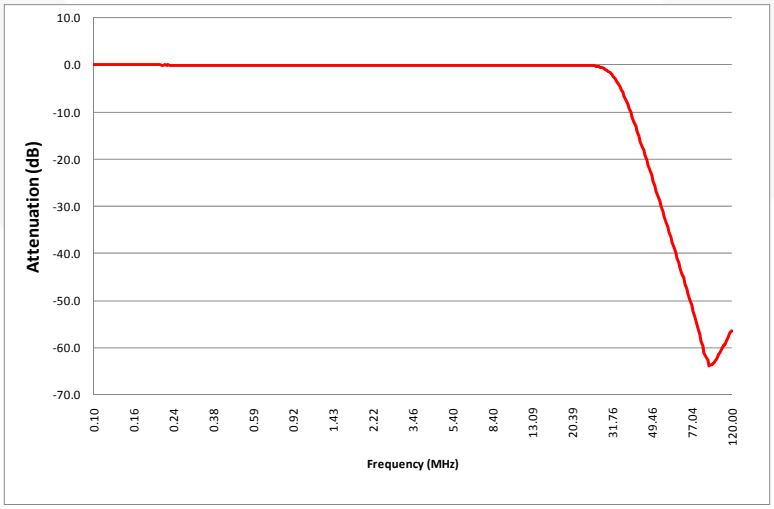


Figure 5. HD Frequency Response

Typical Performance Characteristics (Continued)

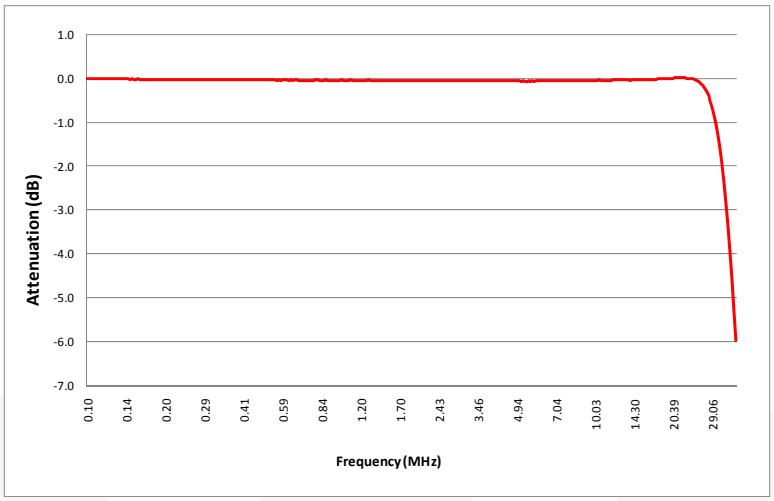


Figure 6. HD Frequency Response (Flatness)

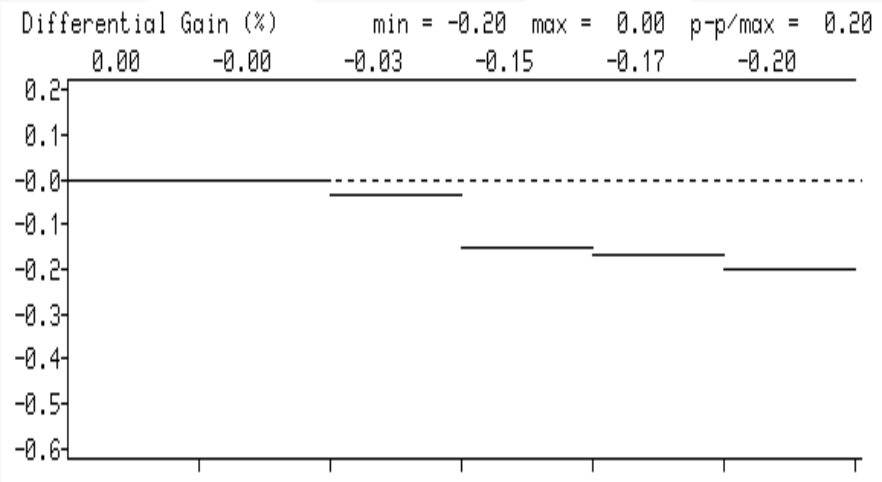


Figure 7. Differential Gain

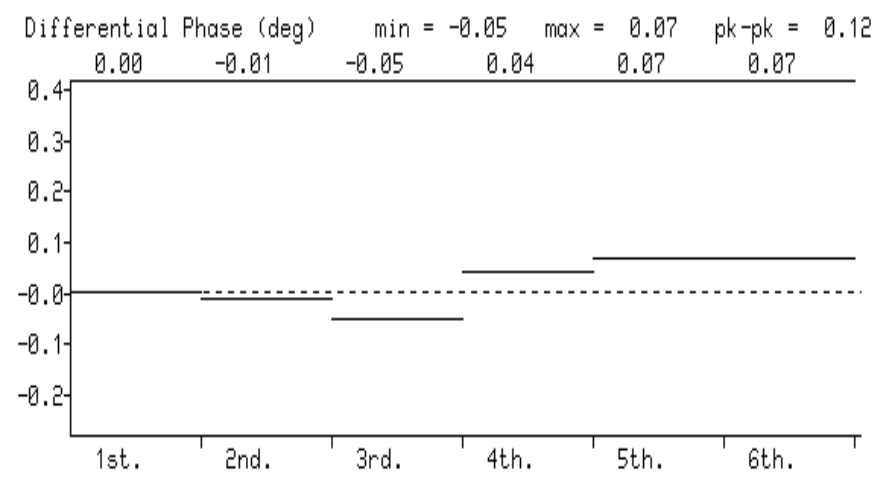


Figure 8. Differential Phase

Typical Application

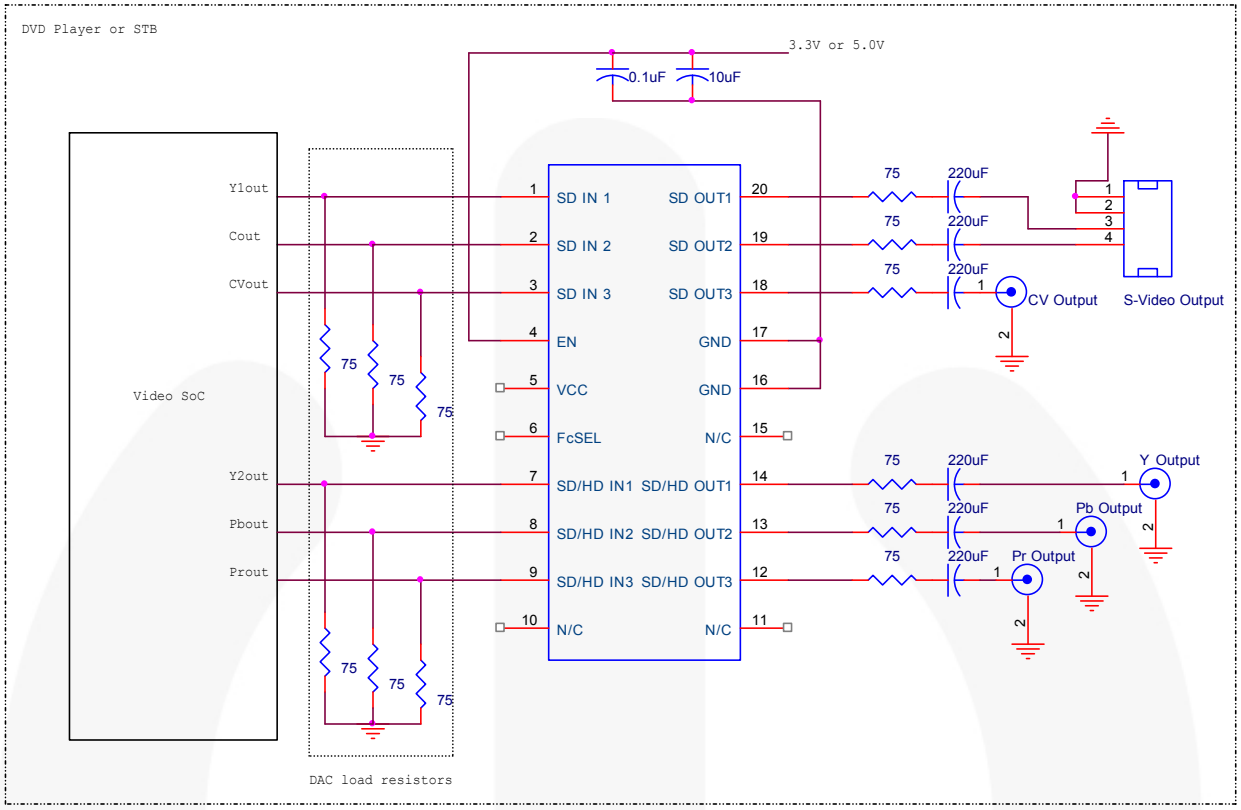
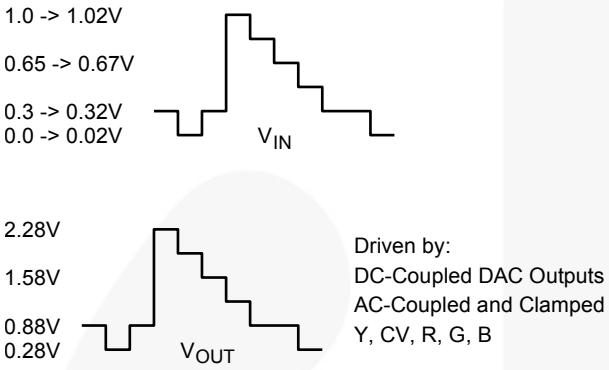


Figure 9. Typical Application

Applications Information

Functional Description

The FMS6346E VoltagePlus™ video filter provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 10.



There is a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 \cdot V_{IN} + 280mV$.

Figure 10. Typical Voltage Levels

The FMS6346E offers three channels with internal diode clamps and three channels with biasing to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6346E without an AC-coupling capacitor. The worst-case sync-tip compression due to the clamp does not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range. When the input is AC coupled, the diode clamp sets the sync-tip (or lowest voltage) just below ground.

For symmetric signals like C, Pb, and Pr; the average DC bias is fairly constant and the inputs are biased to set the DC input voltage to approximately 600mV. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 11.

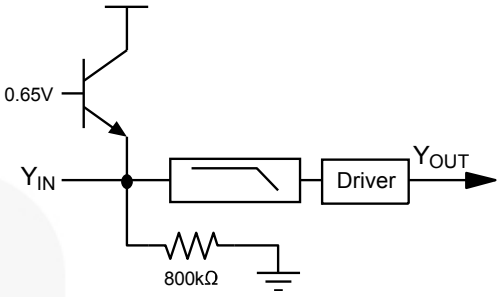


Figure 11. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use the configuration shown in Figure 12.

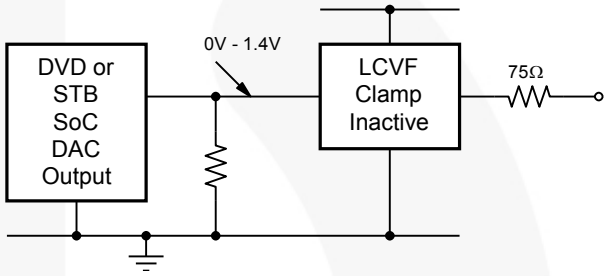


Figure 12. DC-Coupled Inputs and Outputs

If the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC coupled as shown in Figure 13.

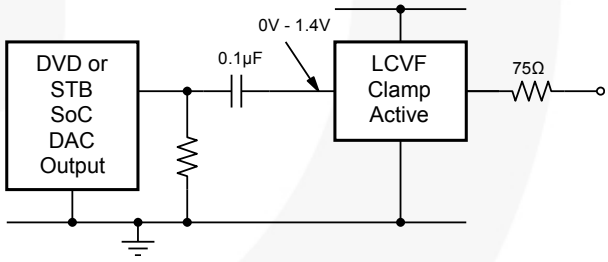


Figure 13. AC-Coupled Inputs, DC-Coupled Outputs

When driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC coupled as shown in Figure 14.

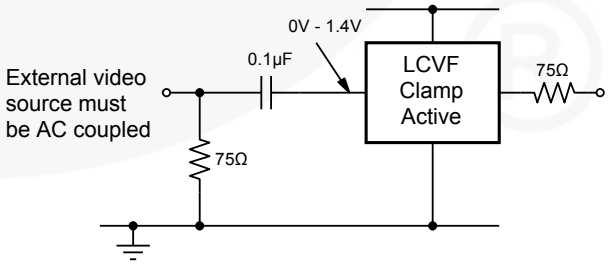


Figure 14. SCART Configuration with DC-Coupled Outputs

The same method can be used to bias the clamp signals.

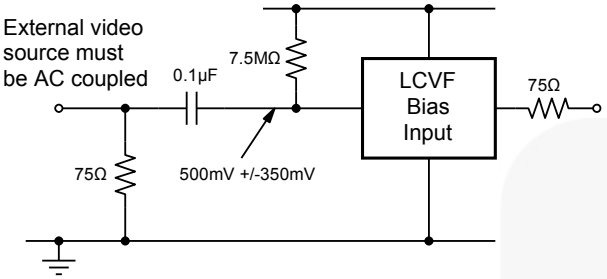


Figure 15. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired, as shown in Figure 16.

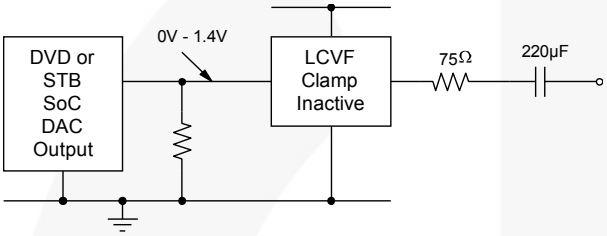


Figure 16. DC-Coupled Inputs, AC-Coupled Outputs

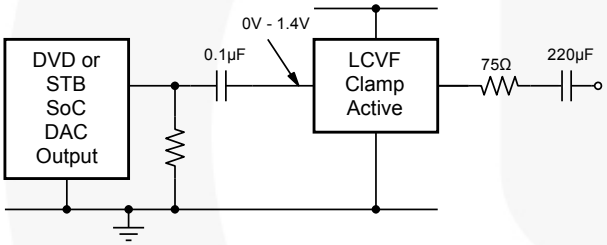


Figure 17. Coupled Inputs, AC-Coupled Outputs

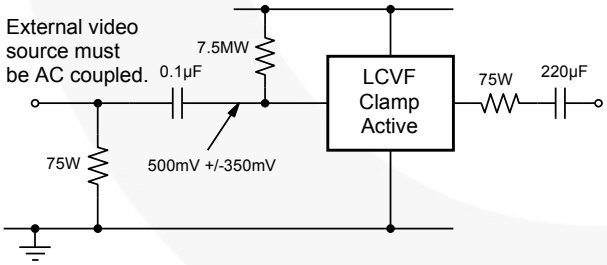


Figure 18. Biased SCART with AC-Coupled Outputs

Note:

6. The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6346E output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the power dissipation and internal temperature rise:

$$T_J = T_A + P_d \bullet \theta_{JA} \quad (1)$$

where $P_d = P_{CH1} + P_{CH2} + P_{CHx}$ and

$P_{CHx} = V_S \bullet I_{CH} - (V_O^2/R_L)$

where $V_O = 2V_{IN} + 0.280V$

$I_{CH} = (I_{CC} / 6) + (V_O/R_L)$

V_{IN} = RMS value of input signal

I_{CC} = 50mA, V_S = 3.3V

R_L = channel load resistance

Board layout affects thermal characteristics. *Refer to the Layout Considerations section for more information.*

Output Considerations

The FMS6346E outputs are DC offset from the input by 150mV; therefore $V_{OUT} = 2 \bullet V_{IN}$ DC+150mV. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6346E has a 2 x (6dB) gain, the output is typically connected via a 75Ω series back-matching resistor followed by the 75Ω video cable. Due to the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less then 1V. When AC-coupling the output, ensure that the coupling capacitor passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. The distance from the device pin to the series termination resistor should be no greater than 12.7mm (0.5in).

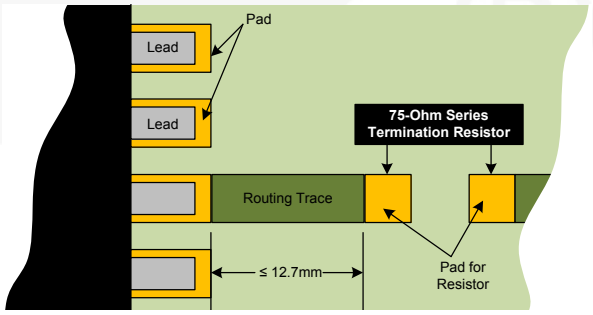


Figure 19. Termination Resistor Placement

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6346EDEMO, to guide layout and aid device testing and characterization.

The FMS6346EDEMO is a four-layer board with a full power and ground plane. Following this layout configuration provides the optimum performance and thermal characteristics. For best results, follow the steps below as a basis for high-frequency layout:

- Include 0.01µF and 0.1µF ceramic bypass capacitors.
- Place the 0.01µF capacitor within 0.75 inches of the power pin.
- Place the 0.1µF capacitor within 0.1 inches of the power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device by at least 0.5 inches.
- Minimize all trace lengths to reduce series inductances.

Physical Dimensions

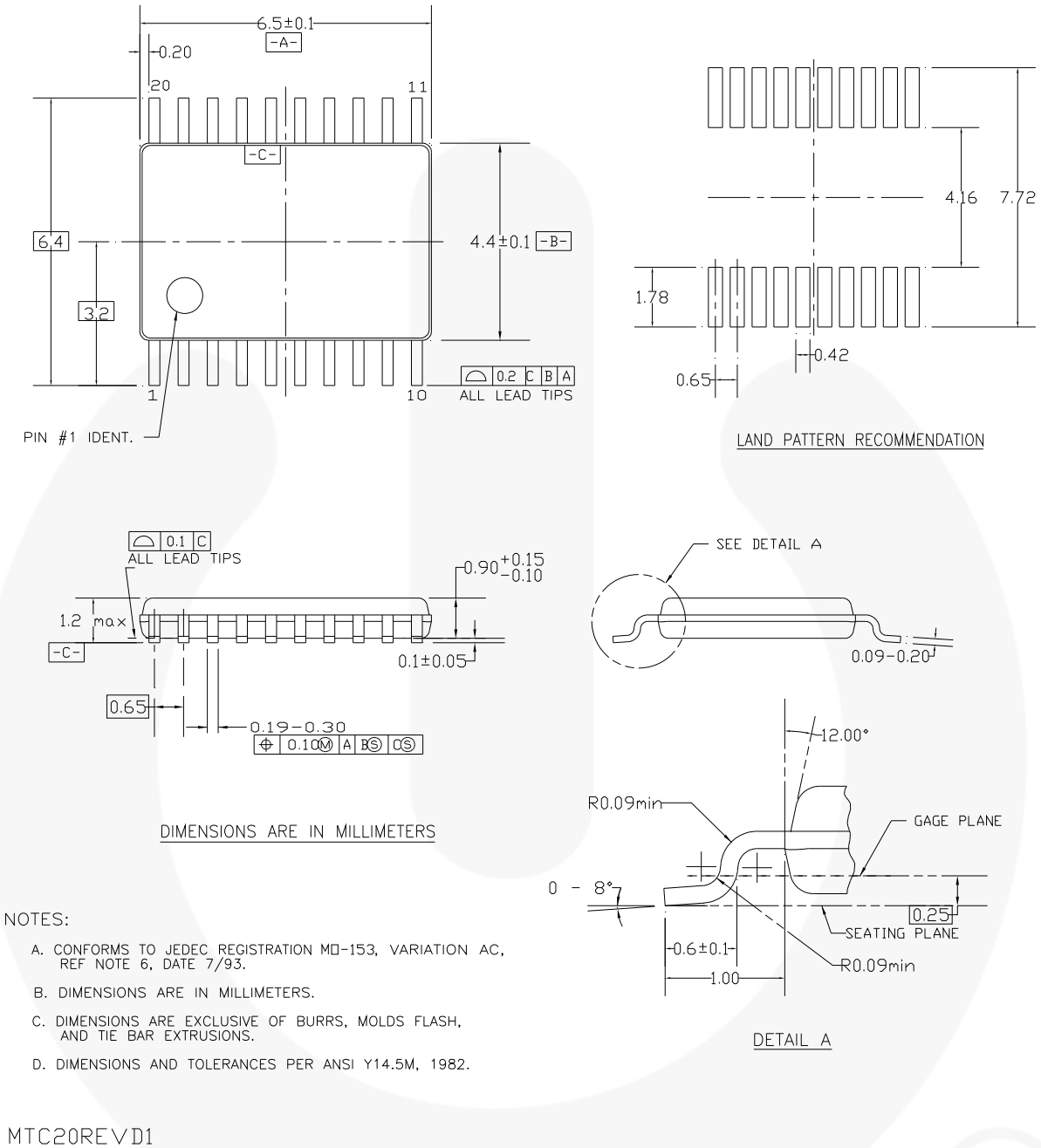


Figure 20. 20-Lead, Thin-Shrink Small-Outline Package (TSSOP)

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MicroFET™
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MicroPak2™
MillerDrive™
MotionMax™
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mWSaver™
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SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC®
TriFault Detect™
TRUECURRENT®*
μSerDes™
SerDes
UHC®
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UniFET™
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I57

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com