

OPA111

Low Noise Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE:** 100% Tested, $8\text{nV}\sqrt{\text{Hz}}$ max (10kHz)
- **LOW BIAS CURRENT:** 1pA max
- **LOW OFFSET:** 250 μV max
- **LOW DRIFT:** 1 $\mu\text{V}/^\circ\text{C}$ max
- **HIGH OPEN-LOOP GAIN:** 120dB min
- **HIGH COMMON-MODE REJECTION:** 100dB min

DESCRIPTION

The OPA111 is a precision monolithic dielectrically isolated FET (*Difet*[®]) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET[®] amplifiers.

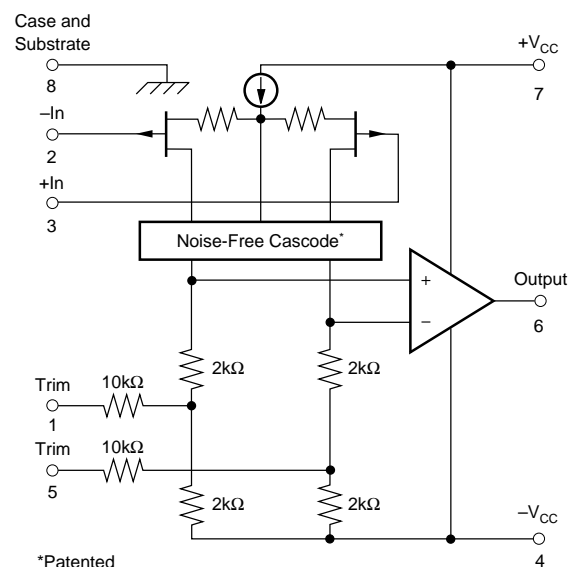
Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **OPTOELECTRONICS**
- **MEDICAL EQUIPMENT—CAT SCANNER**
- **RADIATION HARD EQUIPMENT**



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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITION	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, $f_O = 10\text{Hz}$	100% Tested		40	80		30	60		40	80	$\text{nV}/\sqrt{\text{Hz}}$
$f_O = 100\text{Hz}$	100% Tested		15	40		11	30		15	40	$\text{nV}/\sqrt{\text{Hz}}$
$f_O = 1\text{kHz}$	100% Tested		8	15		7	12		8	15	$\text{nV}/\sqrt{\text{Hz}}$
$f_O = 10\text{kHz}$	100% Tested		6	8		6	8		6	8	$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 10\text{Hz}$ to 10kHz	100% Tested		0.7	1.2		0.6	1		0.7	1.2	μVrms
Current, $f_B = 0.1\text{Hz}$ to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3	$\mu\text{Vp-p}$
Current, $f_B = 0.1\text{Hz}$ to 10Hz	(1)		9.5	15		7.5	12		9.5	15	fAp-p
$f_O = 0.1\text{Hz}$ thru 20kHz	(1)		0.5	0.8		0.4	0.6		0.5	0.8	$\text{fA}/\sqrt{\text{Hz}}$
OFFSET VOLTAGE ⁽²⁾											
Input Offset Voltage	$V_{CM} = 0\text{VDC}$		± 100	± 500		± 50	± 250		± 100	± 500	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		± 2	± 5		± 0.5	± 1		± 2	± 5	$\mu\text{V}/^\circ\text{C}$
Supply Rejection	$V_{CC} = \pm 10\text{V}$ to $\pm 18\text{V}$	90	110	± 31	100	110	± 10	90	110	± 31	dB $\mu\text{V/V}$
BIAS CURRENT ⁽²⁾											
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 0.8	± 2		± 0.5	± 1		± 0.8	± 2	pA
OFFSET CURRENT ⁽²⁾											
Input Offset Current	$V_{CM} = 0\text{VDC}$		± 0.5	± 1.5		± 0.25	± 0.75		± 0.5	± 1.5	pA
IMPEDANCE											
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$
VOLTAGE RANGE											
Common-Mode Input Range		± 10	± 11		± 10	± 11		± 10	± 11		V
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	90	110		100	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	114	125		120	125		114	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20Vp-p , $R_L = 2\text{k}\Omega$	16	32		16	32		16	32		kHz
Slew Rate	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	1	2		1	2		1	2		$\text{V}/\mu\text{s}$
Settling Time, 0.1%	Gain = -1 , $R_L = 2\text{k}\Omega$		6			6			6		μs
0.01%	10V Step		10			10			10		μs
Overload Recovery, 50% Overdrive ⁽³⁾	Gain = -1		5			5			5		μs
RATED OUTPUT											
Voltage Output	$R_L = 2\text{k}\Omega$	± 11	± 12		± 11	± 12		± 11	± 12		V
Current Output	$V_O = \pm 10\text{VDC}$	± 5.5	± 10		± 5.5	± 10		± 5.5	± 10		mA
Output Resistance	DC, Open Loop		100			100			100		Ω
Load Capacitance Stability	Gain = $+1$		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			± 15			± 15			± 15		VDC
Voltage Range, Derated Performance		± 5		± 18	± 5		± 18	± 5		± 18	VDC
Current, Quiescent	$I_O = 0\text{mADC}$		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	Ambient Temp.	-25		$+85$	-25		$+85$	-55		$+125$	$^\circ\text{C}$
Operating	Ambient Temp.	-55		$+125$	-55		$+125$	-55		$+125$	$^\circ\text{C}$
Storage	Ambient Temp.	-65		$+150$	-65		$+150$	-65		$+150$	$^\circ\text{C}$
θ Junction-Ambient			200			200			200		$^\circ\text{C}/\text{W}$

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

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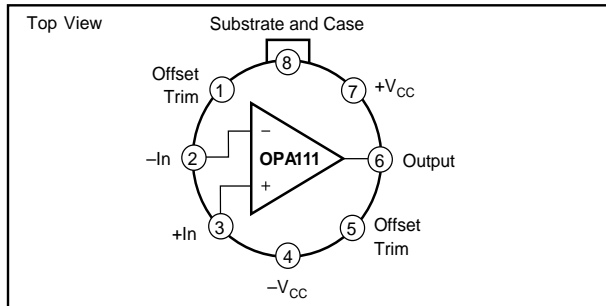
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITION	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient Temp.	-25		+85	-25		+85	-55		+125	°C
INPUT											
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$ $V_{CC} = \pm 10\text{V to } \pm 18\text{V}$		± 220 ± 2	± 1000 ± 5		± 110 ± 0.5	± 500 ± 1		± 300 ± 2	± 1500 ± 5	μV $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V/V}$
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$		± 50	± 250		± 30	± 130		± 820	± 4100	pA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$		± 30	± 200		± 15	± 100		± 510	± 3100	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10 86	± 11 100		± 10 90	± 11 100		± 10 86	± 11 100		V dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	110	120		114	120		110	120		dB
RATED OUTPUT											
Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	± 10.5 ± 5.25 10	± 11 ± 10 40		± 11 ± 5.25 10	± 11.5 ± 10 40		± 11 ± 5.25 10	± 11.5 ± 10 40		V mA mA
POWER SUPPLY											
Current, Quiescent	$I_O = 0\text{mADC}$		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ⁽¹⁾	750mW
Differential Input Voltage ⁽²⁾	±36VDC
Input Voltage Range ⁽²⁾	±18VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration ⁽³⁾	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on $\theta_{JC} = 150^\circ\text{C/W}$ or $\theta_{JA} = 300^\circ\text{C/W}$. (2) For supply voltages less than $\pm 18\text{VDC}$, the absolute maximum input voltage is equal to $+18\text{V} > V_{IN} > -V_{CC} - 6\text{V}$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .

PACKAGE INFORMATION

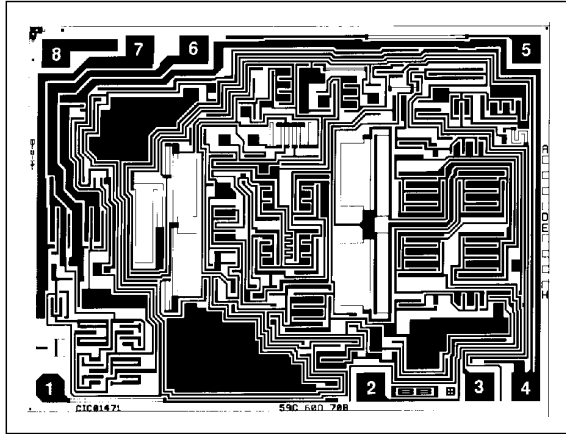
MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA111AM	TO-99	001
OPA111BM	TO-99	001
OPA111SM	TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, MAX (μV)
OPA111AM	TO-99	-25°C to +85°C	±500
OPA111BM	TO-99	-25°C to +85°C	±250
OPA111SM	TO-99	-55°C to +125°C	±500

DICE INFORMATION



OPA111AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V _s
5	Offset Trim
6	Output
7	+V _s
8	Substrate

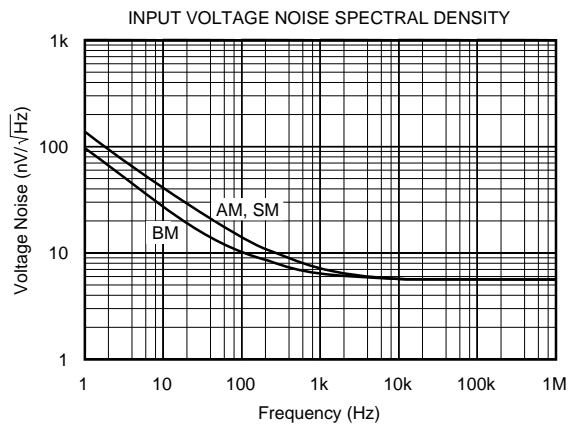
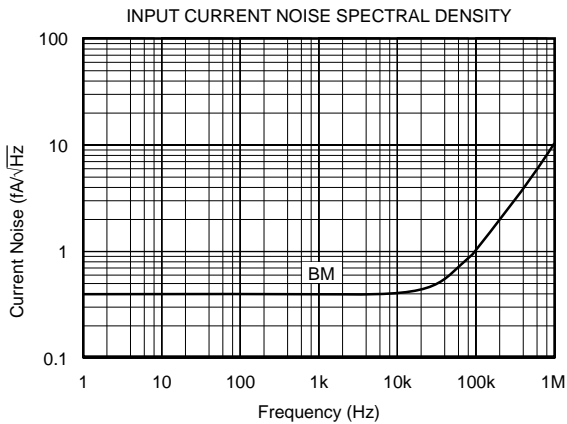
Substrate Bias: This Dielectrically-Isolated Substrate is normally connected to common.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	95 x 71 ±5	2.41 x 1.80 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:	None	
Transistor Count:	44	

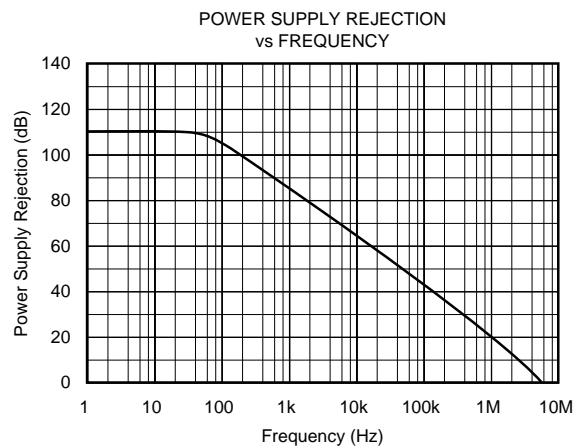
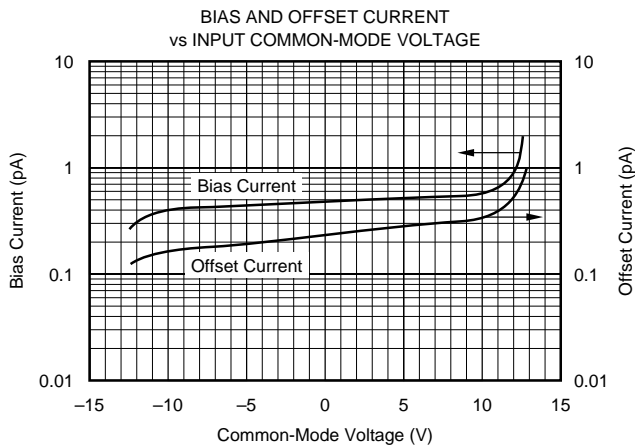
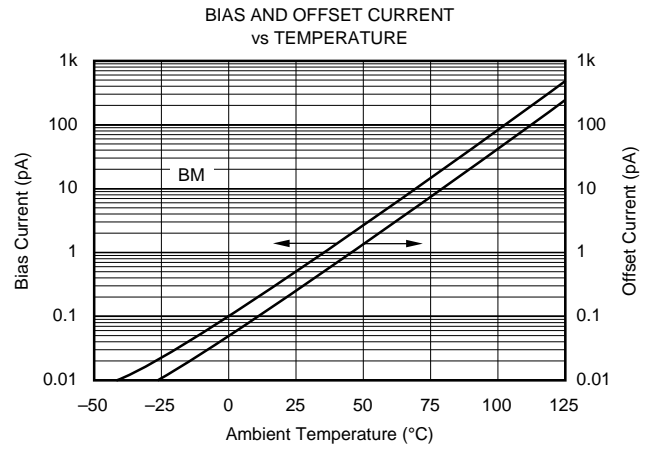
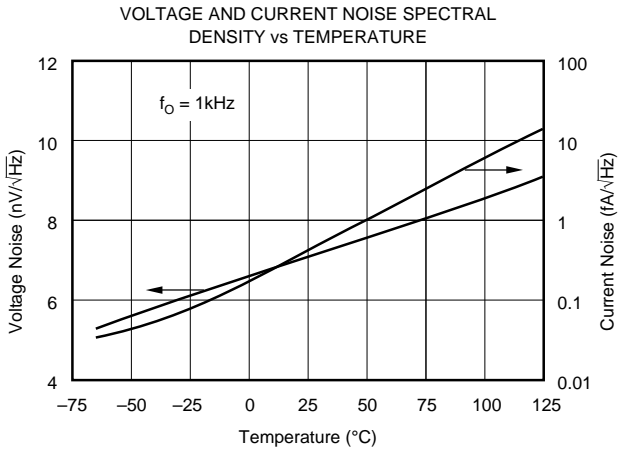
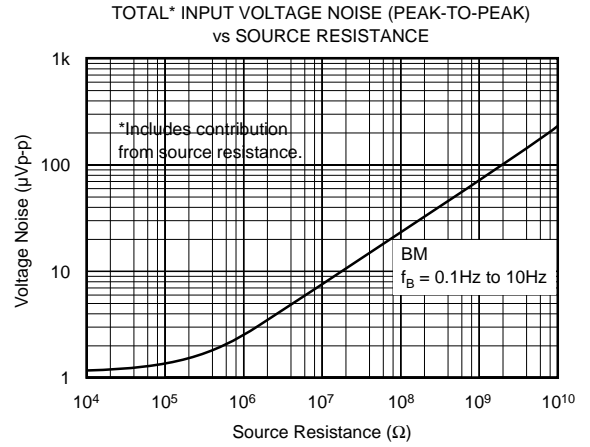
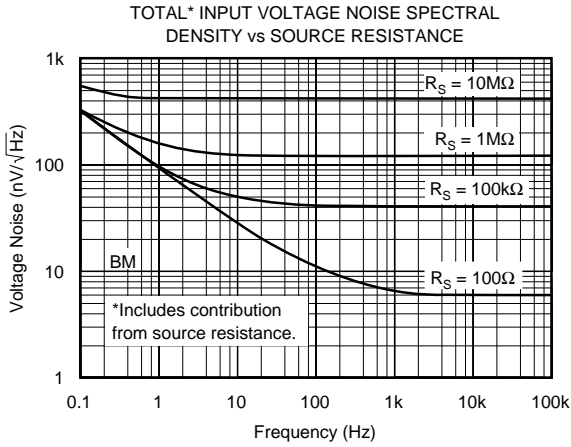
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

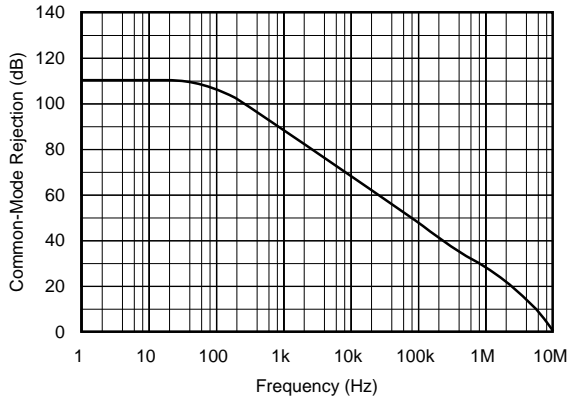
$T_A = +25^\circ\text{C}$, $V_{OC} = \pm 15\text{VDC}$ unless otherwise noted.



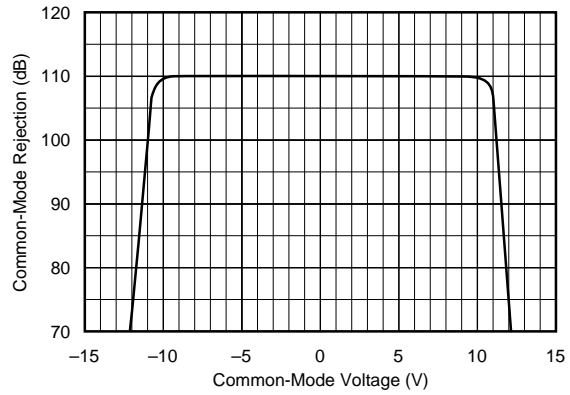
TYPICAL PERFORMANCE CURVES (CONT)

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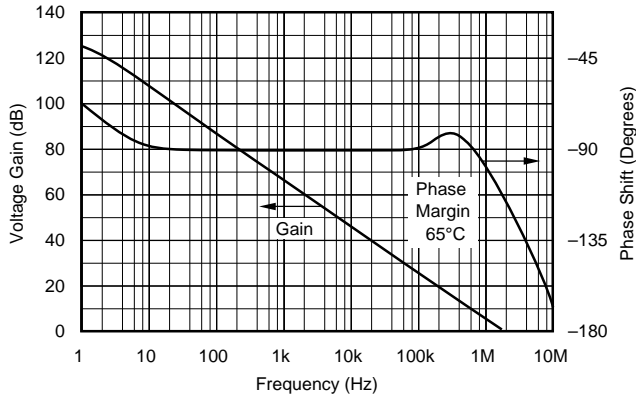
COMMON-MODE REJECTION
vs FREQUENCY



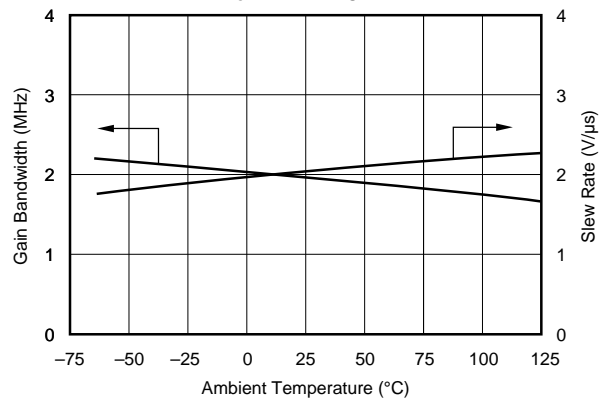
COMMON-MODE REJECTION
vs INPUT COMMON MODE VOLTAGE



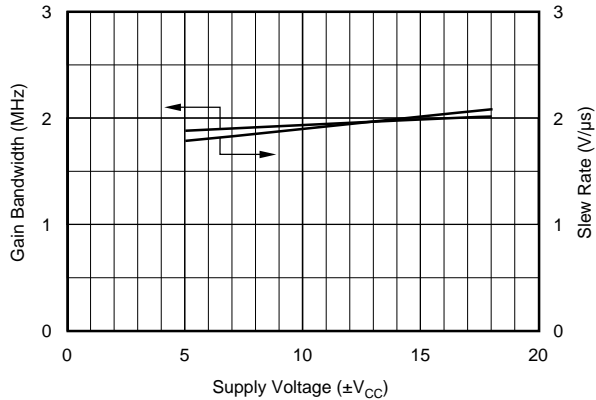
OPEN-LOOP FREQUENCY RESPONSE



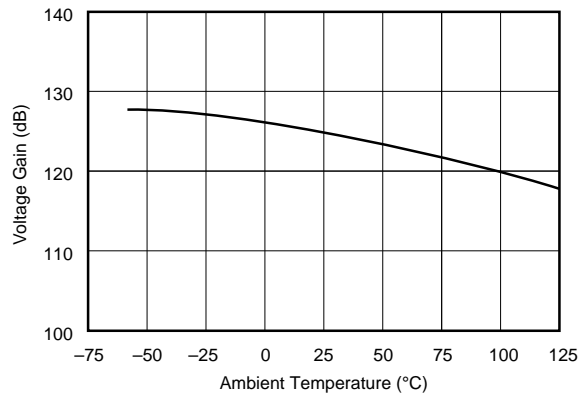
GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE

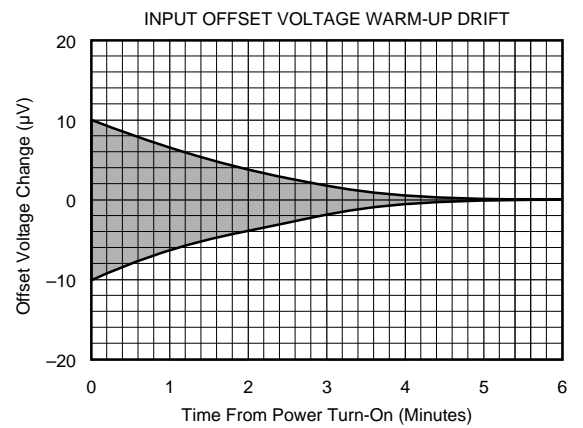
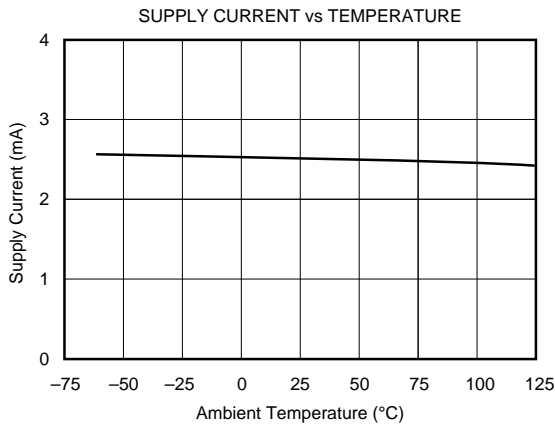
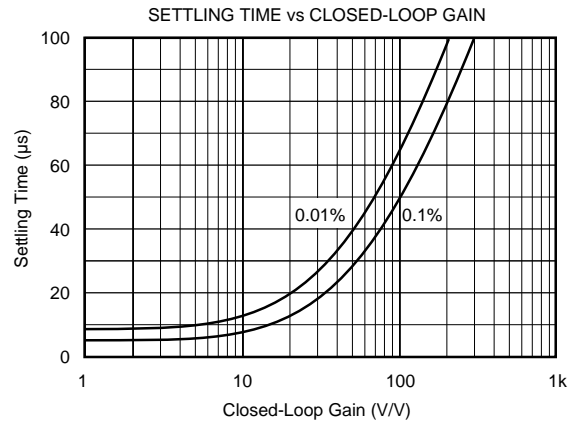
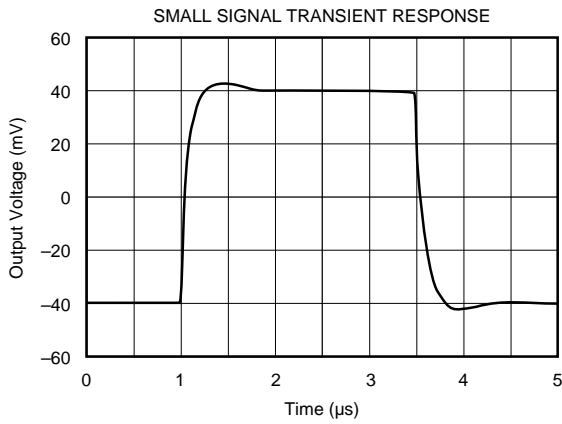
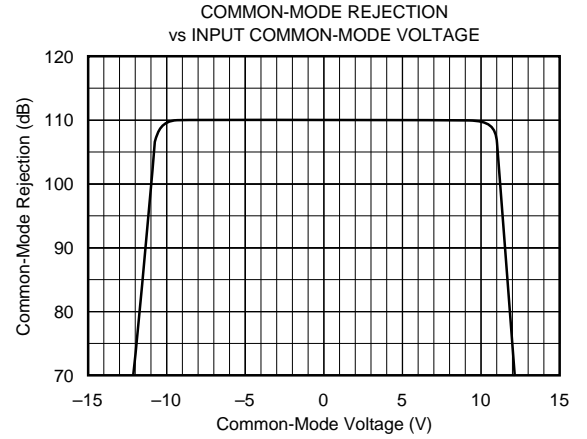
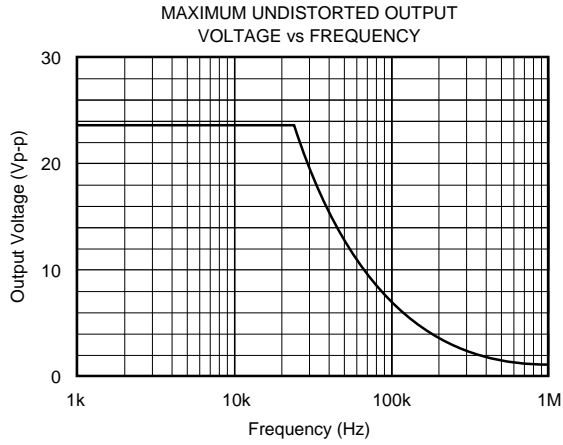


OPEN-LOOP GAIN vs TEMPERATURE



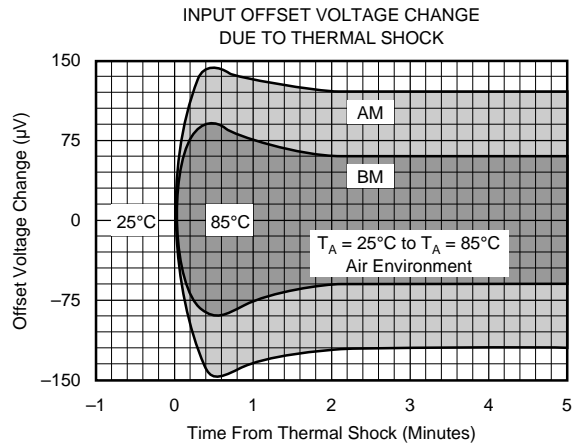
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA111 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA111 can replace most other amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

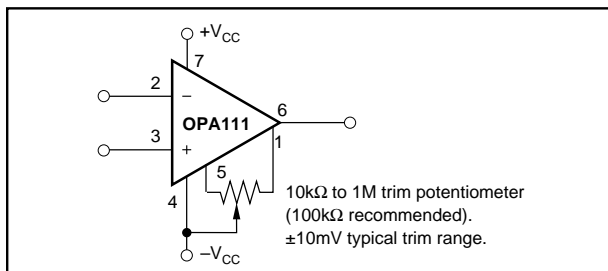


FIGURE 1. Offset Voltage Trim.

Unlike BIFET amplifiers, The *Difet* OPA111 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A $10\text{k}\Omega$ series resistor will limit input current to a safe level with up to $\pm 15\text{V}$ input levels, even if both supply voltages are lost.

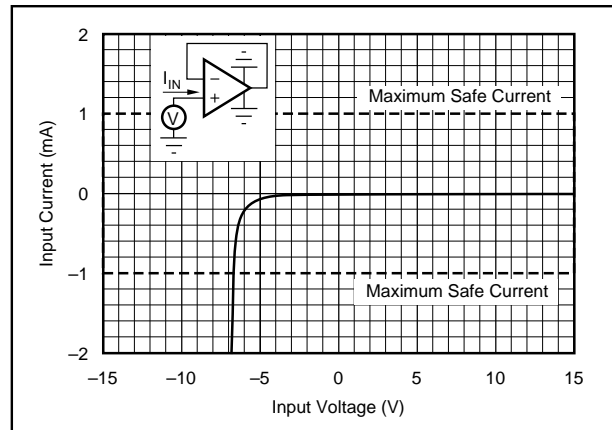


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA111. To avoid leakage problems, it is recommended that the signal input lead of the OPA111 be wired to a Teflon standoff. If the OPA111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A “guard” pattern

should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 (case) should be connected to ground.

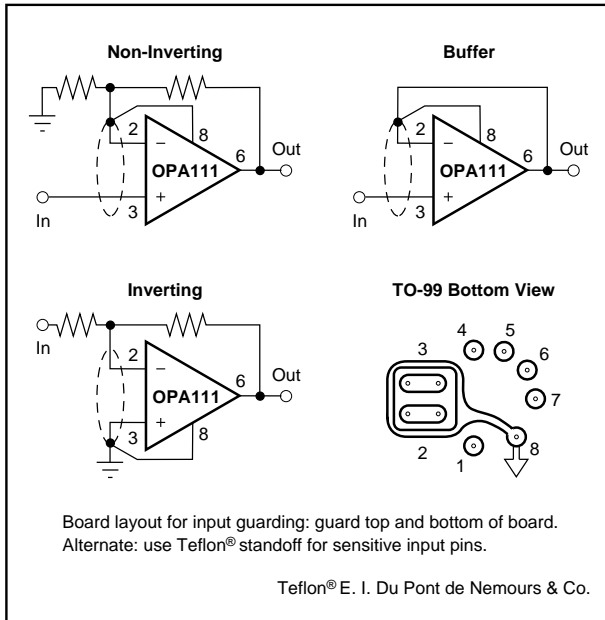


FIGURE 3. Connection of Input Guard.

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 will have a lower total noise than an OP-27 (see Figure 4).

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias current of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 5). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA111 is not compromised by common-mode voltage.

APPLICATIONS CIRCUITS

Figures 6 through 18 are circuit diagrams of various applications for the OPA111.

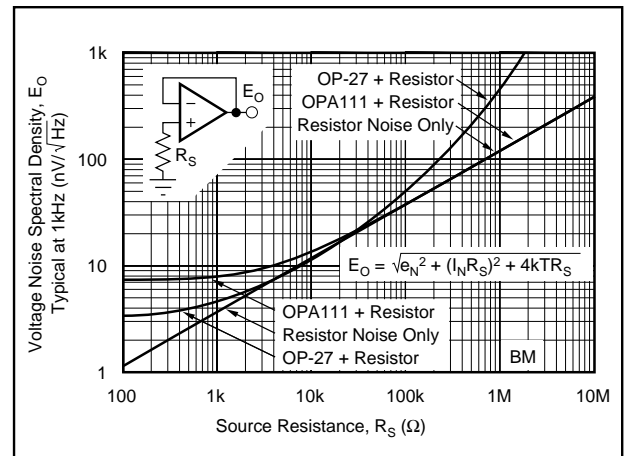


FIGURE 4. Voltage Noise Spectral Density vs Source Resistance.

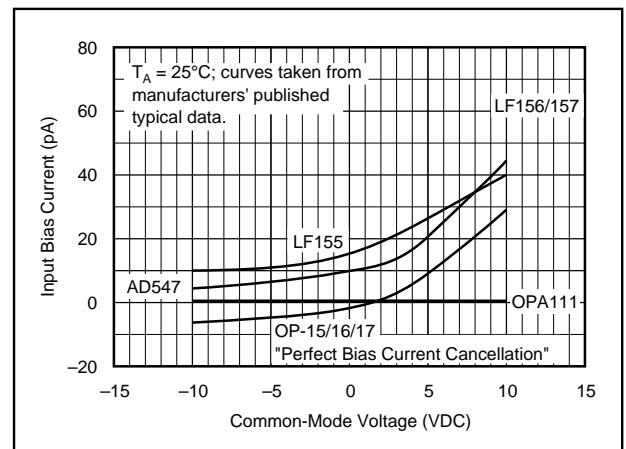


FIGURE 5. Input Bias Current vs Common-Mode Voltage.

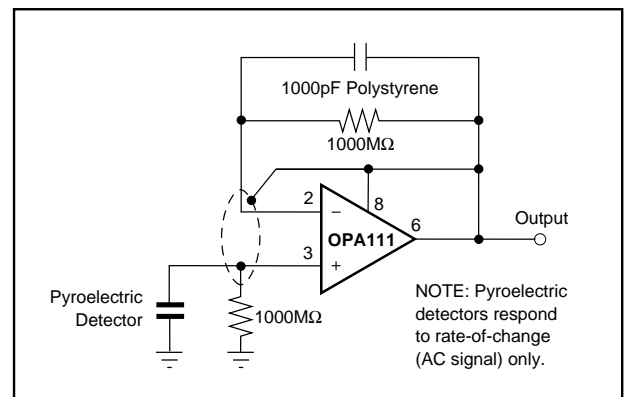


FIGURE 6. Pyroelectric Infrared Detector.

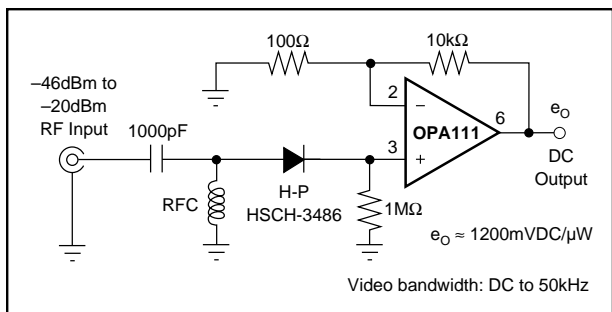


FIGURE 7. Zero-Bias Schottky Diode Square-Law RF Detector.

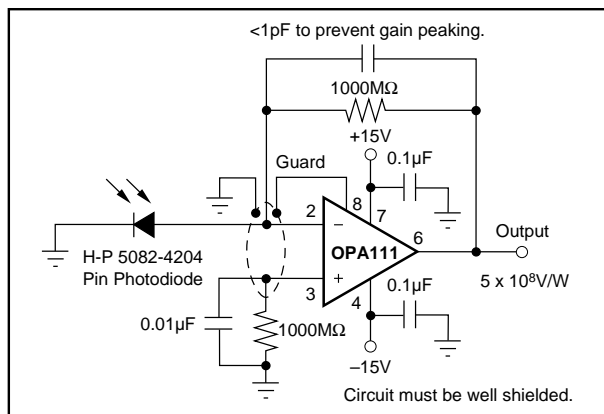


FIGURE 10. Sensitive Photodiode Amplifier.

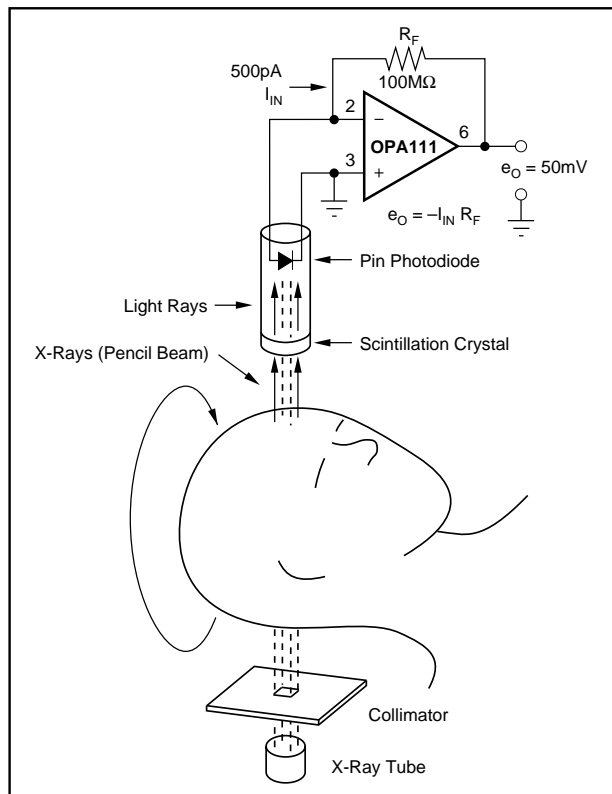


FIGURE 8. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

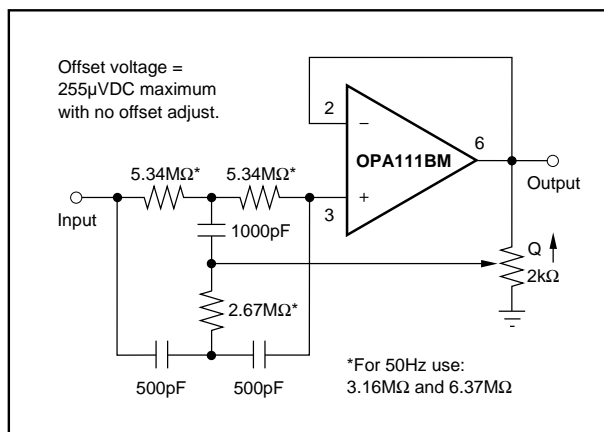


FIGURE 11. 60Hz Reject Filter.

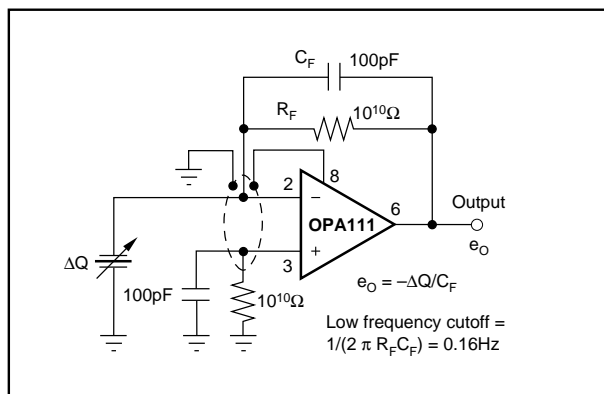


FIGURE 12. Piezoelectric Transducer Charge Amplifier.

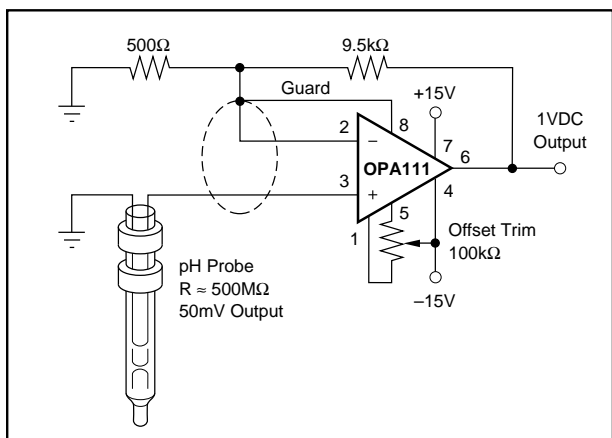


FIGURE 9. High Impedance ($10^{14}\Omega$) Amplifier.

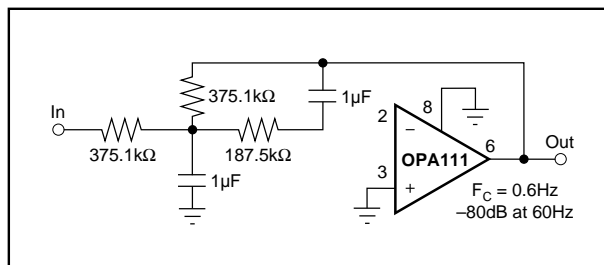


FIGURE 13. 0.6Hz Second-Order Low-Pass Filter.

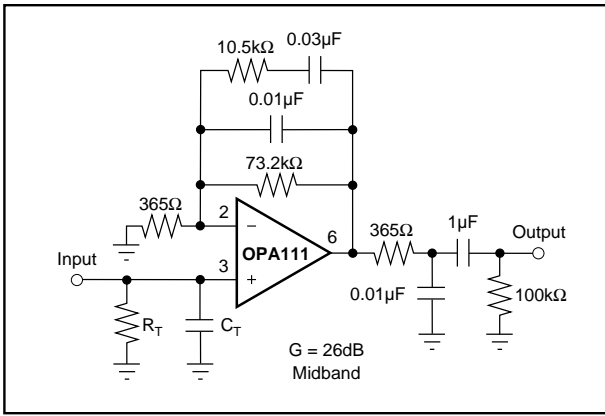


FIGURE 14. RIAA Equalized Phono Preamp.

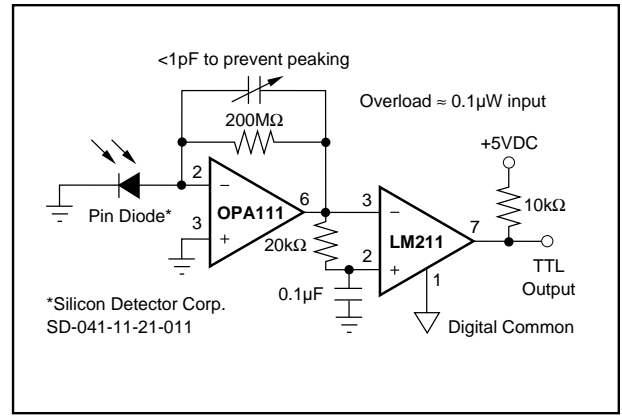


FIGURE 15. High Sensitivity (under 1nW) Fiber Optic Receiver for 9600 Baud Manchester Data.

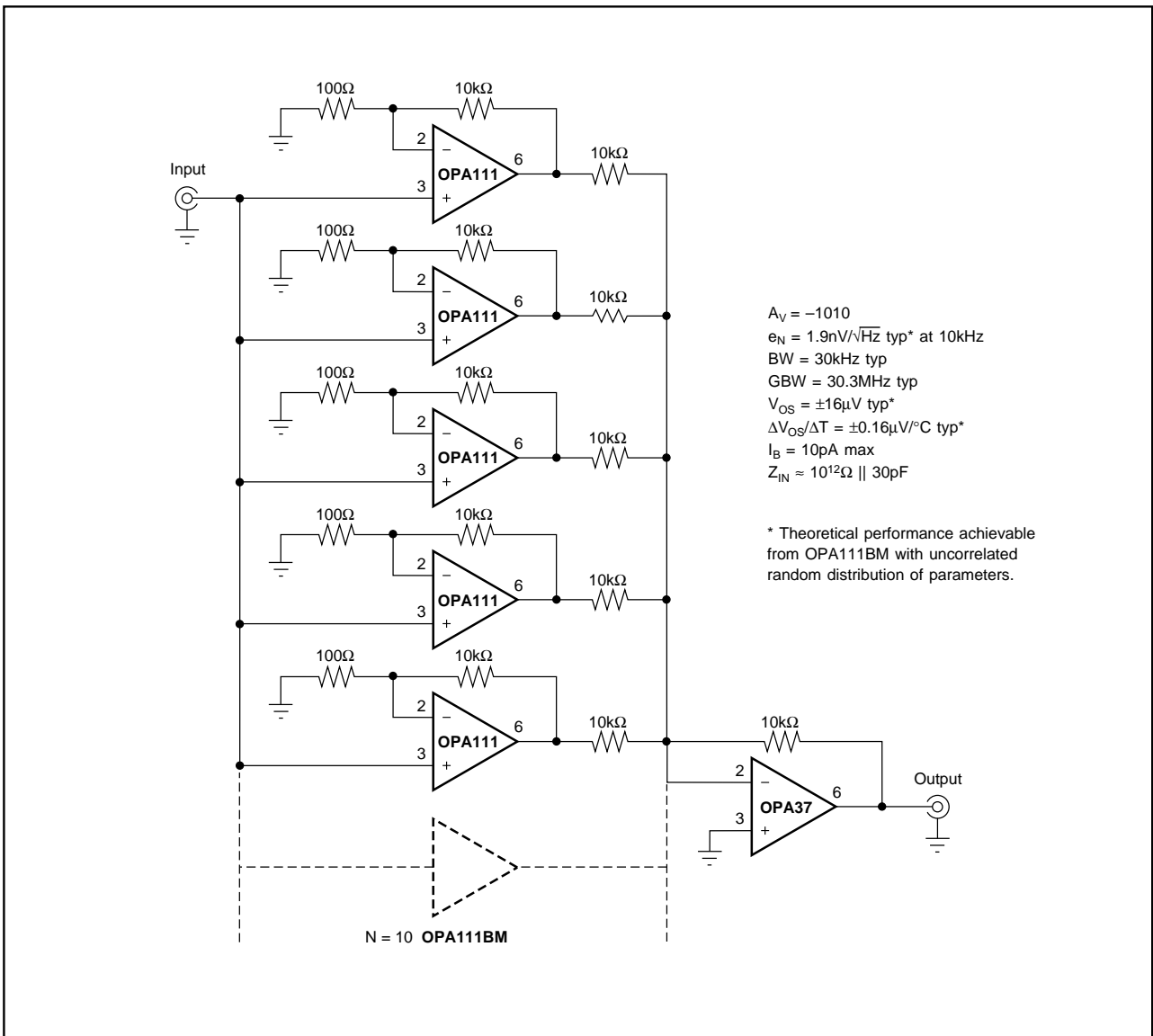


FIGURE 16. 'N' Stage Parallel-Input Amplifier for Reduced Relative Amplifier Noise at the Output.

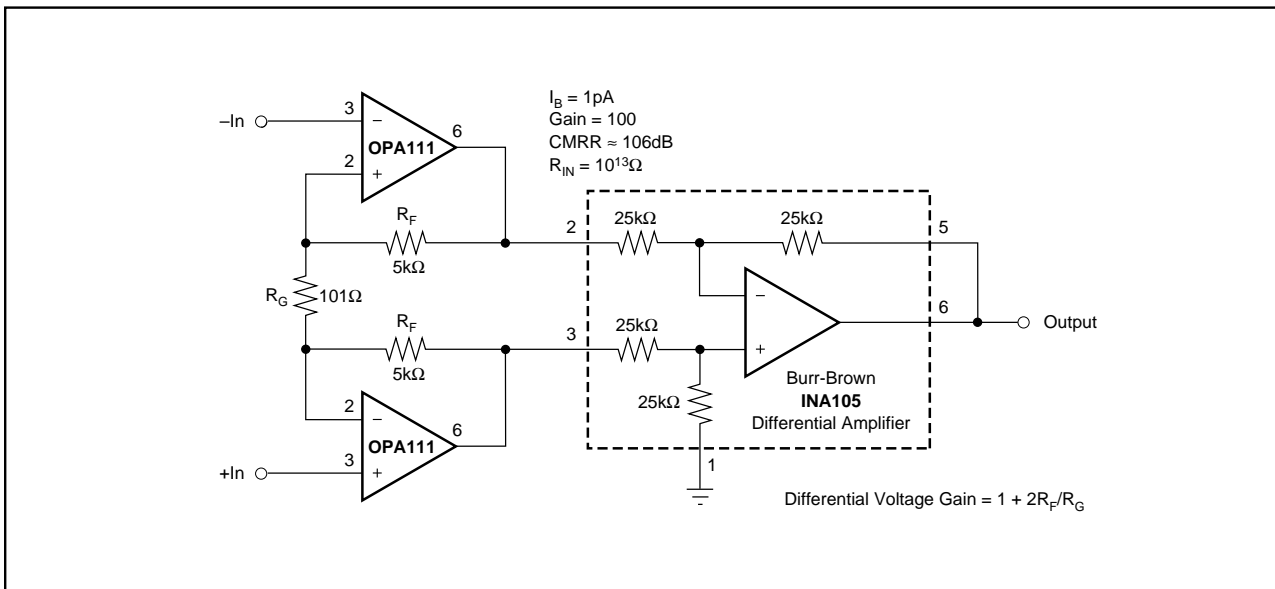


FIGURE 17. FET Input Instrumentation Amplifier.

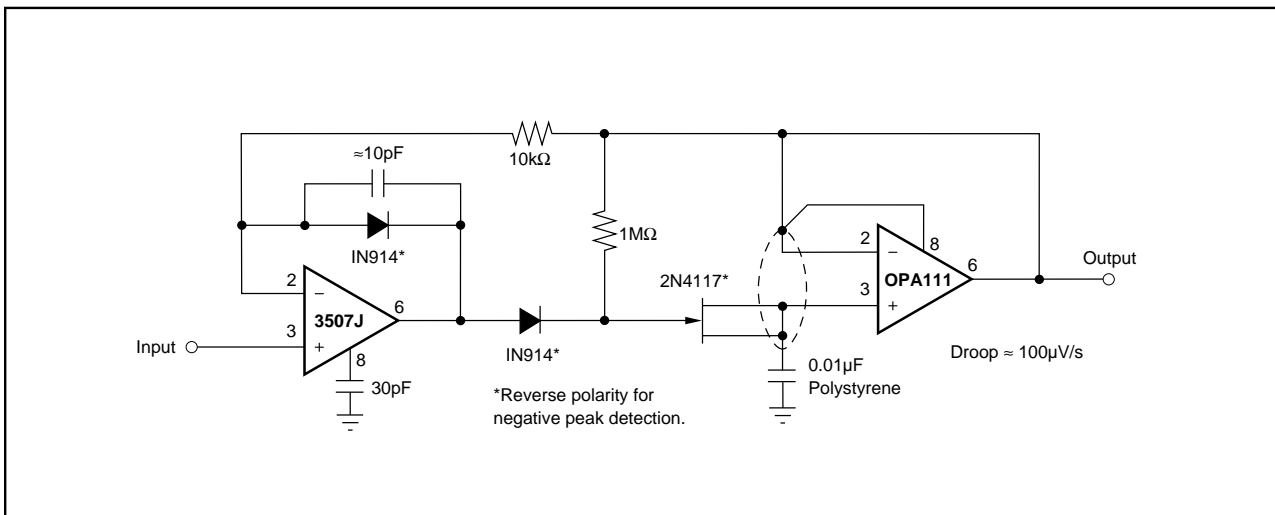


FIGURE 18. Low-Droop Positive Peak Detector.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA111AM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA111BM	NRND	TO-99	LMC	8	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA111SM	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI
OPA111SMQ	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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