MOD5270

Ethernet Core Module

100 Version with RJ-45 | 200 Version with 10-pin header

NetBurner

DATASHEET

Key Points

- Use as a high-performance single board computer or add Ethernet connectivity to a new or existing design
- Customize with a development kit and begin writing application code immediately!
- Industrial temperature range (-40°C to 85°C)

Device Connectivity

- 10/100Mbps Ethernet
- 3 UARTs, I²C, and SPI
- SD/MMC flash card ready
- 47 digital I/Os
- 16-bit address bus and 32-bit data bus with 3 chip selects

Performance and memory

- 32-bit 147.5 MHz Processor
- 8MB SDRAM and 512KB Flash

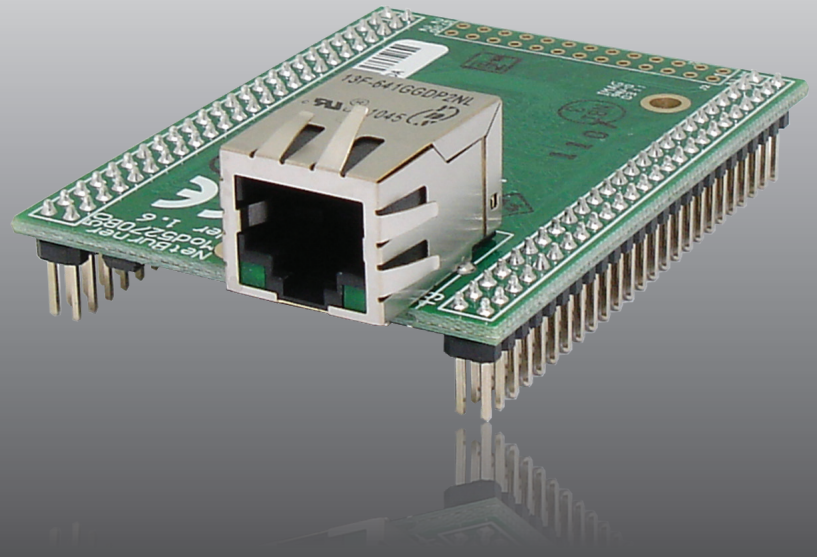
Companion development kit

The following is available with the development kit:

- Customize any aspect of operation including web pages, data filtering, or custom network applications
- Development software: NB Eclipse IDE, Graphical debugger, deployment tools, and examples
- Communication software: TCP/IP stack, HTTP web server, FTP, E-mail, and flash file system
- System software: uC/OS RTOS, ANSI C/C++ compiler and linker

The following optional software modules are not included with kit and are sold separately:

- Embedded SSL & SSH Security Suite (Module License Version)
- SNMP



Specifications

Processor and Memory
32-bit Freescale ColdFire 5270 running at 147.5MHz with 8MB SDRAM, 512KB Flash, and 64Kb SRAM.

Network Interface
10/100 BaseT with RJ-45 connector (100 Version)
10-pin header (200 Version)

Data I/O Interface (J1 and J2)
- Up to 3 UARTs
- Up to 47 digital I/O
- Up to 3 external timer in and up to 4 timer outputs
- Up to 4 external IRQs
- I^2C interface
- SPI interface
- SD/MMC flash card ready
- 16-bit address bus and 32-bit data bus with 3 chip selects

Flash Card Support
FAT32 support for SD Cards up to 8GB (requires exclusive use of SPI signals). Card types include SD/MMC (up to 2GB) and SDHC.

Serial Configurations
The UARTs can be configured in the following way:
- 3 TTL ports
- Add external level shifter for RS-232
- Add external level shifter for RS-422/485 (up to three ports)

Note: UART 0/1/2 also provides RTS/CTS hardware handshaking signals.

LEDs
Link and Speed (100 Version only, on RJ-45)

Physical Characteristics
Dimensions (inches): 2.60” x 2.00”
Weight: 1 oz.
Mounting Holes: 2 x 0.125” dia.

Power
DC Input Voltage: 3.3V @ 380mA typical

Environmental Operating Temperature
-40° to 85° C

RoHS Compliance
The Restriction of Hazardous Substances guidelines ensure that electronics are manufactured with fewer environment harming materials.

Part Numbers

MOD5270 Ethernet Core Module (100 Version, with RJ-45)
Part Number: MOD5270-100IR

MOD5270 Ethernet Core Module (200 Version, with 10-pin header)
Part Number: MOD5270-200IR

MOD5270 LC Development Kit
Part Number: NNDK-MOD5270LC-KIT
Kit includes all the hardware and software you need to customize the included platform hardware. See NetBurner Store product page for package contents. Note: Includes the MOD-DEV-70 development board.

MOD5270 Development Kit
Part Number: NNDK-MOD5270-KIT
Kit includes all the hardware and software you need to customize the included platform hardware. See NetBurner Store product page for package contents. Note: Includes the MOD-DEV-100 development board.

Embedded SSL & SSH Security Suite (Module License Version)
Part Number: NBLIC-SSL-MODULE
Only required if you are using a development kit.

SNMP V1 (Module License Version)
Part Number: NBLIC-SNMP
Available as an option if you are using a development kit.

Ordering Information

E-mail: sales@netburner.com
Online Store: www.NetBurner.com
Telephone: 1-800-695-6828

Pinout and Signal Description

The 200 version board has a 10-pin header instead of an RJ-45 jack. This header enables you to relocate the jack to another location or to add a different jack with power over ethernet (PoE) capabilities to your module. Table 1 provides descriptions of pin function of the 10-pin header.

Table 1: **Pinout and Signal Descriptions for JP2 Header** (1)

Pin	Signal	Description
1	TX-	Transmit -
2	TX+	Transmit +
3	VCC[1]	2.5V
4	RX+	Recieve +
5	RX-	Recieve -
6	VCC[1]	2.5V
7	GND	Ground
8	N/C	Not Connected
9	LED	Link LED
10	LED	Speed LED

Note:
1. Ethernet magnetics center tap voltage provided by NetBurner device

The module has two dual in-line 50 pin headers which enable you to connect to one of our standard NetBurner Carrier Boards, or a board you create on your own. Table 2-3 provides descriptions of pin function of the module header.

Table 2: **Pinout and Signal Descriptions for J1 Connector** (1)

J1 Connector						
Pin	**CPU Pin**	**Function 1**	**Function 2**	**General Purpose I/O**	**Description**	**Max Voltage**
1		GND			Ground	-
2		GND			Ground	-
3		VCC3V			Input Power 3.3 VDC	3.3VDC
4	J13	R/$\overline{W}$			Read / NOT Write[1]	3.3VDC
5	B10	$\overline{CS1}$		PCS1	Chip Select 1[1]	3.3VDC
6	C9	$\overline{CS2}$		PCS2	Chip Select 2[1]	3.3VDC
7	A9	$\overline{CS3}$		PCS3	Chip Select 3[1]	3.3VDC
8	N6	$\overline{OE}$			Output Enable	3.3VDC
9	C6	$\overline{BS2}$	$\overline{CAS2}$		Byte Strobe for D16 to D23 (8 bits)[1] or Column Address Strobe 2[1]	3.3VDC
10	B6	$\overline{BS3}$	$\overline{CAS3}$		Byte Strobe for D24 to D31 (8 bits)[1] or Column Address Strobe 3[1]	3.3VDC
11		$\overline{TIP}$			Transfer in Progress[1,2]	3.3VDC
12	L2	D16			Data Bus - Data 16[4]	3.3VDC
13	H11	$\overline{TA}$		PBUSCTL6	Transfer Acknowledge[1]	3.3VDC
14	K4	D18			Data Bus - Data 18	3.3VDC
15	L1	D17			Data Bus - Data 17	3.3VDC
16	K2	D20			Data Bus - Data 20	3.3VDC
17	K3	D19			Data Bus - Data 19	3.3VDC
18	J4	D22			Data Bus - Data 22	3.3VDC
19	K1	D21			Data Bus - Data 21	3.3VDC
20	J2	D24			Data Bus - Data 24	3.3VDC
21	J3	D23			Data Bus - Data 23	3.3VDC
22	H4	D26			Data Bus - Data 26	3.3VDC
23	J1	D25			Data Bus - Data 25	3.3VDC
24	H2	D28			Data Bus - Data 28	3.3VDC
25	H3	D27			Data Bus - Data 27	3.3VDC

Note:

1. Active low signals, such as $\overline{RESET}$, are indicated with an overbar
2. The TIP signal is the logical AND of *CS1, *CS2 and *CS3. TIP can be used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 - D31.
3. The CLKOUT signal is 1/2 the system frequency of 147.456 MHz.
4. This is the LSB (Least-significant bit). This bit is unused for 16-bit ports
5. This is the MSB (Most-significant bit)
6. Each UART can be clocked from an internal or external source. For external clocks, each UARTn,can be clocked by the corresponding DTn_IN input pin.
7. If using I^2C, pull-up resistors must be added to SDA/SCL.
8. The Mod5270 provides QSPI chip selects QSPI_CS0, QSPI_CS1 & QSPI_CS3.
9. 32-bit mode only

J1 Connector (continued)					
Pin	CPU Pin	Function	General Purpose I/O	Description	Max Voltage
26	G2	D30		Data Bus - Data 30	3.3VDC
27	H1	D29		Data Bus - Data 29[5]	3.3VDC
28	N13	$\overline{\text{RESET}}$		Processor Reset Input[1]	3.3VDC
29	G1	D31		Data Bus - Data 31	3.3VDC
30	P13	$\overline{\text{RSTOUT}}$		Processor Reset Output[1]	3.3VDC
31	K14	CLK_OUT		Buffer Clock Out (CLKOUT-73.728 Mhz)[3]	3.3VDC
32	G13	A0		Data Bus - Address 0[4]	3.3VDC
33	G12	A1		Data Bus - Address 1	3.3VDC
34	G11	A2		Data Bus - Address 2	3.3VDC
35	F14	A3		Data Bus - Address 3	3.3VDC
36	F13	A4		Data Bus - Address 4	3.3VDC
37	F12	A5		Data Bus - Address 5	3.3VDC
38	E14	A6		Data Bus - Address 6	3.3VDC
39	E13	A7		Data Bus - Address 7	3.3VDC
40	E12	A8		Data Bus - Address 8	3.3VDC
41	E11	A9		Data Bus - Address 9	3.3VDC
42	D14	A10		Data Bus - Address 10	3.3VDC
43	D13	A11		Data Bus - Address 11	3.3VDC
44	D12	A12		Data Bus - Address 12	3.3VDC
45	C14	A13		Data Bus - Address 13	3.3VDC
46	C13	A14		Data Bus - Address 14	3.3VDC
47	B14	A15		Data Bus - Address 15[5]	3.3VDC
48		VCC3V		Input Power 3.3 VDC	3.3VDC
49		GND		Ground	-
50		GND		Ground	-

Note:

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7. If using I^2C, pull-up resistors must be added to SDA/SCL.
8. The Mod5270 provides QSPI chip selects QSPI_CS0, QSPI_CS1 & QSPI_CS3.
9. 32-bit mode only

Table 3: **Pinout and Signal Descriptions for J2 Connector** (1)

J2 Connector						
Pin	**CPU Pin**	**Function 1**	**Function 2**	**General Purpose I/O**	**Description**	**Max Voltage**
1		GND			Ground	-
2		VCC3V			Input Power 3.3 VDC	3.3VDC
3	F2	UART0_RX		PUARTL0	UART 0 Receive[6]	3.3VDC
4	F1	UART0_TX		PUARTL1	UART 0 Transmit[6]	3.3VDC
5		NC			No Connect	3.3VDC
6	N1	D14		PDATAH14	Data Bus - Data 14	3.3VDC
7	M2	D13		PDATAH13	Data Bus - Data 13	3.3VDC
8	M1	D15		PDATAH15	Data Bus - Data 15	3.3VDC
9	P2	D11		PDATAH11	Data Bus - Data 11	3.3VDC
10	N2	D12		PDATAH12	Data Bus - Data 12	3.3VDC
11	L3	D10		PDATAH10	Data Bus - Data 10	3.3VDC
12	M3	D9		PDATAH9	Data Bus - Data 9	3.3VDC
13	N3	D8		PDATAH8	Data Bus - Data 8	3.3VDC
14		GND			Ground	-
15	P5	D0		PDATAL0	Data Bus - Data 0	3.3VDC
16	N5	D1		PDATAL1	Data Bus - Data 1	3.3VDC
17	P4	D4		PDATAL4	Data Bus - Data 4	3.3VDC
18	M5	D2		PDATAL2	Data Bus - Data 2	3.3VDC
19	N4	D5		PDATAL5	Data Bus - Data 5	3.3VDC
20	M4	D6		PDATAL6	Data Bus - Data 6	3.3VDC
21	D8	UART1_RX		PUARTL4	UART 1 Receive[6]	3.3VDC
22	D9	UART1_TX		PUARTL5	UART 1 Transmit[6]	3.3VDC
23	L5	D3		PDATAL3	Data Bus - Data 3	3.3VDC
24	P3	D7		PDATAL7	Data Bus - Data 7	3.3VDC
25	C5	SPI_CLK	I2C_SCL	PQSPI2	SPI Clock[8] or I²C Serial Clock[7]	3.3VDC

Note:

1. Active low signals, such as $\overline{\text{RESET}}$, are indicated with an overbar
2. The TIP signal is the logical AND of *CS1, *CS2 and *CS3. TIP can be used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 - D31.
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6. Each UART can be clocked from an internal or external source. For external clocks, each UARTn,can be clocked by the corresponding DTn_IN input pin.
7. If using I²C, pull-up resistors must be added to SDA/SCL.
8. The Mod5270 provides QSPI chip selects QSPI_CS0, QSPI_CS1 & QSPI_CS3.
9. 32-bit mode only

J2 Connector (continued)							
Pin	CPU Pin	Function 1	Function 2	Function 3	General Purpose I/O	Description	Max Voltage
26	G14	T3OUT	UART2_RTS	SPI_CS3	PTIMER6	Timer Output 3 or UART 2 Request To Send[1,6] or SPI Chip Select 3	3.3VDC
27	B5	SPI_DIN	I2C_SDA		PQSPI1	SPI Data In or I²C Serial Data[7]	3.3VDC
28	A5	SPI_DOUT			PQSPI0	SPI Data Out	3.3VDC
29	F3	UART0_CTS			PUARTL3	UART 0 Clear To Send[1,6]	3.3VDC
30	A6	SPI_CS0			PQSPI3	SPI Chip Select 0[8]	3.3VDC
31	E4	T0IN	DREQ0		PTIMER1	Timer Input 0 or DMA Request 0[1]	3.3VDC
32	C8	UART1_RTS	U2_RTS		PUARTL6	UART 1[1,6] or UART 2 Request to Send[1,6]	3.3VDC
33	B8	UART1_CTS	U2_CTS		PUARTL7	UART 1[1,6] or UART 2 Clear to Send[1,6]	3.3VDC
34	M6	T1OUT	DACK1		PTIMER2	Timer Output 1 or DMA Acknowledge 1	3.3VDC
35	M9	T2IN	DREQ2	T2OUT	PTIMER5	Timer Input 2 or DMA Request 2[1] or Timer Output 2	3.3VDC
36	F4	T0OUT	DACK0		PTIMER0	Timer Output 0 or DMA Acknowledge 0	3.3VDC
37	L6	T1IN	DREQ1	T1OUT	PTIMER3	Timer Input 1 or DMA Request 1[1] or Timer Output 1	3.3VDC
38	G3	UART0_RTS			PUARTL2	UART 0 Request To Send[1,6]	3.3VDC
39	J12	I2C_SDA			PFECI2C1	I²C Serial Data[7]	3.3VDC
40	B7	SPI_CS1	SD_CKE		PQSPI4	SPI Chip Select 1[8] or SDRAM Clock Enable	3.3VDC
41	A7	UART2_RX			PUARTH0	UART 2 Receive[6]	3.3VDC
42	J11	I2C_SCL			PFECI2C0	I²C Serial Clock	3.3VDC
43	L8	IRQ1			PIRQ1	External Interrupt 1[1]	3.3VDC
44	A8	UART2_TX			PUARTH1	UART 2 Transmit[6]	3.3VDC
45	N8	IRQ3			PIRQ3	External Interrupt 3[1]	3.3VDC
46		GND				Ground	-
47	L7	IRQ5			PIRQ5	External Interrupt 5[1]	3.3VDC
48	N7	IRQ7			PIRQ7	External Interrupt 7[1]	3.3VDC
49		GND				Ground	-
50		VCC3V				Input power 3.3 VDC	3.3VDC

Note:

1. Active low signals, such as RESET, are indicated with an overbar
2. The TIP signal is the logical AND of *CS1, *CS2 and *CS3. TIP can be used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16 - D31.
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9. 32-bit mode only

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