AMIS-30543

Micro-Stepping Motor Driver

Introduction

The AMIS−30543 is a micro−stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and an SPI interface with an external microcontroller. It has an on−chip voltage regulator, reset−output and watchdog reset, able to supply peripheral devices. AMIS−30543 contains a current−translation table and takes the next micro−step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (=direction) register or input pin. The chip provides a so−called "speed and load angle" output. This allows the creation of stall detection algorithms and control loops based on load−angle to adjust torque and speed. It is using a proprietary PWM algorithm for reliable current control.

The AMIS−30543 is implemented in I2T100 technology, enabling both high−voltage analog circuitry and digital functionality on the same chip. The chip is fully compatible with the automotive voltage requirements.

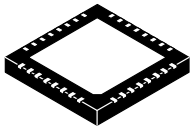
The AMIS−30543 is ideally suited for general−purpose stepper motor applications in the automotive, industrial, medical, and marine environment. With the on−chip voltage regulator it further reduces the BOM for mechatronic stepper applications.

Key Features

- Dual H−Bridge for 2−Phase Stepper Motors
- Programmable Peak−Current Up to 3 A
- On−Chip Current Translator
- SPI Interface
- Speed and Load Angle Output
- Eleven Step Modes from Full Step Up to 128 Micro−Steps
- Fully Integrated Current−Sense
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Active Fly−Back Diodes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 5 V and 3.3 V Microcontrollers
- Integrated 5 V Regulator to Supply External Microcontroller
- Integrated Reset Function to Reset External Microcontroller
- Integrated Watchdog Function
- These Devices are Pb−Free and are RoHS Compliant

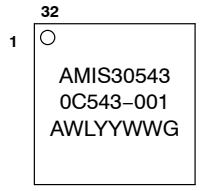
ON Semiconductor®

http://onsemi.com



QFN32
CASE 485J

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 37 of this data sheet.

BLOCK DIAGRAM

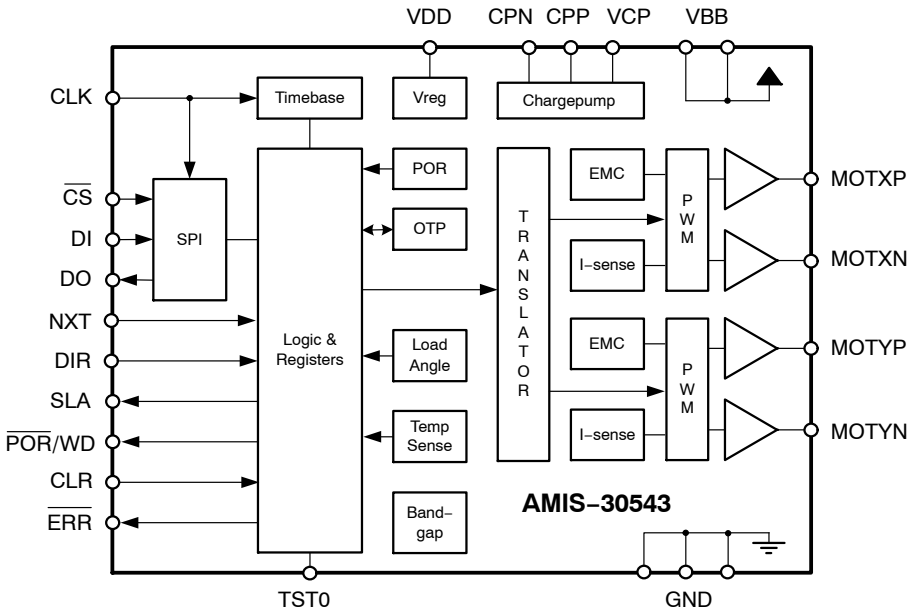


Figure 1. Block Diagram AMIS−30543

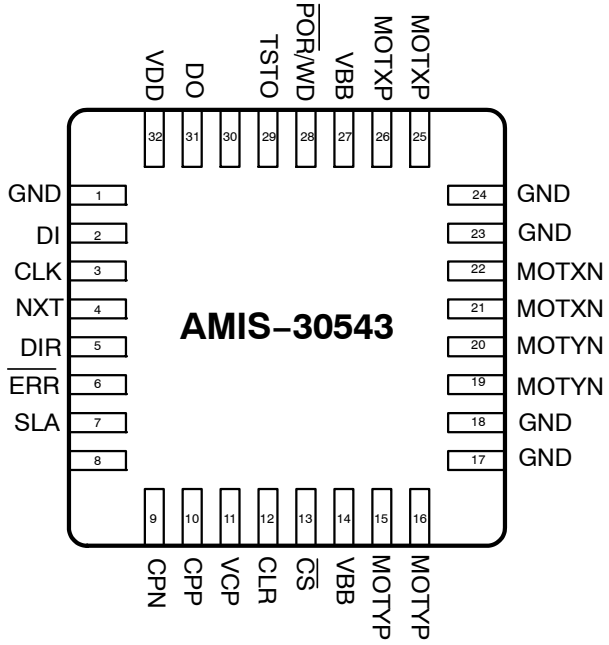


Figure 2. Pin Out AMIS−30543

Table 1. PIN LIST AND DESCRIPTION

Name	Pin	Description	Type	Equivalent Schematic
GND	1	Ground	Supply	
DI	2	SPI Data In	Digital Input	Type 2
CLK	3	SPI Clock Input	Digital Input	Type 2
NXT	4	Next micro−step input	Digital Input	Type 2
DIR	5	Direction input	Digital Input	Type 2
$\overline{ERR}$	6	Error output (open drain)	Digital Output	Type 4
SLA	7	Speed load angle output	Analog Output	Type 5
/	8	No function (to be left open in normal operation)		
CPN	9	Negative connection of charge pump capacitor	High Voltage	
CPP	10	Positive connection of charge pump capacitor	High Voltage	
VCP	11	Charge pump filter−capacitor	High Voltage	
CLR	12	“Clear” = chip reset input	Digital Input	Type 1
$\overline{CS}$	13	SPI chip select input	Digital Input	Type 2
VBB	14	High voltage supply Input	Supply	Type 3
MOTYP	15, 16	Negative end of phase Y coil output	Driver Output	
GND	17, 18	Ground, heat sink	Supply	
MOTYN	19, 20	Positive end of phase Y coil output	Driver Output	
MOTXN	21, 22	Positive end of phase X coil output	Driver Output	
GND	23, 24	Ground, heat sink	Supply	
MOTXP	25, 26	Negative end of phase X coil output	Driver Output	
VBB	27	High voltage supply input	Supply	Type 3
$\overline{POR}$/WD	28	Power−on−reset and watchdog reset output (open drain)	Digital Output	Type 4
TST0	29	Test pin input (to be tied to ground in normal operation)	Digital Input	
/	30	No function (to be left open in normal operation)		
DO	31	SPI data output (open drain)	Digital Output	Type 4
VDD	32	Logic supply output (needs external decoupling capacitor)	Supply	Type 3

Table 2. ABSOLUTE MAXIMUM RATINGS

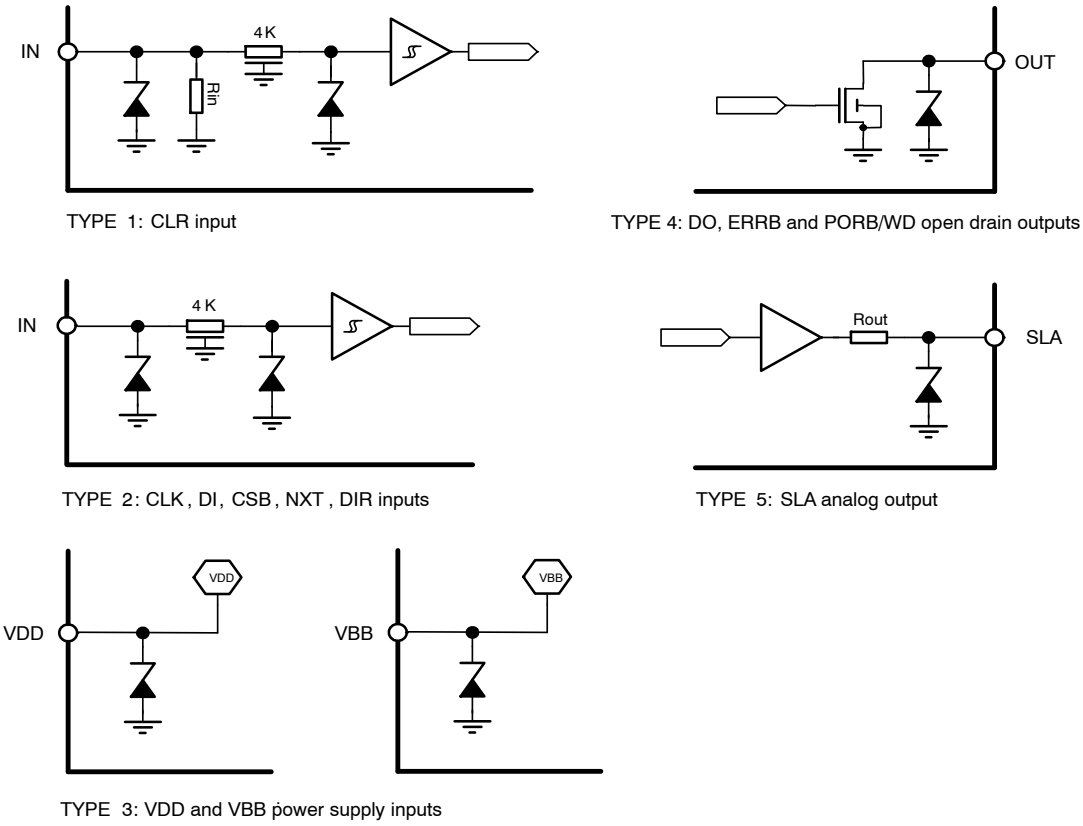
Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC supply voltage (Note 1)	−0.3	+40	V
T_{ST}	Storage temperature	−55	+160	°C
T_J	Junction Temperature under bias (Note 2)	−50	+175	°C
V_{ESD}	Electrostatic discharges on component level, All pins (Note 3)	−2	+2	kV
V_{ESD}	Electrostatic discharges on component level, HiV pins (Note 4)	−8	+8	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For limited time < 0.5 s.
2. Circuit functionality not guaranteed.
3. Human body model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B).
4. HiV = High Voltage Pins MOTxx, V_{BB}, GND; (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B).

EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.



TYPE 1: CLR input

TYPE 4: DO, ERRB and PORB/WD open drain outputs

TYPE 2: CLK, DI, CSB, NXT, DIR inputs

TYPE 5: SLA analog output

TYPE 3: VDD and VBB power supply inputs

Figure 3. In− and Output Equivalent Diagrams

PACKAGE THERMAL CHARACTERISTICS

The AMIS−30543 is available in a NQFP32 package. For cooling optimizations, the NQFP has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer. Figure 4 gives an example for good power distribution solutions.

For precise thermal cooling calculations the major thermal resistances of the device are given in Table 5. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the exposed pad)

The major thermal resistances of the device are the Rth from the junction to the ambient (Rthja) and the overall Rth from the junction to exposed pad (Rthjp). In Table 4 below one can find the values for the Rthja and Rthjp, simulated according to JESD−51.

The Rthja for 2S2P is simulated conform JEDEC JESD−51 as follows:

- A 4−layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1.46 mm (FR4 PCB material)
- The 2 signal layers: 70 μm thick copper with an area of 5500 mm^2 copper and 20% conductivity
- The 2 power internal planes: 36 μm thick copper with an area of 5500 mm^2 copper and 90% conductivity

The Rthja for 1S0P is simulated conform to JEDEC JESD−51 as follows:

- A 1−layer printed circuit board with only 1 layer
- Board thickness is 1.46 mm (FR4 PCB material)
- The layer has a thickness of 70 μm copper with an area of 5500 mm^2 copper and 20% conductivity

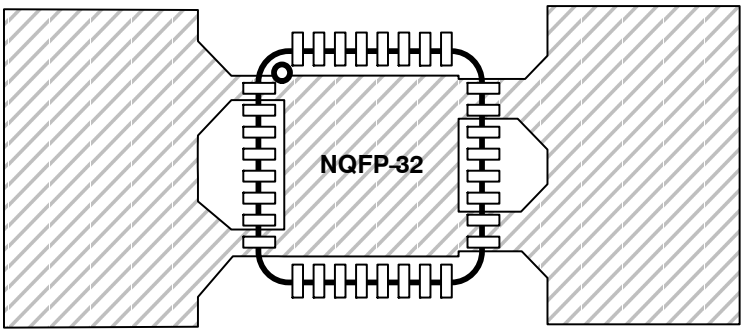


Figure 4. Example of NQFP−32 PCB Ground Plane Layout in Top View (Preferred Layout at Top and Bottom)

ELECTRICAL SPECIFICATION

Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 3. OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC Supply	+6	+30	V
T_J	Junction Temperature (Note 5)	−40	+172	°C

5. No more than 100 cumulative hours in life time above T_{tw}.

Table 4. DC PARAMETERS (The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
SUPPLY AND VOLTAGE REGULATORS							
V_{BB}	V_{BB}	Nominal operating supply range		6		30	V
I_{BB}		Total internal current consumption (Note 6)	Unloaded outputs			12	mA
V_{DD}	V_{DD}	Regulated Output Voltage	I_{LOAD} within limits	4.5	5	5.5	V
V_{DD_SLP}		Regulated Output Voltage in Sleep Mode	$-1\ mA \le I_{LOAD} \le 0\ mA$ $V_{BB} > 9\ V$	4		5.5	V
I_{INT}		Internal load current (Note 6)	Unloaded outputs			8	mA
I_{LOAD}		Max Output Current	$6\ V \le V_{BB} < 8\ V$	15			
			$8\ V \le V_{BB} \le 30\ V$	40			
I_{DDLIM}		Current limitation	Pin shorted to ground			200	mA
I_{LOAD_SLP}		Current Consumption when in Sleep Mode	$V_{BB} > 9\ V$		230		μA
POWER−ON−RESET (POR)							
V_{DDH}	V_{DD}	Internal POR comparator threshold	V_{DD} rising	3.9	4.2	4.4	V
V_{DDL}		Internal POR comparator threshold	V_{DD} falling		3.86		V
V_{DDHYS}		Internal POR comparator hysteresis			0.35		V
MOTORDRIVER							
$I_{MDmax,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation	$T_J = 130°C$		3000		mA
R_{HS}		On−resistance high−side driver, CUR[4:0] = 0...31 (Note 7)			0.15	0.4	Ω
			$T_J = 160°C$			0.45	Ω
R_{LS3}		On−resistance low−side driver, CUR[4:0] = 16...25 (Note 7)			0.1	0.4	Ω
			$T_J = 160°C$			0.45	Ω
R_{LS2}		On−resistance low−side driver, CUR[4:0] = 10...15 (Note 7)			0.2	0.7	Ω
			$T_J = 160°C$			0.8	Ω
R_{LS1}		On−resistance low−side driver, CUR[4:0] = 3...9 (Note 7)			0.4	1.1	Ω
			$T_J = 160°C$			1.25	Ω
R_{LS0}		On−resistance low−side driver, CUR[4:0] = 0...2 (Note 7)			0.8	2.2	Ω
			$T_J = 160°C$			2.50	Ω
DIGITAL INPUTS							
I_{leak}	DI, CLK NXT, DIR CLR, $\overline{CS}$	Input Leakage (Note 8)	$T_J = 160°C$			1	μA
V_{IL}		Logic Low Threshold		0		0.65	V
V_{IH}		Logic High Threshold		2.35		V_{DD}	V
R_{pd_CLR}	CLR	Internal Pulldown Resistor		120	200	300	kΩ
R_{pd_TST}	TST0	Internal Pulldown Resistor		3		9	kΩ

6. Current with oscillator running, all analogue cells active, SPI communication and NXT pulses applied. No floating inputs. Parameter guaranteed by design.
7. Characterization Data Only
8. Not valid for pins with internal Pulldown resistor

Table 4. DC PARAMETERS (The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUTS							
V_{OL}	DO, $\overline{ERR}$, $\overline{POR}$/WD	Logic Low level open drain	I_{OL} = 5 mA			0.5	V
THERMAL WARNING AND SHUTDOWN							
T_{tw}		Thermal Warning		150	160	170	°C
T_{tsd}		Thermal shutdown (Notes 9 and 10)			T_{tw} + 20		°C
CHARGE PUMP							
V_{cp}	VCP	Output voltage	6 V< V_{BB} < 15 V		2 * V_{BB} − 2		V
			15 V < V_{BB} < 30 V	V_{BB} + 9	V_{BB} + 12.5	V_{BB}+16	V
C_{buffer}		External buffer capacitor		180	220	470	nF
C_{pump}	CPP CPN	External pump capacitor		180	220	470	nF
PACKAGE THERMAL RESISTANCE VALUE							
Rth_{ja}	NQFP	Thermal Resistance Junction−to−Ambient	Simulated Conform JEDEC JESD−51, 2S2P		30		K/W
			Simulated Conform JEDEC JESD−51, 1S0P		60		K/W
Rth_{jp}	NQFP	Thermal Resistance Junction−to−Exposed Pad			0.95		K/W
SPEED AND LOAD ANGLE OUTPUT							
V_{out}	SLA	Output Voltage Range		0.2		V_{DD} − 0.2	V
V_{off}		Output Offset SLA pin		−50		50	mV
G_{sla}		Gain of SLA Pin = V_{BEMF} / V_{COIL}	SLAG = 0		0.5		
			SLAG = 1		0.25		
R_{out}		Output Resistance SLA pin				1	kΩ

9. No more than 100 cumulated hours in life time above T_{tw}.
10. Thermal shutdown is derived from thermal warning. Characterization Data Only.

Table 5. AC PARAMETERS (The AC parameters are given for V_{BB} and temperature in their operating ranges)

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
INTERNAL OSCILLATOR							
f_{osc}		Frequency of internal oscillator		3.6	4	4.4	MHz
MOTOR DRIVER							
f_{PWM}	MOTxx	PWM frequency	Frequency depends only on internal oscillator	20.5	22.8	25.1	kHz
		Double PWM frequency		41.0	45.6	50.2	kHz
tb_{rise}	MOTxx	Turn−on voltage slope, 10% to 90%	EMC[1:0] = 00		200		V/μs
			EMC[1:0] = 01		140		V/μs
			EMC[1:0] = 10		70		V/μs
			EMC[1:0] = 11		35		V/μs
tb_{fall}	MOTxx	Turn−off voltage slope, 90% to 10%	EMC[1:0] = 00		200		V/μs
			EMC[1:0] = 01		140		V/μs
			EMC[1:0] = 10		70		V/μs
			EMC[1:0] = 11		35		V/μs
DIGITAL OUTPUTS							
t_{H2L}	$\frac{DO}{\overline{ERR}}$	Output fall−time from V_{inH} to V_{inL}	Capacitive load 400 pF and pullup resistor of 1.5 kΩ			50	ns
CHARGE PUMP							
f_{CP}	CPN CPP	Charge pump frequency			250		kHz
t_{CPU}	MOTxx	Startup time of charge pump (Note 11)	Spec external components			5	ms
CLR FUNCTION							
t_{CLR}	CLR	Hard reset duration time		100			μs
POWER−UP							
t_{PU}	$\overline{POR}$/WD	Powerup time	V_{BB} = 12 V, I_{LOAD} = 50 mA, C_{LOAD} = 220 nF		100		μs
t_{POR}		Reset duration	See Figure 16		100		ms
t_{RF}		Reset filter time	See Figure 16		0.5		μs
WATCHDOG							
t_{WDTO}	$\overline{POR}$/WD	Watchdog time out interval		32		512	ms
t_{WDPR}		Prohibited watchdog acknowledge delay			2		ms
NXT FUNCTION							
t_{NXT_HI}	NXT	NXT Minimum, High Pulse Width	See Figure 5	2			μs
t_{NXT_HI}		NXT Minimum, Low Pulse Width	See Figure 5	2			μs
t_{DIR_SET}		NXT Hold Time, Following Change of DIR	See Figure 5	0.5			μs
t_{DIR_HOLD}		NXT Hold Time, Before Change of DIR	See Figure 5	0.5			μs

11. Guaranteed by design

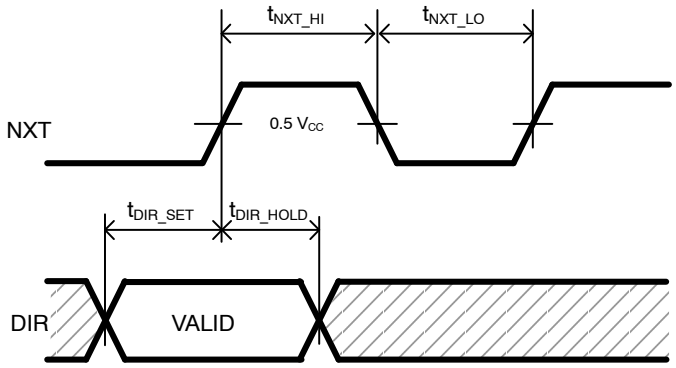


Figure 5. NXT−Input Timing Diagram

Table 6. SPI TIMING PARAMETERS

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}	SPI Clock Period	1			μs
t_{CLK_HIGH}	SPI Clock High Time	100			ns
t_{CLK_LOW}	SPI Clock Low Time	100			ns
t_{SET_DI}	DI Set Up Time, Valid Data Before Rising Edge of CLK	50			ns
t_{HOLD_DI}	DI Hold Time, Hold Data After Rising Edge of CLK	50			ns
t_{CSB_HIGH}	$\overline{CS}$ High Time	2.5			μs
t_{SET_CSB}	$\overline{CS}$ Set Up Time, $\overline{CS}$ Low Before Rising Edge of CLK	100			ns
t_{SET_CLK}	CLK Set Up Time, CLK Low Before Rising Edge of $\overline{CS}$	100			ns

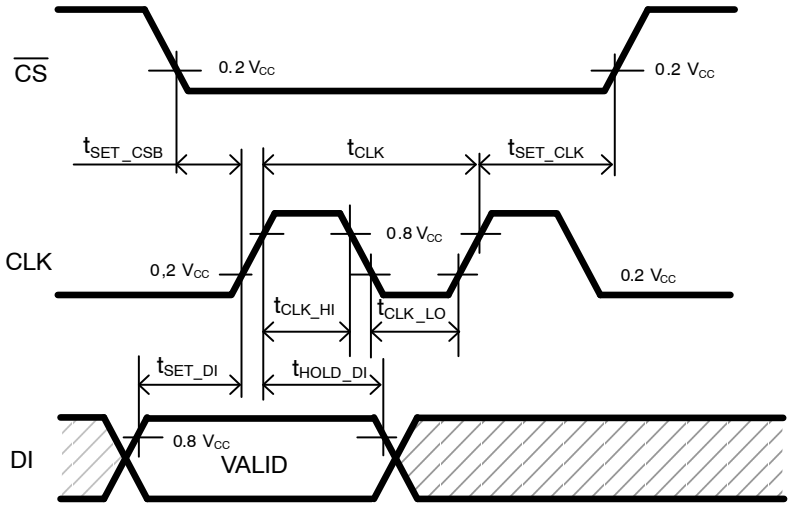


Figure 6. SPI Timing

TYPICAL APPLICATION SCHEMATIC

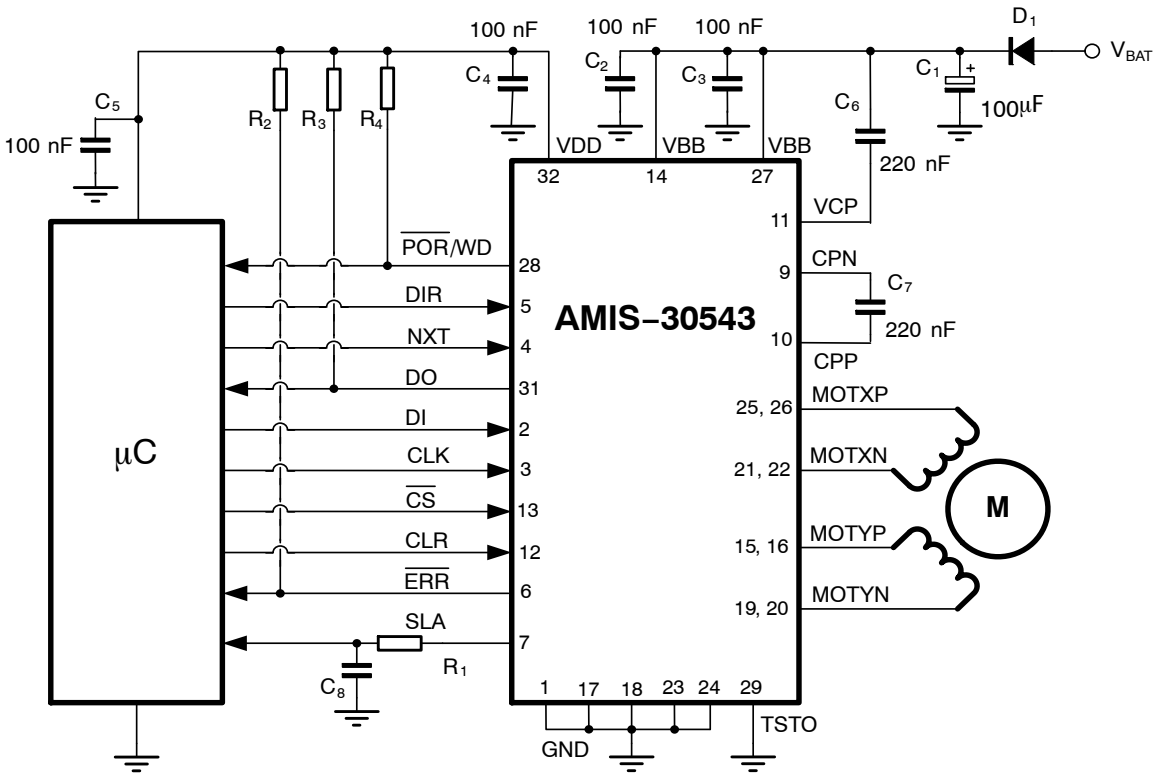


Figure 7. Typical Application Schematic AMIS−30543

Table 7. EXTERNAL COMPONENTS LIST AND DESCRIPTION

Component	Function	Typ Value	Tolerance	Unit
C_1	V_{BB} Buffer Capacitor (Note 12)	100	−20 +80%	μF
C_2, C_3	V_{BB} Decoupling Block Capacitor (Note 13)	100	−20 +80%	nF
C_4	V_{DD} Buffer Capacitor	100	±20%	nF
C_5	V_{DD} Buffer Capacitor	100	±20%	nF
C_6	Charge Pump Buffer Capacitor	220	±20%	nF
C_7	Charge Pump Pumping Capacitor	220	±20%	nF
C_8	Low Pass Filter SLA	1	±20%	nF
R_1	Low Pass Filter SLA	5.6	±1%	kΩ
R_2, R_3, R_4	Pullup Resistor Open Drain Output	4.7	±1%	kΩ
D_1	Optional Reverse Protection Diode	MURD530		

12. ESR < 1 Ω.
13. ESR < 50 mΩ.

FUNCTIONAL DESCRIPTION

H−Bridge Drivers

A full H−bridge is integrated for each of the two stator windings. Each H−bridge consists of two low−side and two high−side N−type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (high−impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H−bridge switches, it is guaranteed that the top− and bottom−switches of the same half−bridge are never conductive simultaneously (interlock delay).

A two−stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate−drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (see Table 12 SPI Control Parameter Overview EMC[1:0]).

The power transistors are equipped with so−called “active diodes”: when a current is forced trough the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain−bulk diode of the transistor.

Depending on the desired current range and the micro−step position at hand, the $R_{DS(on)}$ of the low−side transistors will be adapted such that excellent current−sense accuracy is maintained. The $R_{DS(on)}$ of the high−side transistors remain unchanged; see Table 4 DC Parameters for more details.

PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H−bridge switches. The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock. The frequency of the PWM controller can be doubled and an artificial jitter can be added (see Table 12 SPI Control Parameter Overview PWMJ). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

Automatic Forward and Slow−Fast Decay

The PWM generation is in steady−state using a combination of forward and slow−decay. The absence of fast−decay in this mode, guarantees the lowest possible current−ripple “by design”. For transients to lower current levels, fast−decay is automatically activated to allow high−speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

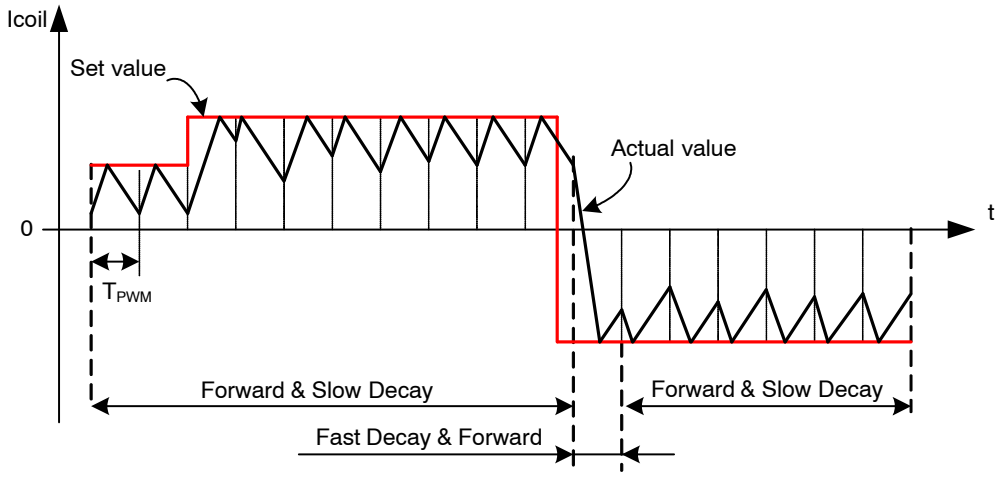


Figure 8. Forward and Slow/Fast Decay PWM

Automatic Duty Cycle Adaptation

In case the supply voltage is lower than 2*Bemf, then the duty cycle of the PWM is adapted automatically to > 50% to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The over−all current−ripple is divided by two if PWM frequency is doubled (see Table 12 SPI Control Parameter Overview PWMF)

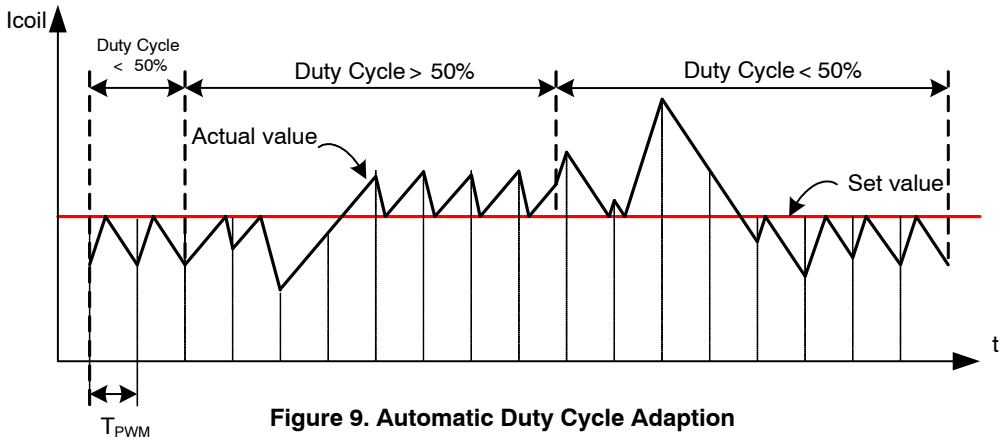


Figure 9. Automatic Duty Cycle Adaption

Step Translator and Step Mode

The step translator provides the control of the motor by means of SM[2:0], ESM[2:0], SPI register DIRCTRL and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of eleven possible stepping modes can be selected through SPI−bits SM[2:0] and ESM[2:0] (see Table 12 SPI Control Parameter Overview). After power−on or hard reset, the coil−current translator is set to the default 1/32 micro−stepping at position '0'. When remaining in the same step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 9 lists the output current vs. the translator position.

As shown in Figure 10 the output current−pairs can be projected approximately on a circle in the (I_x, I_y) plane. There are, however, two exceptions: uncompensated half step and uncompensated full step. In these step modes the currents are not regulated to a fraction of I_{max} but are in all intermediate steps regulated at 100%. In the (I_x, I_y) plane the current−pairs are projected on a square. Table 8 lists the output current vs. the translator position for these cases.

Table 8. SQUARE TRANSLATOR TABLE FOR UNCOMPENSATED FULL STEP AND UNCOMPENSATED HALF STEP

	Stepmode (SM[2:0])		% of I_{max}	
	101	110		
MSP[8:0]	Uncompensated Half Step	Uncompensated Full Step	Coil x	Coil y
0 0000 0000	**0**	–	0	100
0 0100 0000	1	1	100	100
0 1000 0000	2	–	100	0
0 1100 0000	3	2	100	−100
1 0000 0000	4	–	0	−100
1 0100 0000	5	3	−100	−100
1 1000 0000	6	–	−100	0
1 1100 0000	7	0	−100	100

Table 9. CIRCULAR TRANSLATOR TABLE

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
000000000	0	0	0	0	0	0	0		0	0	100
000000001	1									1	100
000000010	2	1								2	100
000000011	3									4	100
000000100	4	2	1							5	100
000000101	5									6	100
000000110	6	3								7	100
000000111	7									9	100
000001000	8	4	2	1						10	100
000001001	9									11	99
000001010	10	5								12	99
000001011	11									13	99
000001100	12	6	3							15	99
000001101	13									16	99
000001110	14	7								17	99
000001111	15									18	98
000010000	16	8	4	2	1					20	98
000010001	17									21	98
000010010	18	9								22	98
000010011	19									23	97
000010100	20	10	5							24	97
000010101	21									25	97
000010110	22	11								27	96
000010111	23									28	96
000011000	24	12	6	3						29	96
000011001	25									30	95
000011010	26	13								31	95
000011011	27									33	95
000011100	28	14	7							34	94
000011101	29									35	94
000011110	30	15								36	93
000011111	31									37	93
000100000	32	16	8	4	2	1				38	92
000100001	33									39	92
000100010	34	17								41	91
000100011	35									42	91
000100100	36	18	9							43	90
000100101	37									44	90
000100110	38	19								45	89
000100111	39									46	89
000101000	40	20	10	5						47	88
000101001	41									48	88
000101010	42	21								49	87

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
000101011	43									50	86
000101100	44	22	11							51	86
000101101	45									52	85
000101110	46	23								53	84
000101111	47									55	84
000110000	48	24	12	6	3					56	83
000110001	49									57	82
000110010	50	25								58	82
000110011	51									59	81
000110100	52	26	13							60	80
000110101	53									61	80
000110110	54	27								62	79
000110111	55									62	78
000111000	56	28	14	7						63	77
000111001	57									64	77
000111010	58	29								65	76
000111011	59									66	75
000111100	60	30	15							67	74
000111101	61									68	73
000111110	62	31								69	72
000111111	63									70	72
001000000	64	32	16	8	4	2	1	0		71	71
001000001	65									72	70
001000010	66	33								72	69
001000011	67									73	68
001000100	68	34	17							74	67
001000101	69									75	66
001000110	70	35								76	65
001000111	71									77	64
001001000	72	36	18	9						77	63
001001001	73									78	62
001001010	74	37								79	62
001001011	75									80	61
001001100	76	38	19							80	60
001001101	77									81	59
001001110	78	39								82	58
001001111	79									82	57
001010000	80	40	20	10	5					83	56
001010001	81									84	55
001010010	82	41								84	53
001010011	83									85	52
001010100	84	42	21							86	51
001010101	85									86	50

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
001010110	86	43								87	49
001010111	87									88	48
001011000	88	44	22	11						88	47
001011001	89									89	46
001011010	90	45								89	45
001011011	91									90	44
001011100	92	46	23							90	43
001011101	93									91	42
001011110	94	47								91	41
001011111	95									92	39
001100000	96	48	24	12	6	3				92	38
001100001	97									93	37
001100010	98	49								93	36
001100011	99									94	35
001100100	100	50	25							94	34
001100101	101									95	33
001100110	102	51								95	31
001100111	103									95	30
001101000	104	52	26	13						96	29
001101001	105									96	28
001101010	106	53								96	27
001101011	107									97	25
001101100	108	54	27							97	24
001101101	109									97	23
001101110	110	55								98	22
001101111	111									98	21
001110000	112	56	28	14	7					98	20
001110001	113									98	18
001110010	114	57								99	17
001110011	115									99	16
001110100	116	58	29							99	15
001110101	117									99	13
001110110	118	59								99	12
001110111	119									99	11
001111000	120	60	30	15						100	10
001111001	121									100	9
001111010	122	61								100	7
001111011	123									100	6
001111100	124	62	31							100	5
001111101	125									100	4
001111110	126	63								100	2
001111111	127									100	1
010000000	128	64	32	16	8	4	2		1	100	0

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
010000001	129									100	−1
010000010	130	65								100	−2
010000011	131									100	−4
010000100	132	66	33							100	−5
010000101	133									100	−6
010000110	134	67								100	−7
010000111	135									100	−9
010001000	136	68	34	17						100	−10
010001001	137									99	−11
010001010	138	69								99	−12
010001011	139									99	−13
010001100	140	70	35							99	−15
010001101	141									99	−16
010001110	142	71								99	−17
010001111	143									98	−18
010010000	144	72	36	18	9					98	−20
010010001	145									98	−21
010010010	146	73								98	−22
010010011	147									97	−23
010010100	148	74	37							97	−24
010010101	149									97	−25
010010110	150	75								96	−27
010010111	151									96	−28
010011000	152	76	38	19						96	−29
010011001	153									95	−30
010011010	154	77								95	−31
010011011	155									95	−33
010011100	156	78	39							94	−34
010011101	157									94	−35
010011110	158	79								93	−36
010011111	159									93	−37
010100000	160	80	40	20	10	5				92	−38
010100001	161									92	−39
010100010	162	81								91	−41
010100011	163									91	−42
010100100	164	82	41							90	−43
010100101	165									90	−44
010100110	166	83								89	−45
010100111	167									89	−46
010101000	168	84	42	21						88	−47
010101001	169									88	−48
010101010	170	85								87	−49
010101011	171									86	−50

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
010101100	172	86	43							86	−51
010101101	173									85	−52
010101110	174	87								84	−53
010101111	175									84	−55
010110000	176	88	44	22	11					83	−56
010110001	177									82	−57
010110010	178	89								82	−58
010110011	179									81	−59
010110100	180	90	45							80	−60
010110101	181									80	−61
010110110	182	91								79	−62
010110111	183									78	−62
010111000	184	92	46	23						77	−63
010111001	185									77	−64
010111010	186	93								76	−65
010111011	187									75	−66
010111100	188	94	47							74	−67
010111101	189									73	−68
010111110	190	95								72	−69
010111111	191									72	−70
011000000	192	96	48	24	12	6	3	1		71	−71
011000001	193									70	−72
011000010	194	97								69	−72
011000011	195									68	−73
011000100	196	98	49							67	−74
011000101	197									66	−75
011000110	198	99								65	−76
011000111	199									64	−77
011001000	200	100	50	25						63	−77
011001001	201									62	−78
011001010	202	101								62	−79
011001011	203									61	−80
011001100	204	102	51							60	−80
011001101	205									59	−81
011001110	206	103								58	−82
011001111	207									57	−82
011010000	208	104	52	26	13					56	−83
011010001	209									55	−84
011010010	210	105								53	−84
011010011	211									52	−85
011010100	212	106	53							51	−86
011010101	213									50	−86
011010110	214	107								49	−87

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
011010111	215									48	−88
011011000	216	108	54	27						47	−88
011011001	217									46	−89
011011010	218	109								45	−89
011011011	219									44	−90
011011100	220	110	55							43	−90
011011101	221									42	−91
011011110	222	111								41	−91
011011111	223									39	−92
011100000	224	112	56	28	14	7				38	−92
011100001	225									37	−93
011100010	226	113								36	−93
011100011	227									35	−94
011100100	228	114	57							34	−94
011100101	229									33	−95
011100110	230	115								31	−95
011100111	231									30	−95
011101000	232	116	58	29						29	−96
011101001	233									28	−96
011101010	234	117								27	−96
011101011	235									25	−97
011101100	236	118	59							24	−97
011101101	237									23	−97
011101110	238	119								22	−98
011101111	239									21	−98
011110000	240	120	60	30	15					20	−98
011110001	241									18	−98
011110010	242	121								17	−99
011110011	243									16	−99
011110100	244	122	61							15	−99
011110101	245									13	−99
011110110	246	123								12	−99
011110111	247									11	−99
011111000	248	124	62	31						10	−100
011111001	249									9	−100
011111010	250	125								7	−100
011111011	251									6	−100
011111100	252	126	63							5	−100
011111101	253									4	−100
011111110	254	127								2	−100
011111111	255									1	−100
100000000	256	128	64	32	16	8	4		2	0	−100
100000001	257									−1	−100

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
100000010	258	129								−2	−100
100000011	259									−4	−100
100000100	260	130	65							−5	−100
100000101	261									−6	−100
100000110	262	131								−7	−100
100000111	263									−9	−100
100001000	264	132	66	33						−10	−100
100001001	265									−11	−99
100001010	266	133								−12	−99
100001011	267									−13	−99
100001100	268	134	67							−15	−99
100001101	269									−16	−99
100001110	270	135								−17	−99
100001111	271									−18	−98
100010000	272	136	68	34	17					−20	−98
100010001	273									−21	−98
100010010	274	137								−22	−98
100010011	275									−23	−97
100010100	276	138	69							−24	−97
100010101	277									−25	−97
100010110	278	139								−27	−96
100010111	279									−28	−96
100011000	280	140	70	35						−29	−96
100011001	281									−30	−95
100011010	282	141								−31	−95
100011011	283									−33	−95
100011100	284	142	71							−34	−94
100011101	285									−35	−94
100011110	286	143								−36	−93
100011111	287									−37	−93
100100000	288	144	72	36	18	9				−38	−92
100100001	289									−39	−92
100100010	290	145								−41	−91
100100011	291									−42	−91
100100100	292	146	73							−43	−90
100100101	293									−44	−90
100100110	294	147								−45	−89
100100111	295									−46	−89
100101000	296	148	74	37						−47	−88
100101001	297									−48	−88
100101010	298	149								−49	−87
100101011	299									−50	−86
100101100	300	150	75							−51	−86

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
100101101	301									−52	−85
100101110	302	151								−53	−84
100101111	303									−55	−84
100110000	304	152	76	38	19					−56	−83
100110001	305									−57	−82
100110010	306	153								−58	−82
100110011	307									−59	−81
100110100	308	154	77							−60	−80
100110101	309									−61	−80
100110110	310	155								−62	−79
100110111	311									−62	−78
100111000	312	156	78	39						−63	−77
100111001	313									−64	−77
100111010	314	157								−65	−76
100111011	315									−66	−75
100111100	316	158	79							−67	−74
100111101	317									−68	−73
100111110	318	159								−69	−72
100111111	319									−70	−72
101000000	320	160	80	40	20	10	5	2		−71	−71
101000001	321									−72	−70
101000010	322	161								−72	−69
101000011	323									−73	−68
101000100	324	162	81							−74	−67
101000101	325									−75	−66
101000110	326	163								−76	−65
101000111	327									−77	−64
101001000	328	164	82	41						−77	−63
101001001	329									−78	−62
101001010	330	165								−79	−62
101001011	331									−80	−61
101001100	332	166	83							−80	−60
101001101	333									−81	−59
101001110	334	167								−82	−58
101001111	335									−82	−57
101010000	336	168	84	42	21					−83	−56
101010001	337									−84	−55
101010010	338	169								−84	−53
101010011	339									−85	−52
101010100	340	170	85							−86	−51
101010101	341									−86	−50
101010110	342	171								−87	−49
101010111	343									−88	−48

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
101011000	344	172	86	43						−88	−47
101011001	345									−89	−46
101011010	346	173								−89	−45
101011011	347									−90	−44
101011100	348	174	87							−90	−43
101011101	349									−91	−42
101011110	350	175								−91	−41
101011111	351									−92	−39
101100000	352	176	88	44	22	11				−92	−38
101100001	353									−93	−37
101100010	354	177								−93	−36
101100011	355									−94	−35
101100100	356	178	89							−94	−34
101100101	357									−95	−33
101100110	358	179								−95	−31
101100111	359									−95	−30
101101000	360	180	90	45						−96	−29
101101001	361									−96	−28
101101010	362	181								−96	−27
101101011	363									−97	−25
101101100	364	182	91							−97	−24
101101101	365									−97	−23
101101110	366	183								−98	−22
101101111	367									−98	−21
101110000	368	184	92	46	23					−98	−20
101110001	369									−98	−18
101110010	370	185								−99	−17
101110011	371									−99	−16
101110100	372	186	93							−99	−15
101110101	373									−99	−13
101110110	374	187								−99	−12
101110111	375									−99	−11
101111000	376	188	94	47						−100	−10
101111001	377									−100	−9
101111010	378	189								−100	−7
101111011	379									−100	−6
101111100	380	190	95							−100	−5
101111101	381									−100	−4
101111110	382	191								−100	−2
101111111	383									−100	−1
110000000	384	192	96	48	24	12	6		3	−100	0
110000001	385									−100	1
110000010	386	193								−100	2

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
110000011	387									−100	4
110000100	388	194	97							−100	5
110000101	389									−100	6
110000110	390	195								−100	7
110000111	391									−100	9
110001000	392	196	98	49						−100	10
110001001	393									−99	11
110001010	394	197								−99	12
110001011	395									−99	13
110001100	396	198	99							−99	15
110001101	397									−99	16
110001110	398	199								−99	17
110001111	399									−98	18
110010000	400	200	100	50	25					−98	20
110010001	401									−98	21
110010010	402	201								−98	22
110010011	403									−97	23
110010100	404	202	101							−97	24
110010101	405									−97	25
110010110	406	203								−96	27
110010111	407									−96	28
110011000	408	204	102	51						−96	29
110011001	409									−95	30
110011010	410	205								−95	31
110011011	411									−95	33
110011100	412	206	103							−94	34
110011101	413									−94	35
110011110	414	207								−93	36
110011111	415									−93	37
110100000	416	208	104	52	26	13				−92	38
110100001	417									−92	39
110100010	418	209								−91	41
110100011	419									−91	42
110100100	420	210	105							−90	43
110100101	421									−90	44
110100110	422	211								−89	45
110100111	423									−89	46
110101000	424	212	106	53						−88	47
110101001	425									−88	48
110101010	426	213								−87	49
110101011	427									−86	50
110101100	428	214	107							−86	51
110101101	429									−85	52

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
110101110	430	215								−84	53
110101111	431									−84	55
110110000	432	216	108	54	27					−83	56
110110001	433									−82	57
110110010	434	217								−82	58
110110011	435									−81	59
110110100	436	218	109							−80	60
110110101	437									−80	61
110110110	438	219								−79	62
110110111	439									−78	62
110111000	440	220	110	55						−77	63
110111001	441									−77	64
110111010	442	221								−76	65
110111011	443									−75	66
110111100	444	222	111							−74	67
110111101	445									−73	68
110111110	446	223								−72	69
110111111	447									−72	70
111000000	448	224	112	56	28	14	7	3		−71	71
111000001	449									−70	72
111000010	450	225								−69	72
111000011	451									−68	73
111000100	452	226	113							−67	74
111000101	453									−66	75
111000110	454	227								−65	76
111000111	455									−64	77
111001000	456	228	114	57						−63	77
111001001	457									−62	78
111001010	458	229								−62	79
111001011	459									−61	80
111001100	460	230	115							−60	80
111001101	461									−59	81
111001110	462	231								−58	82
111001111	463									−57	82
111010000	464	232	116	58	29					−56	83
111010001	465									−55	84
111010010	466	233								−53	84
111010011	467									−52	85
111010100	468	234	117							−51	86
111010101	469									−50	86
111010110	470	235								−49	87
111010111	471									−48	88
111011000	472	236	118	59						−47	88

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
111011001	473									−46	89
111011010	474	237								−45	89
111011011	475									−44	90
111011100	476	238	119							−43	90
111011101	477									−42	91
111011110	478	239								−41	91
111011111	479									−39	92
111100000	480	240	120	60	30	15				−38	92
111100001	481									−37	93
111100010	482	241								−36	93
111100011	483									−35	94
111100100	484	242	121							−34	94
111100101	485									−33	95
111100110	486	243								−31	95
111100111	487									−30	95
111101000	488	244	122	61						−29	96
111101001	489									−28	96
111101010	490	245								−27	96
111101011	491									−25	97
111101100	492	246	123							−24	97
111101101	493									−23	97
111101110	494	247								−22	98
111101111	495									−21	98
111110000	496	248	124	62	31					−20	98
111110001	497									−18	98
111110010	498	249								−17	99
111110011	499									−16	99
111110100	500	250	125							−15	99
111110101	501									−13	99
111110110	502	251								−12	99
111110111	503									−11	99
111111000	504	252	126	63						−10	100
111111001	505									−9	100
111111010	506	253								−7	100
111111011	507									−6	100
111111100	508	254	127							−5	100
111111101	509									−4	100
111111110	510	255								−2	100
111111111	511									−1	100

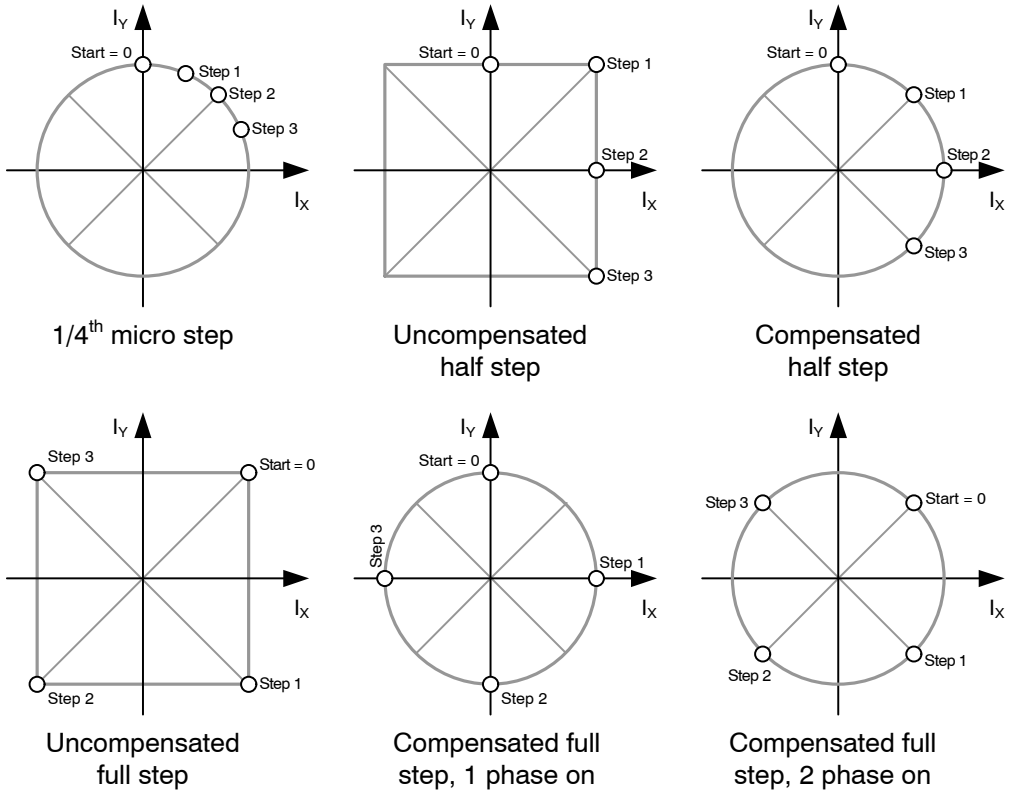


Figure 10. Translator Table: Circular and Square

Direction

The direction of rotation is selected by means of following combination of the DIR input pin and the SPI−controlled direction bit <DIRCTRL>. (see Table 12 SPI Control Parameter Overview)

NXT Input

Changes on the NXT input will move the motor current one step up/down in the translator table (even when the motor is disabled: <MOTEN> = 0). Depending on the NXT−polarity bit <NXTP> (see Table 12 SPI Control Parameter Overview), the next step is initiated either on the rising edge or the falling edge of the NXT input.

Translator Position

The translator position MSP[8:0] can be read in SPI Status Register 3 and Status Register 4 (See Table 14 SR3 and SR4). This is a 9−bit number equivalent to the 1/128th micro−step (see Table 9 “Circular Translator Table”). The translator position is updated immediately following a NXT trigger.

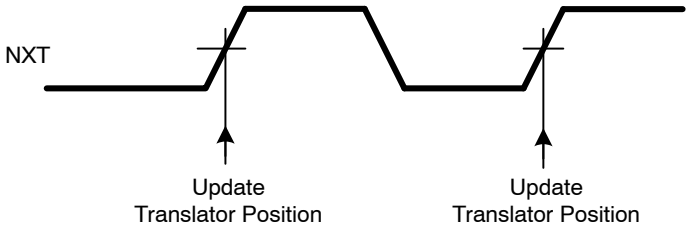


Figure 11. Translator Position Timing Diagram

Synchronization of Step Mode and NXT Input

When step mode is re−programmed to another resolution (Figure 12), then this is put in effect immediately upon the first arriving “NXT” input. If the micro−stepping resolution is increased, the coil currents will be regulated to the nearest micro−step, according to the fixed grid of the increased resolution. If however the micro−stepping resolution is decreased, then it is possible to introduce an offset (or phase shift) in the micro−step translator table.

If the step resolution is decreased at a translator table position that is shared both by the old and new resolution setting, then the offset is zero and micro−stepping is proceeds according to the translator table.

If the translator position is **not** shared both by the old and new resolution setting, then the micro−stepping proceeds with an offset relative to the translator table (See Figure 12 right hand side).

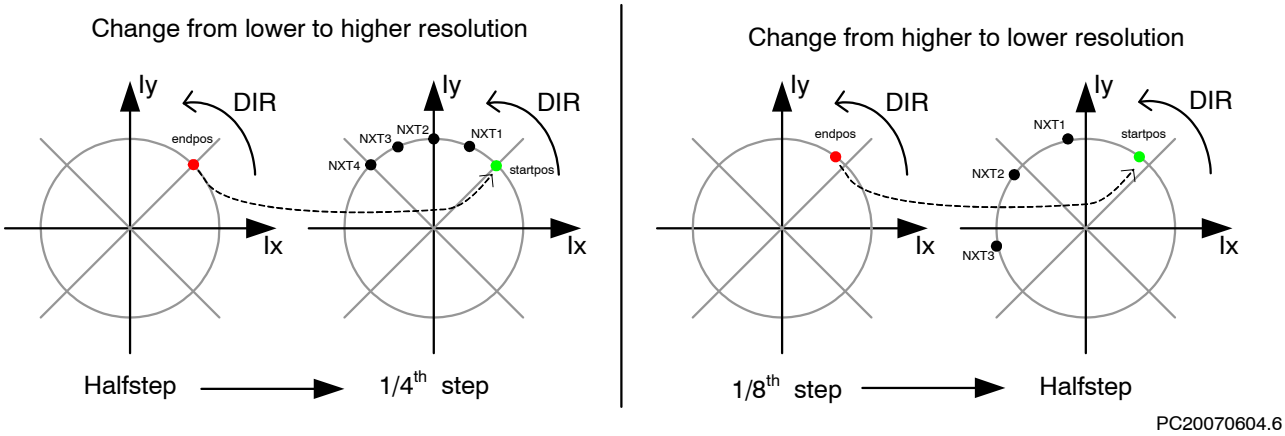


Figure 12. NXT−Step Mode Synchronization

Left: Change from lower to higher resolution. The left−hand side depicts the ending half−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the micro−step position.
Right: Change from higher to lower resolution. The left−hand side depicts the ending micro−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the half−step position.
Note: It is advised to reduce the micro−stepping resolution only at micro−step positions that overlap with desired micro−step positions of the new resolution.

Programmable Peak−Current

The amplitude of the current waveform in the motor coils (coil peak current = I_{max}) is adjusted by means of an SPI parameter "CUR[4:0]" (see Table 12 SPI Control Parameter Overview). Whenever this parameter is changed, the coil−currents will be updated immediately at the next PWM period. Figure 13 presents the Peak−Current and Current Ratings in conjunction to the Current setting CUR[4:0].

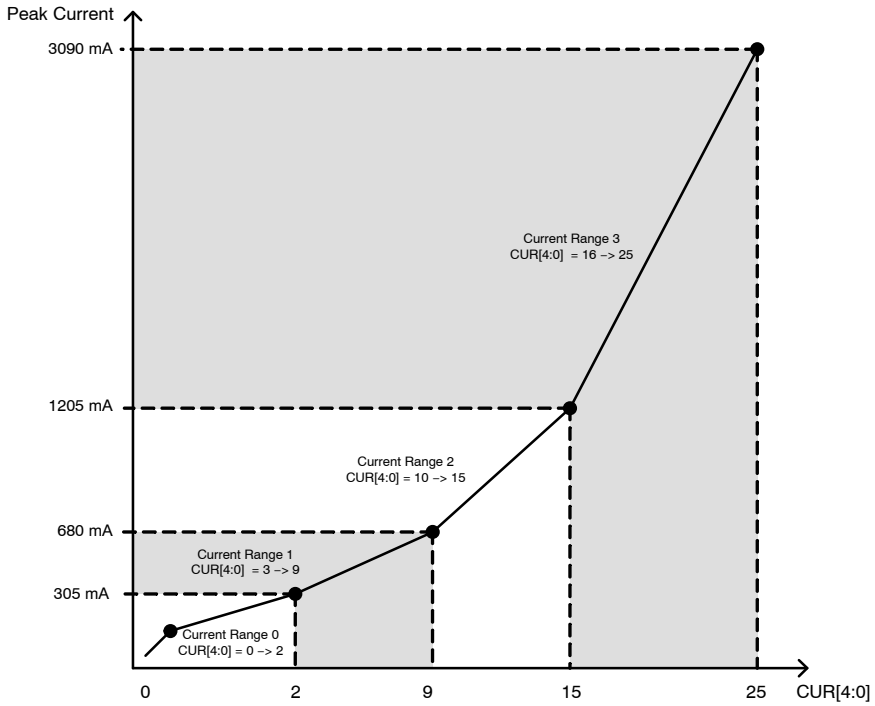


Figure 13. Programmable Peak−Current Overview

Speed and Load Angle Output

The SLA−pin provides an output voltage that indicates the level of the Back−e.m.f. voltage of the motor. This Back−e.m.f. voltage is sampled during every so−called ”coil current zero crossings”. Per coil, two zero−current positions exist per electrical period, yielding in total four zero−current observation points per electrical period.

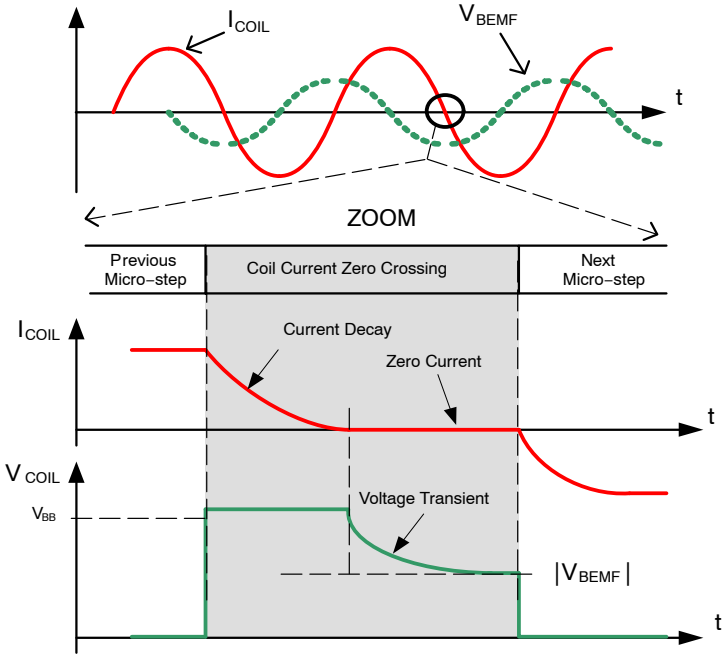


Figure 14. Principle of Bemf Measurement

Because of the relatively high recirculation currents in the coil during current decay, the coil voltage V_{COIL} shows a transient behavior. As this transient is not always desired in application software, two operating modes can be selected by means of the bit <SLAT> (see “SLA−transparency” in Table 12 SPI Control Parameter Overview). The SLA pin shows in “transparent mode” full visibility of the voltage transient behavior. This allows a sanity−check of the speed−setting versus motor operation and characteristics and supply voltage levels. If the bit “SLAT” is cleared, then only the voltage samples at the end of each coil current zero crossing are visible on the SLA−pin. Because the transient behavior of the coil voltage is not visible anymore, this mode generates smoother Back e.m.f. input for post−processing, e.g. by software.

In order to bring the sampled Back e.m.f. to a descent output level (0 V to 5 V), the sampled coil voltage V_{COIL} is divided by 2 or by 4. This divider is set through an SPI bit <SLAG>. (see Table 12 SPI Control Parameter Overview)

The following drawing illustrates the operation of the SLA−pin and the transparency−bit. “PWMsh” and “I_{COIL} = 0” are internal signals that define together with SLAT the sampling and hold moments of the coil voltage.

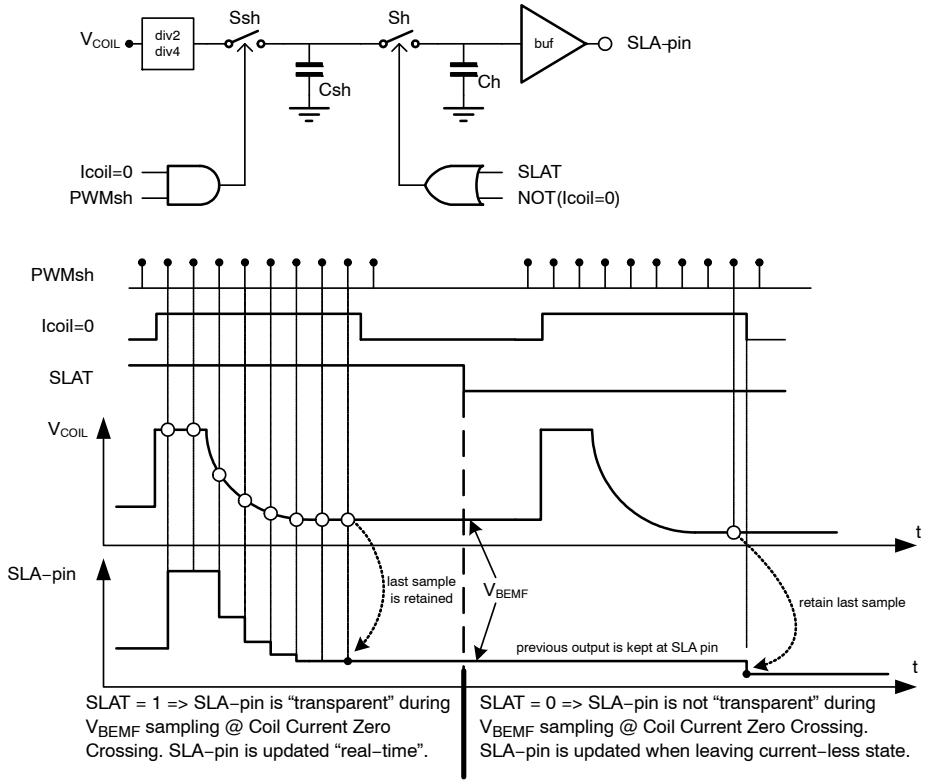


Figure 15. Timing Diagram of SLA−Pin

Warning, Error Detection and Diagnostics Feedback

Thermal Warning and Shutdown

When junction temperature rises above T_{TW}, the thermal warning bit <TW> is set (Table 14 SPI Status registers Address SR0). If junction temperature increases above thermal shutdown level, then the circuit goes in “Thermal Shutdown” mode (<TSD>) and all driver transistors are disabled (high impedance) (see Table 14 SPI Status registers Address SR2). The conditions to reset flag <TSD> is to be at a temperature lower than T_{tw} and to clear the <TSD> flag by reading it using any SPI read command.

Overcurrent Detection

The overcurrent detection circuit monitors the load current in each activated output stage. If the load current exceeds the over−current detection threshold, then the overcurrent flag is set and the drivers are switched off to reduce the power dissipation and to protect the integrated circuit. Each driver transistor has an individual detection bit (see Table 14 SPI Status Registers Address SR1 and SR2: <OVCXij> and <OVCYij>). Error condition is latched and the microcontroller needs to clean the status bits to reactivate the drivers.

Note: Successive reading the SPI Status Registers 1 and 2 in case of a short circuit condition, may lead to damage to the drivers.

Open Coil/Current Not Reached Detection

Open coil detection is based on the observation of 100% duty cycle of the PWM regulator. If in a coil 100% duty cycle is detected for longer than 200 ms then the related driver transistors are disabled (high−impedance) and an appropriate bit in the SPI status register is set (<OPENX> or <OPENY>). (Table 14)

When the resistance of a motor coil is very large and the supply voltage is low, it can happen that the motor driver is not able to deliver the requested current to the motor. Under these conditions the PWM controller duty cycle will be 100% and after 200 ms the error pin and <OPENX>, <OPENY> will flag this situation (motor current is kept alive). This feature can be used to test if the operating conditions (supply voltage, motor coil resistance) still allow reaching the requested coil−current or else the coil current should be reduced.

Charge Pump Failure

The charge pump is an important circuit that guarantees low $R_{DS(on)}$ for all drivers, especially for low supply voltages. If supply voltage is too low or external components are not properly connected to guarantee $R_{DS(on)}$ of the drivers, then the bit <CPFAIL> is set (Table 14). Also after POR the charge pump voltage will need some time to exceed the required threshold. During that time <CPFAIL> will be set to “1”.

Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = <TW> OR <TSD> OR <OVCXij> OR <OVCYij> OR <OPENi> OR <CPFAIL>

Logic Supply Regulator

AMIS−30543 has an on−chip 5 V low−drop regulator with external capacitor to supply the digital part of the chip, some low−voltage analog blocks and external circuitry. The voltage level is derived from an internal bandgap reference. To calculate the available drive−current for external circuitry, the specified I_{load} should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See Table 4. DC parameters

Power−On Reset (POR) Function

The open drain output pin $\overline{POR}$/WD provides an “active low” reset for external purposes. At powerup of AMIS−30543, this pin will be kept low for some time to reset for example an external microcontroller. A small analogue filter avoids resetting due to spikes or noise on the V_{DD} supply.

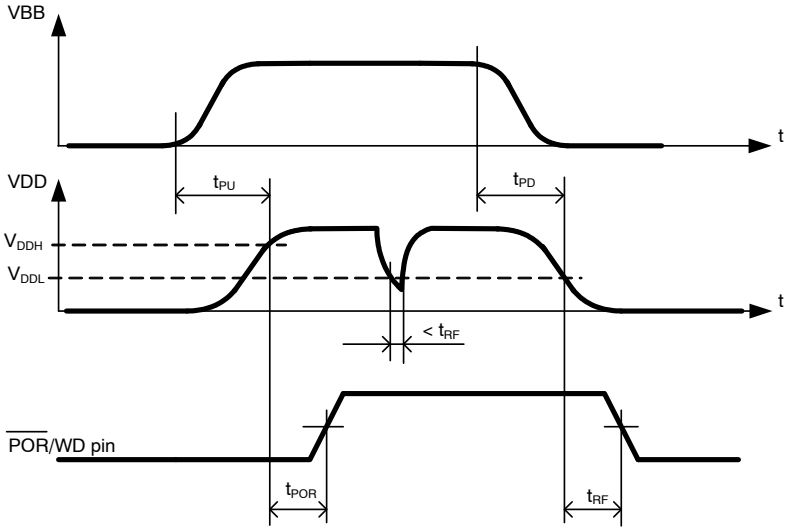


Figure 16. Power−on−Reset Timing Diagram

Watchdog Function

The watchdog function is enabled/disabled through <WDEN> bit (Table 11: SPI CONTROL REGISTERS). Once this bit has been set to “1” (watchdog enable), the microcontroller needs to re−write this bit to clear an internal timer before the watchdog timeout interval expires. In case the timer is activated and WDEN is acknowledged too early (before t_{WDPR}) or not within the interval (after t_{WDTO}), then a reset of the microcontroller will occur through $\overline{POR}$/WD pin. In addition, a warm/cold boot bit <WD> is available (see Tables 14 and 15) for further processing when the external microcontroller is alive again.

CLR pin (=Hard Reset)

Logic 0 on CLR pin allows normal operation of the chip. To reset the complete digital inside AMIS−30543, the input CLR needs to be pulled to logic 1 during minimum time given by t_{CLR} (Table 5 AC Parameters). This reset function clears all internal registers without the need of a power−cycle, except in sleep mode. Logic 0 on CLR pin resumes normal operation again.

The voltage regulator and charge pump remains functional during and after the reset and the $\overline{POR}$/WD pin is not activated. Watchdog function is reset completely.

Sleep Mode

The bit <SLP> in SPI Control Register 2 (See Table 10) is provided to enter a so−called “sleep mode”. This mode allows reduction of current−consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low−power mode
- All internal registers are maintaining their logic content
- NXT and DIR inputs are forbidden
- SPI communication remains possible (slight current increase during SPI communication)
- Oscillator and digital clocks are silent, except during SPI communication
- Registers cannot be cleared by using the CLR pin

VBB should be minimum 9 V to be able to enter Sleep Mode.

The voltage regulator remains active but with reduced current−output capability ($I_{LOADSLP}$). The watchdog timer stops running and it's value is kept in the counter. Upon leaving sleep mode, this timer continues from the value it had before entering sleep mode.

Normal operation is resumed after writing logic '0' to bit <SLP>. A startup time is needed for the charge pump to stabilize. After this time, NXT commands can be issued.

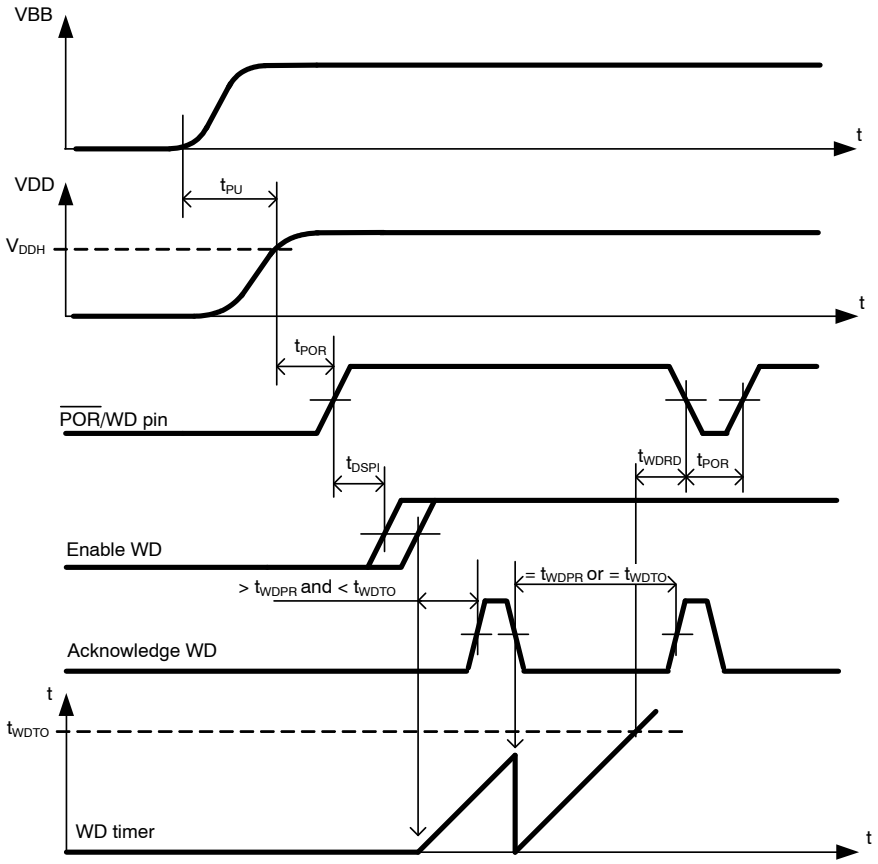


Figure 17. Watchdog Timing Diagram

NOTE: t_{DSPI} is the time needed by the external microcontroller to shift−in the <WDEN> bit after a powerup.

The duration of the watchdog timeout interval is programmable through the WDT[3:0] bits (See also Table 11: SPI CONTROL REGISTERS. The timing is given in Table 10 below.

Table 10. WATCHDOG TIMEOUT INTERVAL AS FUNCTION OF WDT[3.0]

Index WDT[3:0]		t_{WDTO} (ms)	Index WDT[3:0]		t_{WDTO} (ms)
0	0000	32	8	1000	288
1	0001	64	9	1001	320
2	0010	96	10	1010	352
3	0011	128	11	1011	384
4	0100	160	12	1100	416
5	0101	192	13	1101	448
6	0110	224	14	1110	480
7	0111	256	15	1111	512

SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS−30543. The implemented SPI block is designed to interface directly with numerous micro−controllers from several manufacturers. AMIS−30543 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (AMIS−30543), and DI signal is the output from the Master. A chip select line ($\overline{CS}$) allows individual selection of a Slave SPI device in a multiple−slave system. The $\overline{CS}$ line is active low. If AMIS−30543 is not selected, DO is pulled up with the external pull up resistor. Since AMIS−30543 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

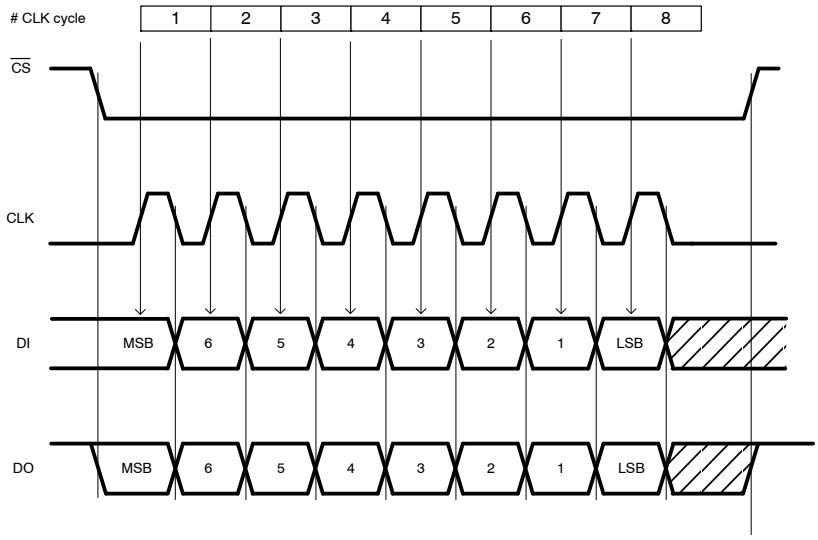


Figure 18. Timing Diagram of a SPI Transfer

NOTE: At the falling edge of the eight clock pulse the data−out shift register is updated with the content of the addressed internal SPI register. The internal SPI registers are updated at the first rising edge of the AMIS−30543 system clock when $\overline{CS}$ = High

Transfer Packet:

Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more bytes.

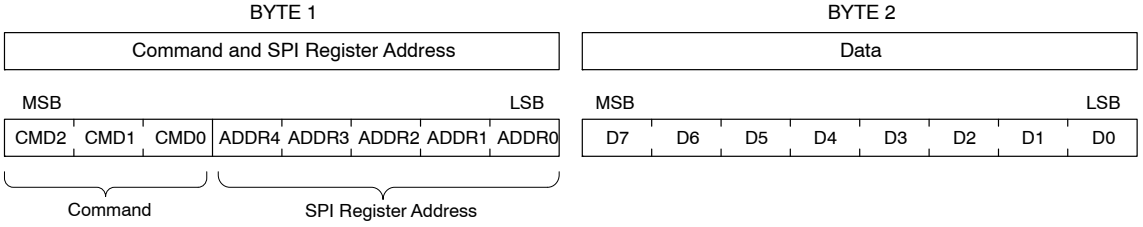


Figure 19. SPI Transfer Packet

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS−30543 the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from AMIS−30543 in a READ operation.

Two command types can be distinguished in the communication between master and AMIS−30543:

- READ **from** SPI Register with address ADDR[4:0]: **CMD2** = “0”
- WRITE **to** SPI Register with address ADDR[4:0]: **CMD2** = “1”

READ Operation

If the Master wants to read data from Status or Control Registers, it initiates the communication by sending a READ command. This READ command contains the address of the SPI register to be read out. At the falling edge of the eight clock pulse the data−out shift register is updated with the content of the corresponding internal SPI register. In the next 8−bit clock pulse train this data is shifted out via DO pin. At the same time the data shifted in from DI (Master) should be interpreted as the following successive command or dummy data.

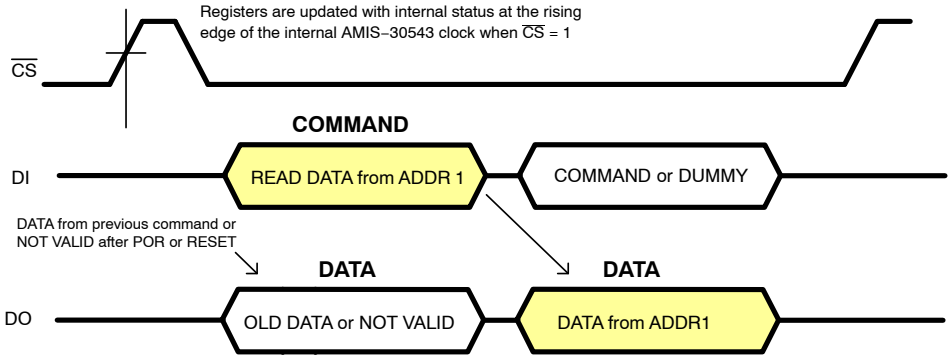


Figure 20. Single READ Operation where DATA from SPI Register with Address 1 is Read by the Master

All 4 Status Registers (see SPI Registers) contain 7 data bits and a parity check bit. The most significant bit (D7) represents a parity of D[6:0]. If the number of logical ones in D[6:0] is odd, the parity bit D7 equals “1”. If the number of logical ones in D[6:0] is even then the parity bit D7 equals “0”. This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

Also the Control Registers can be read out following the same routine. Control Registers don’t have a parity check.

The $\overline{CS}$ line is active low and may remain low between successive READ commands as illustrated in Figure 22. There is however one exception. In case an error condition is latched in one of Status Registers (see SPI Registers) the $\overline{ERR}$ pin is activated (See Section Error Output). This signal flags a problem to the external microcontroller. By reading the Status Registers information about the root cause of the problem can be determined. After this READ operation the Status Registers are cleared. Because the Status Registers and $\overline{ERR}$ pin (see SPI Registers) are only updated by the internal system clock when the $\overline{CS}$ line is high, the Master should force $\overline{CS}$ high immediately after the READ operation. For the same reason it is recommended to keep the $\overline{CS}$ line high always when the SPI bus is idle.

WRITE Operation

If the Master wants to write data to a Control Register it initiates the communication by sending a WRITE command. This contains the address of the SPI register to write to. The command is followed with a data byte. This incoming data will be stored in the corresponding Control Register after $\overline{CS}$ goes from low to high! AMIS−30543 responds on every incoming byte by shifting out via DO the data stored in the last received address.

It is important that the writing action (command − address and data) to the Control Register is exactly 16 bits long. If more or less bits are transmitted the complete transfer packet is ignored.

A WRITE command executed for a read−only register (e.g. Status Registers) will not affect the addressed register and the device operation.

Because after a power−on−reset the initial address is unknown the data shifted out via DO is not valid.

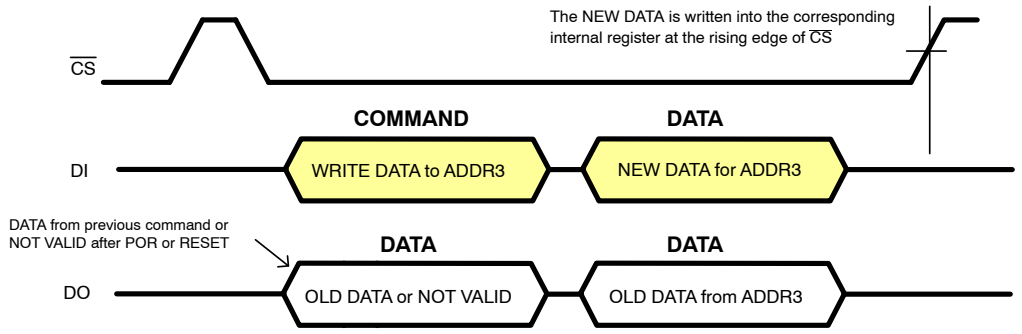


Figure 21. Single WRITE Operation Where DATA from the Master is Written in SPI Register with Address 3

Examples of combined READ and WRITE Operations

In the following examples successive READ and WRITE operations are combined. In Figure 22 the Master first reads the status from Register at ADDR4 and at ADDR5 followed by writing a control byte in Control Register at ADDR2. Note that during the write command the old data of the pointed register is returned at the moment the new data is shifted in

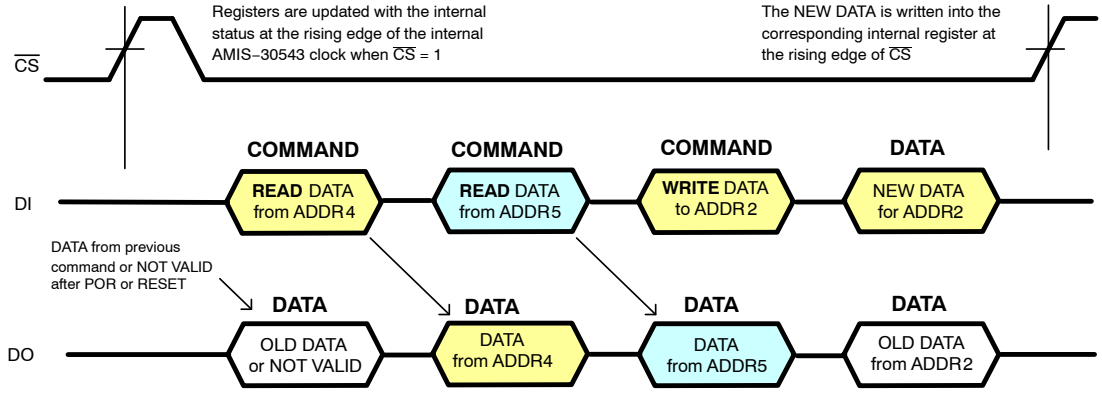


Figure 22. 2 Successive READ Commands Followed by a WRITE Command

After the write operation the Master could initiate a read back command in order to verify the data correctly written as illustrated in Figure 23. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is transmitted. This rule also applies when the master device wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when $\overline{CS}$ line is high, the first read out byte might represent old status information.

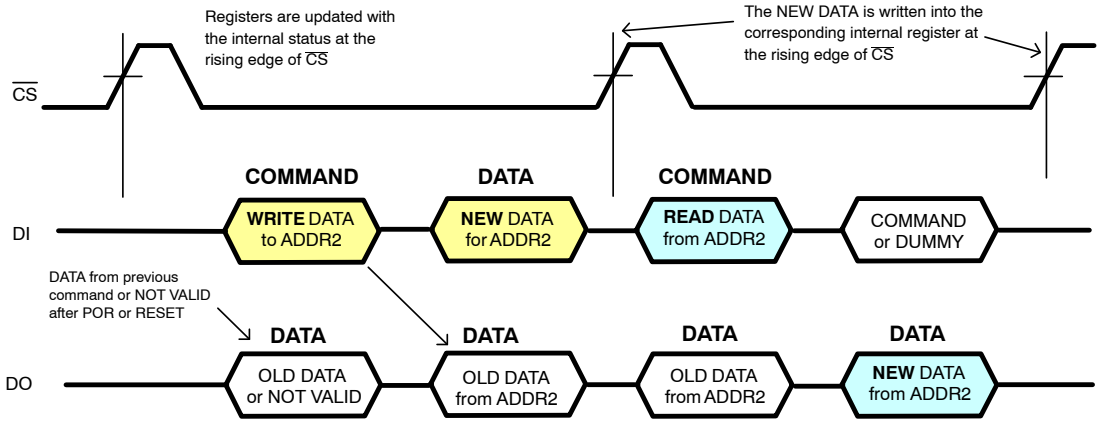


Figure 23. A WRITE Operation Where DATA from the Master is Written in SPI Register with Address 2 Followed by a READ Back Operation to Confirm a Correct WRITE Operation

NOTE: The internal data−out shift buffer of AMIS−30543 is updated with the content of the selected SPI register only at the last (every eight) falling edge of the CLK signal (see SPI Transfer Format and Pin Signals). As a result, new data for transmission cannot be written to the shift buffer at the beginning of the transfer packet and the first byte shifted out might represent old data.

Table 11. SPI CONTROL REGISTERS (All SPI control registers have Read/Write Access and default to “0” after power−on or hard reset)

		Structure							
	Content	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Access	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Address	**Reset**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
WR (00h)	Data	WDEN	WDT[3:0]				–	–	–
CR0 (01h)	Data	SM[2:0]			CUR[4:0]				
CR1 (02h)	Data	DIRCTRL	NXTP	–	–	PWMF	PWMJ	EMC[1:0]	
CR2 (03h)	Data	MOTEN	SLP	SLAG	SLAT	–	–	–	–
CR3 (09h)	Data	–	–	–	–	–	ESM[2:0]		

Where:

R/W Read and Write access

Reset: Status after power−On or hard reset

Table 12. SPI CONTROL PARAMETER OVERVIEW

Symbol	Description	Status		Value
DIRCTRL	Controls the direction of rotation (in combination with logic level on input DIR)	<DIR> = 0	<DIRCTRL> = 0	CW motion (Note 15)
			<DIRCTRL> = 1	CCW motion (Note 15)
		<DIR> = 1	<DIRCTRL> = 0	CCW motion (Note 15)
			<DIRCTRL> = 1	CW motion (Note 15)
NXTP	Selects if NXT triggers on rising or falling edge	<NXTP> = 0	Trigger on rising edge	
		<NXTP> = 1	Trigger on falling edge	
EMC[1:0]	Turn On − Turn−off Slopes of motor driver (Note 14)	00	Very Fast	
		01	Fast	
		10	Slow	
		11	Very Slow	
SLAT	Speed load angle transparency bit	<SLAT> = 0	SLA is not transparent	
		<SLAT> = 1	SLA is transparent	
SLAG	Speed load angle gain setting	<SLAG> = 0	Gain = 0.5	
		<SLAG> = 1	Gain = 0.25	
PWMF	Enables doubling of the PWM frequency (Note 14)	<PWMF> = 0	Default Frequency	
		<PWMF> = 1	Double Frequency	
PWMJ	Enables jittery PWM	<PWMJ> = 0	Jitter disabled	
		<PWMJ> = 1	Jitter enabled	
SM[2:0]	Stepmode (only valid if ESM[2:0] = 000)	000	1/32 Micro − Step	
		001	1/16 Micro − Step	
		010	1/8 Micro − Step	
		011	1/4 Micro − Step	
		100	Compensated Half Step	
		101	Uncompensated Half Step	
		110	Uncompensated full step	
		111	Uncompensated full step	
ESM[2:0]	Stepmode	001	1/128 Micro−Step	
		010	1/64 Micro−Step	
		011	Compensated full step, 2 phase on	
		100	Compensated full step, 1 phase on	
		Other	Stepping mode defined by SM[2:0]	
SLP	Enables sleep mode (if V_{BB} > 9 V)	<SLP> = 0	Active mode	
		<SLP> = 1	Sleep mode	
MOTEN	Activates the motor driver outputs	<MOTEN> = 0	Drivers disabled	
		<MOTEN> = 1	Drivers enabled	

14. The typical values can be found in Table 4: DC Parameters and in Table 5: AC parameters
15. Depending on the wiring of the motor connections

CUR[4:0] Selects IMCmax peak. This is the peak or amplitude of the regulated current waveform in the motor coils.

Table 13. SPI CONTROL PARAMETER OVERVIEW CUR[4:0]

Current Range (Note 17)	Index CUR[4:0]		Current (mA) (Note 16)	Current Range (Note 17)	Index CUR[4:0]		Current (mA) (Note 16)
0	0	00000	132	3	16	10000	1405
	1	00001	245		17	10001	1520
	2	00010	355		18	10010	1695
1	3	00011	395		19	10011	1850
	4	00100	445		20	10100	2070
	5	00101	485		21	10101	2240
	6	00110	540		22	10110	2440
	7	00111	585		23	10111	2700
	8	01000	640		24	11000	2845
	9	01001	715		25	11001	3000
2	10	01010	780		26	11010	3000
	11	01011	870		27	11011	3000
	12	01100	955		28	11100	3000
	13	01101	1060		29	11101	3000
	14	01110	1150		30	11110	3000
	15	01111	1260		31	11111	3000

16. Typical current amplitude at T_J = 125
17. Reducing the current over different current ranges might trigger overcurrent detection. See dedicated application note for solutions

SPI Status Register Description

All 5 SPI status registers have Read Access and are default to “0” after power−on or hard reset.

Table 14. SPI STATUS REGISTERS

		Structure							
	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Access	R	R	R	R	R	R	R	R
Address	Reset	0	0	0	0	0	0	0	0
SR0 (04h)	Data is not latched	PAR	TW	CPFAIL	WD	OPENX	OPENY	–	–
SR1 (05h)	Data is latched	PAR	OVCXPT	OVCXPB	OVCXNT	OVCXNB	–	–	–
SR2 (06h)	Data is latched	PAR	OVCYPT	OVCYPB	OVCYNT	OVCYNB	TSD	–	–
SR3 (07h)	Data is not latched	PAR	MSP[8:2]						
SR4 (0Ah)	Data is not latched	PAR	MSP[6:0]						

Where:

R Read only mode access

Reset Status after power−on or hard reset

PAR Parity check

Table 15. SPI STATUS FLAGS OVERVIEW

Mnemonic	Flag	Length (bit)	Related SPI Register	Comment	Reset State
CPFail	Charge pump failure	1	Status Register 0	‘0’ = no failure ‘1’ = failure: indicates that the charge pump does not reach the required voltage level. Note 1	‘0’
MSP[8:0]	Micro−step position	9	Status Register 3 and Status Register 4	Translator micro step position	‘000000000’
OPENX	OPEN Coil X	1	Status Register 0	‘1’ = Open coil detected	‘0’
OPENY	OPEN Coil Y	1	Status Register 0	‘1’ = Open coil detected	‘0’
OVCXNB	**OV**er **C**urrent on X H−bridge; MOT**XN** terminal; **B**ottom tran.	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at bottom transistor XN−terminal	‘0’
OVCXNT	**OV**er **C**urrent on X H−bridge; MOT**XN** terminal; **T**op transist.	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at top transistor XN−terminal	‘0’
OVCXPB	**OV**er **C**urrent on X H−bridge; MOT**XP** terminal; **B**ottom tran.	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at bottom transistor XP−terminal	‘0’
OVCXPT	**OV**er **C**urrent on X H−bridge; MOT**XP** terminal; **T**op transist.	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at top transistor XP−terminal	‘0’
OVCYNB	**OV**er **C**urrent on Y H−bridge; MOTYN terminal; **B**ottom tran.	1	Status Register 2	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at bottom transistor YN−terminal	‘0’
OVCYNT	**OV**er Current on Y H−bridge; MOT**YN** terminal; **T**op transist.	1	Status Register 2	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at top transistor YN−terminal	‘0’
OVCYPB	**OV**er **C**urrent on Y H−bridge; MOT**YP** terminal; **B**ottom tran.	1	Status Register 2	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at bottom transistor YP−terminal	‘0’
OVCYPT	**OV**er **C**urrent on Y H−bridge; MOT**YP** terminal; **T**op transist.	1	Status Register 2	‘0’ = no failure ‘1’ = failure: indicates that over current is detected at top transistor YP−terminal	‘0’
TSD	Thermal shutdown	1	Status Register 2		‘0’
TW	Thermal warning	1	Status Register 0		‘0’
WD	Watchdog event	1	Status Register 0	‘1’ = watchdog reset after time−out	‘0’

NOTE: WD − This bit indicates that the watchdog timer has not been cleared properly. If the master reads that WD is set to “1” after reset, it means that a watchdog reset occurred (warm boot) instead of POR (cold boot). WD bit will be cleared only when the master writes “0” to WDEN bit.

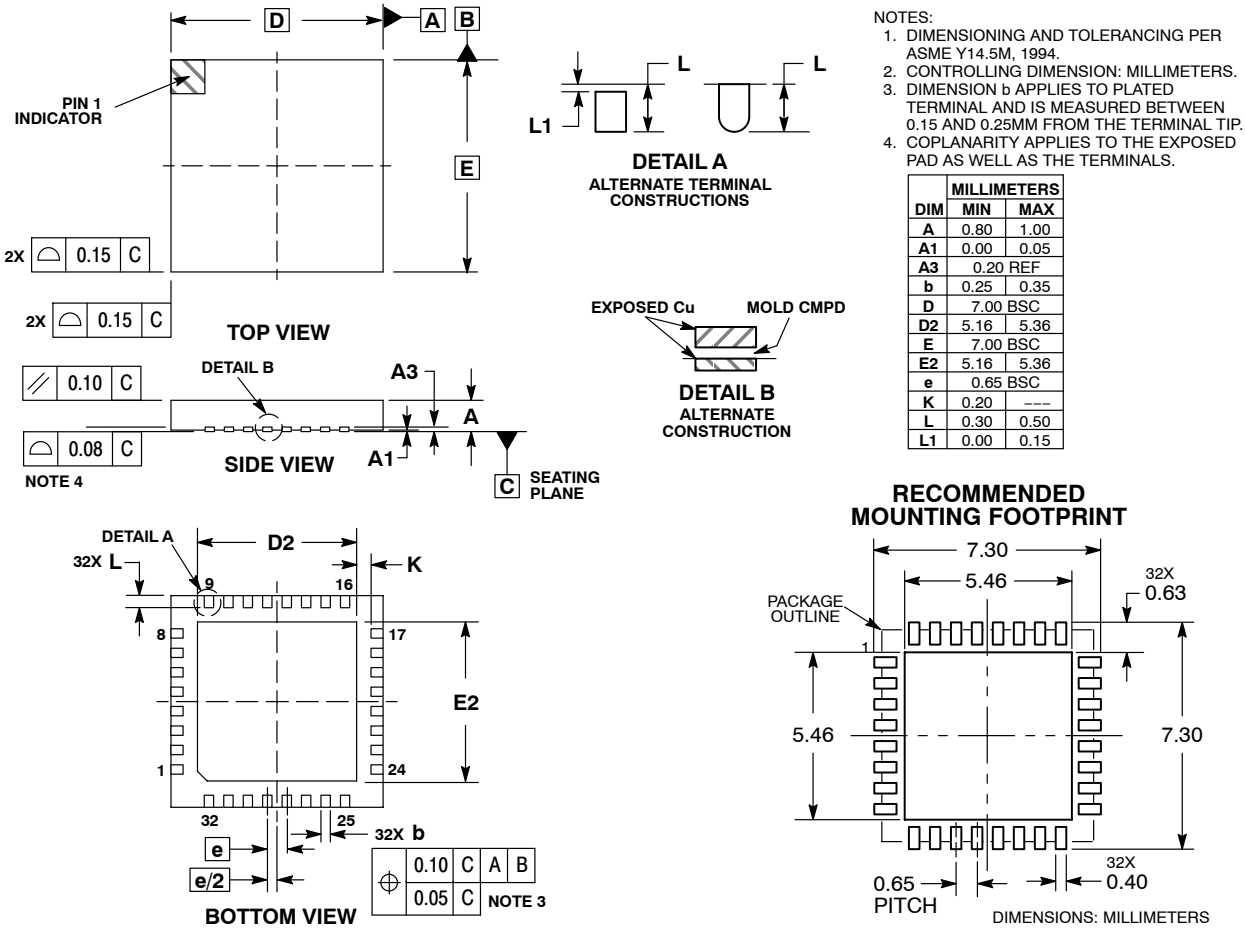
Table 16. ORDERING INFORMATION

Part No.	Peak Current	Temperature Range	Package	Shipping†
AMIS30543C5431G	3000 mA	−40°C to 125°C	NQFP−32 (7 x 7 mm) (Pb−Free)	Units / Tubes
AMIS30543C5431RG	3000 mA	−40°C to 125°C	NQFP−32 (7 x 7 mm) (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN32 7x7, 0.65P
CASE 485J−02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	7.00 BSC	
D2	5.16	5.36
E	7.00 BSC	
E2	5.16	5.36
e	0.65 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.15

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com