IP4787CZ32

DVI and HDMI interface ESD protection, DDC/CEC buffering, hot plug handling and backdrive protection

Rev. 3 — 19 December 2014 **Product data sheet**

1. Product profile

1.1 General description

The IP4787CZ32 is designed to protect High-Definition Multimedia Interface (HDMI) receiver interfaces. It includes HDMI 5 V power management, Display Data Channel (DDC) buffering and decoupling, hot plug drive, backdrive protection, Consumer Electronic Control (CEC) buffering and decoupling, and ±12 kV contact ElectroStatic Discharge (ESD) protection for all external I/Os, exceeding the IEC 61000-4-2, level 4 standard.

The IP4787CZ32 incorporates Transmission Line Clamping (TLC) technology on the high-speed Transition-Minimized Differential Signaling (TMDS) lines to simplify routing and help reduce impedance discontinuities. All TMDS lines are protected by an impedance-matched diode configuration that minimizes impedance discontinuities caused by typical shunt diodes.

The 5 V power management enables host access to the [Extended Display Identification Data (EDID)] memory even if no HDMI plug is connected. The overall load to the 5 V line is according to the HDMI requirements.

The DDC lines use a buffering concept which decouples the internal capacitive load from the external capacitive load for use with standard Complementary Metal Oxide Semiconductor (CMOS) or Low Voltage Transistor-Transistor Logic (LVTTL) I/O cells down to 1.2 V. This buffering also redrives the DDC and CEC signals, allowing the use of longer or cheaper HDMI cables with a higher capacitance. The internal hot plug drive module simplifies the application of the HDMI receiver to control the hot plug signal.

All lines provide appropriate integrated pull-ups and pull-downs for HDMI compliance and backdrive protection to guarantee that HDMI interface signals are not pulled down if the system is powered down or enters Standby mode. Only a single external capacitor is required for operation.

1.2 Features and benefits

- HDMI 2.0 and all backward compatible standards are supported
- 6.0 Gbps TMDS bit rate (600 Mcsc TMDS character rate) compatible
- Supports UHD 4k (2160p) 60 Hz display modes
- Impedance matched 100 Ω differential transmission line ESD protection for TMDS lines (±10 Ω). No Printed-Circuit Board (PCB) pre-compensation required
- Simplified flow-through routing utilizing less overall PCB space
- DDC capacitive decoupling between system side and HDMI connector side and buffering to drive cable with high capacitive load (> 700 pF/25 m)

- All external I/O lines with ESD protection of at least ±12 kV, exceeding the IEC 61000-4-2, level 4 standard
- Hot plug drive module
- Utility biasing module (HEAC compliant)
- CEC buffering and isolation, with integrated backdrive-protected 26 kΩ pull-up
- Robust ESD protection without degradation after repeated ESD strikes
- Highest integration in a small footprint, PCB level, optimized RF routing, 32-pin HVQFN leadless package

1.3 Applications

- The IP4787CZ32 can be used for a wide range of HDMI sink devices, consumer and computing electronics:
  - Digital High-Definition (HD) TV
  - Set-top box
  - PC monitor
  - Projector
  - Multimedia audio amplifier
  - HDMI picture performance quality enhancer module
  - Digital Visual Interface (DVI)

2. Pinning information

2.1 Pinning

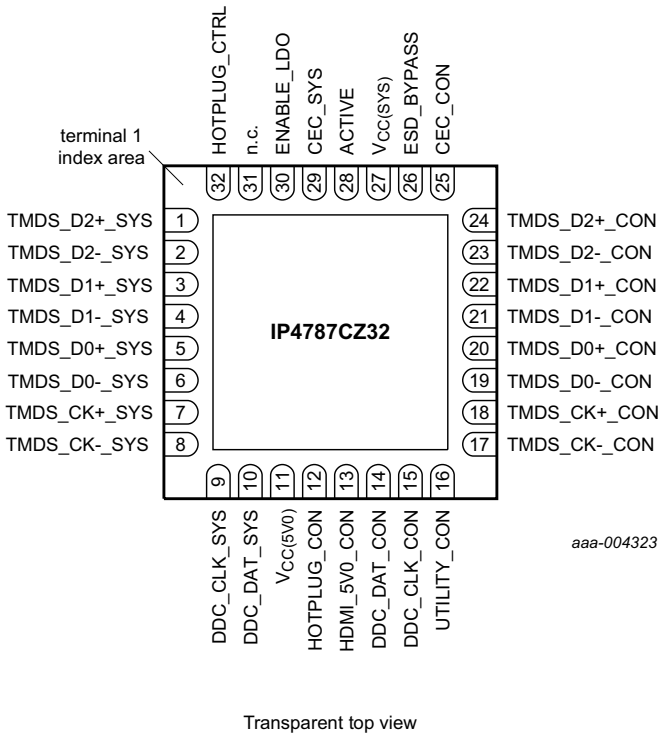


Fig 1. Pin configuration IP4787CZ32

2.2 Pin description

Table 1. Pin description

Pin	Name	Description
1	TMDS_D2+_SYS	TMDS to ASIC inside system
2	TMDS_D2−_SYS	TMDS to ASIC inside system
3	TMDS_D1+_SYS	TMDS to ASIC inside system
4	TMDS_D1−_SYS	TMDS to ASIC inside system
5	TMDS_D0+_SYS	TMDS to ASIC inside system
6	TMDS_D0−_SYS	TMDS to ASIC inside system
7	TMDS_CK+_SYS	TMDS to ASIC inside system
8	TMDS_CK−_SYS	TMDS to ASIC inside system
9	DDC_CLK_SYS	DDC clock system side
10	DDC_DAT_SYS	DDC data system side
11	$V_{CC(5V0)}$	5 V supply input
12	HOTPLUG_CON	hot plug output to connector
13	HDMI_5V0_CON	5 V input from connector
14	DDC_DAT_CON	DDC data connector side

Table 1. Pin description *...continued*

Pin	Name	Description
15	DDC_CLK_CON	DDC clock connector side
16	UTILITY_CON	utility line ESD protection
17	TMDS_CK−_CON	TMDS ESD protection to connector
18	TMDS_CK+_CON	TMDS ESD protection to connector
19	TMDS_D0−_CON	TMDS ESD protection to connector
20	TMDS_D0+_CON	TMDS ESD protection to connector
21	TMDS_D1−_CON	TMDS ESD protection to connector
22	TMDS_D1+_CON	TMDS ESD protection to connector
23	TMDS_D2−_CON	TMDS ESD protection to connector
24	TMDS_D2+_CON	TMDS ESD protection to connector
25	CEC_CON	CEC signal connector side
26	ESD_BYPASS	ESD bias voltage
27	$V_{CC(SYS)}$	supply voltage for level shifting
28	ACTIVE	CEC Standby mode control (LOW for lowest power, CEC-only mode)
29	CEC_SYS	CEC I/O signal system side
30	ENABLE_LDO	5 V LDO enable
31	n.c.	not connected
32	HOTPLUG_CTRL	hot plug control input from system side
ground pad	GND	ground

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4787CZ32	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

4. Functional diagram

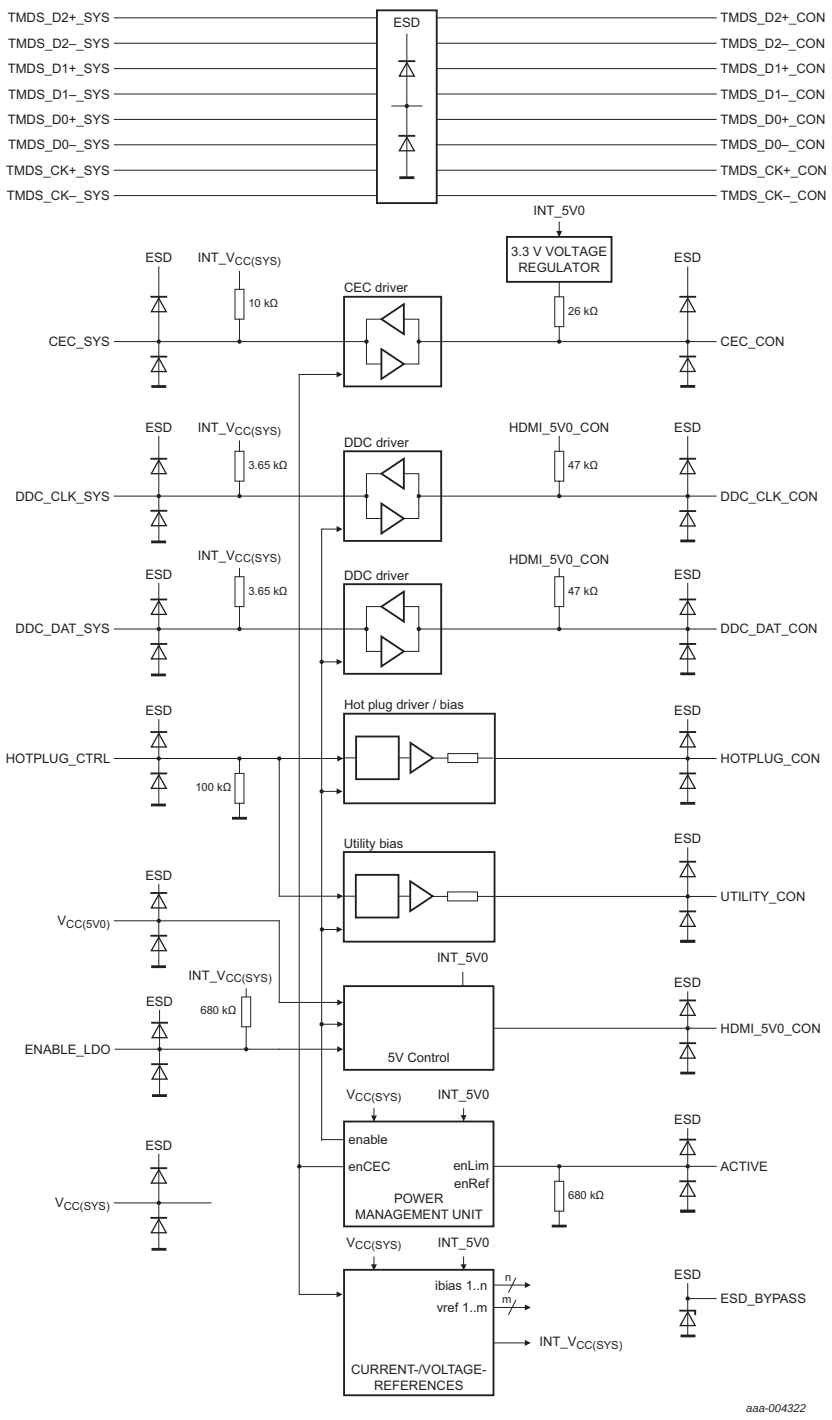


Fig 2. Functional diagram

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		GND − 0.5	6.5	V
V_I	input voltage	I/O pins	GND − 0.5	5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 (contact) [1]	-	±12	kV
		IEC 61000-4-2, level 1 (contact) [2]	-	±2	kV
P_{tot}	total power dissipation	DDC operating at 100 kHz; CEC operating at 1 kHz; 50 % duty cycle; ACTIVE = HIGH	-	50	mW
		DDC and CEC bus in idle mode; ACTIVE = HIGH	-	3.0	mW
		DDC and CEC bus in idle mode; ACTIVE = LOW	-	1.2	mW
T_{amb}	ambient temperature		−25	+85	°C
T_{stg}	storage temperature		−55	+125	°C

[1] Connector-side pins (typically denoted with '_CON' suffix) to ground.

[2] System-side pins: CEC_SYS, DDC_DAT_SYS, DDC_CLK_SYS, HOTPLUG_CTRL, ACTIVE, $V_{CC(SYS)}$ and $V_{CC(5V0)}$.

6. Static characteristics

Table 4. Supplies

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		4.5	5.0	6.5	V
$V_{(HDMI\_5V0\_CON)}$	voltage on pin HDMI_5V0_CON	[1]	4.5	5.0	6.5	V
$V_{CC(SYS)}$	system supply voltage		1.1	3.3	3.63	V

[1] HDMI_5V0_CON is used as supply in case ENABLE_LDO is inactive and $V_{CC(5V0)}$ is unavailable or lower than HDMI_5V0_CON.

Table 5. TMDS protection circuit

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS channel						
$Z_{i(dif)}$	differential input impedance	TDR measured; t_r = 200 ps	90	100	110	Ω
C_{eff}	effective capacitance	equivalent shunt capacitance for TDR minimum; t_r = 200 ps [1][2]	-	0.6	-	pF
Protection diode						
V_{BRzd}	Zener diode breakdown voltage	I = 1.0 mA	6.0	-	9.0	V
r_{dyn}	dynamic resistance	surge; I = 1.0 A; IEC 61000-4-5/9				
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
		TLP [3]				
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
I_{bck}	back current	$V_{CC(5V0)} < V_{ch(TMDS)}$ [4][5]	-	0.1	1.0	μA
I_{LR}	reverse leakage current	V_I = 3.0 V	-	1.0	-	μA
V_F	forward voltage		-	0.7	-	V
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8.0	-	V

[1] This parameter is guaranteed by design.

[2] Capacitive dip at HDMI Time Domain Reflectometer (TDR) measurement conditions.

[3] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing Transmission Line Pulse (TLP) component level method 50 TDR.

[4] Signal pins:
TMDS_D0+_CON, TMDS_D0−_CON, TMDS_D1+_CON, TMDS_D1−_CON, TMDS_D2+_CON, TMDS_D2−_CON, TMDS_CK+_CON, TMDS_CK−_CON,
TMDS_D0+_SYS, TMDS_D0−_SYS, TMDS_D1+_SYS, TMDS_D1−_SYS, TMDS_D2+_SYS, TMDS_D2−_SYS, TMDS_CK+_SYS and TMDS_CK−_SYS.

[5] Backdrive current from TMDS_x_SYS and TMDS_x_CON pins to local $V_{CC(5V0)}$ bias rail at power-down. Device does not block backdrive current leakage through the device to/from ASIC I/O pins connected to TMDS_x_SYS pins.

Table 6. HDMI_5V0_CON

T_{amb} = –25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
r_{dyn}	dynamic resistance	TLP [1]				
		positive transient	-	1.0	-	Ω
		negative transient	-	1.0	-	Ω
V_{CL}	clamping voltage	100 ns TLP; 50 Ω pulser at 50 ns	-	8	-	V
$I_{I(max)}$	maximum input current	$V_{(HDMI\_5V0\_CON)}$ = 5.3 V	-	-	50	mA
I_{bck}	back current	$V_{CC(5V0)} < V_{(HDMI\_5V0\_CON)}$ [2]	-	-	10	μA

[1] ANSI-ESD SP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

[2] I_{bck} defines the current that flows from the $V_{CC(5V0)}$ pin into the system supply. This parameter is guaranteed by design.

Table 7. Static characteristics

T_{amb} = –25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC_CLK_CON; DDC_DAT_CON [1]						
V_{IH}	HIGH-level input voltage		0.5 × $V_{(HDMI\_5V0\_CON)}$	-	6.5	V
V_{IL}	LOW-level input voltage		–0.5	-	0.3 × $V_{(HDMI\_5V0\_CON)}$	V
V_{OH}	HIGH-level output voltage	[2]	$V_{(HDMI\_5V0\_CON)}$ – 0.02	-	$V_{(HDMI\_5V0\_CON)}$ + 0.02	V
V_{OL}	LOW-level output voltage	internal pull-up and external sink	-	100	200	mV
V_{IK}	input clamping voltage	I_I = –18 mA	-	-	–1.0	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 5.0 V; $V_{CC(SYS)}$ = 3.3 V; ACTIVE = HIGH [2][3]	-	8.0	10	pF
R_{pu}	pull-up resistance		42.3	47	51.7	kΩ
DDC_CLK_SYS; DDC_DAT_SYS [1][4]						
V_{IH}	HIGH-level input voltage	$V_{CC(SYS)}$ = 1.2 V	310	-	-	mV
		$V_{CC(SYS)}$ = 1.8 V	450	-	-	mV
		$V_{CC(SYS)}$ = 2.5 V	620	-	-	mV
		$V_{CC(SYS)}$ = 3.3 V	760	-	-	mV
V_{IL}	LOW-level input voltage	$V_{CC(SYS)}$ = 1.2 V	-	-	240	mV
		$V_{CC(SYS)}$ = 1.8 V	-	-	330	mV
		$V_{CC(SYS)}$ = 2.5 V	-	-	370	mV
		$V_{CC(SYS)}$ = 3.3 V	-	-	390	mV
V_{OH}	HIGH-level output voltage	[2]	0.8 × $V_{CC(SYS)}$	-	$V_{CC(SYS)}$ + 0.02	V
V_{OL}	LOW-level output voltage	$V_{CC(SYS)}$ = 1.2 V	-	330	340	mV
		$V_{CC(SYS)}$ = 1.8 V	-	490	500	mV
		$V_{CC(SYS)}$ = 2.5 V	-	640	690	mV
		$V_{CC(SYS)}$ = 3.3 V	-	685	790	mV
V_{IK}	input clamping voltage	I_I = –18 mA	-	-	–1.0	V

Table 7. Static characteristics *...continued*

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	6.0	8.0	pF
R_{pu}	pull-up resistance		3.2	3.65	4.1	kΩ
CEC_CON [1]						
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.80	V
V_{OH}	HIGH-level output voltage		2.88	3.3	3.63	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.5 mA	-	100	200	mV
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 1.65 V; AC input = 2.5 $V_{(p-p)}$; f = 100 kHz [2]	-	8.0	10	pF
R_{pu}	pull-up resistance		23.4	26.0	28.6	kΩ
$I_{leak(CEC)}$	CEC leakage current	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; CEC_CON connected to 3.63 V via 27 kΩ	-	-	0.1	µA
CEC_SYS [1][4]						
V_{IH}	HIGH-level input voltage	$V_{CC(SYS)}$ = 1.2 V	310	-	-	mV
		$V_{CC(SYS)}$ = 1.8 V	450	-	-	mV
		$V_{CC(SYS)}$ = 2.5 V	620	-	-	mV
		$V_{CC(SYS)}$ = 3.3 V	760	-	-	mV
V_{IL}	LOW-level input voltage	$V_{CC(SYS)}$ = 1.2 V	-	-	240	mV
		$V_{CC(SYS)}$ = 1.8 V	-	-	330	mV
		$V_{CC(SYS)}$ = 2.5 V	-	-	370	mV
		$V_{CC(SYS)}$ = 3.3 V	-	-	390	mV
V_{OH}	HIGH-level output voltage	[2]	0.8 × $V_{CC(SYS)}$	-	$V_{CC(SYS)}$ + 0.02	V
V_{OL}	LOW-level output voltage	$V_{CC(SYS)}$ = 1.2 V	-	330	340	mV
		$V_{CC(SYS)}$ = 1.8 V	-	490	500	mV
		$V_{CC(SYS)}$ = 2.5 V	-	640	690	mV
		$V_{CC(SYS)}$ = 3.3 V	-	675	770	mV
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 1.65 V; AC input = 2.5 $V_{(p-p)}$; f = 100 kHz [2]	-	6.0	7.0	pF
R_{pu}	pull-up resistance		8.5	10	11.5	kΩ

Table 7. Static characteristics *...continued*

T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HOTPLUG_CON; UTILITY_CON[1]						
V_{OH}	HIGH-level output voltage		3.6	4	4.4	V
V_{OL}	LOW-level output voltage		-	-	0.4	V
R_O	output resistance		0.8	1.0	1.2	kΩ
C_O	output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	8.0	10	pF
HOTPLUG_CTRL[1]						
V_{IH}	HIGH-level input voltage	HIGH = hot plug on [5]	1.0	-	-	V
V_{IL}	LOW-level input voltage	LOW = hot plug off [5]	-	-	0.4	V
R_{pd}	pull-down resistance		60	100	140	kΩ
C_i	input capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(SYS)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz [2]	-	6.0	7.0	pF

[1] The device is active if the input voltage at pin ACTIVE is above the HIGH level.

[2] This parameter is guaranteed by design.

[3] Capacitive load measured at power-on.

[4] No external pull-up resistor attached.

[5] See Section 9.7 for details on the hot plug functionality.

Table 8. Power management

$V_{CC(SYS)}$ = 1.10 V to 3.63 V; $V_{CC(5V0)}$ = 4.5 V to 6.5 V; GND = 0 V; T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System side: input pin ACTIVE[1]						
V_{IH}	HIGH-level input voltage	HIGH = active [2]	1.0	-	-	V
V_{IL}	LOW-level input voltage	LOW = standby [3]	-	-	0.4	V
R_{pd}	pull-down resistance			680		kΩ
C_i	input capacitance	V_I = 3 V or 0 V [4]	-	6	7	pF
System side: input pin ENABLE_LDO						
V_{IH}	HIGH-level input voltage		1.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.4	V
R_{pu}	pull-up resistance			680		kΩ
C_i	input capacitance	V_I = 3 V or 0 V [4]	-	6	7	pF

[1] The ACTIVE pin should be connected permanently to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ if no enable control is needed.

[2] DDC buffers, Hot Plug Detect (HPD) driver, utility bias and HDMI_5V0_CON out enabled; CEC buffer enabled.

[3] DDC buffers, HPD driver, utility bias and HDMI_5V0_CON out disabled; CEC buffer enabled.

[4] This parameter is guaranteed by design.

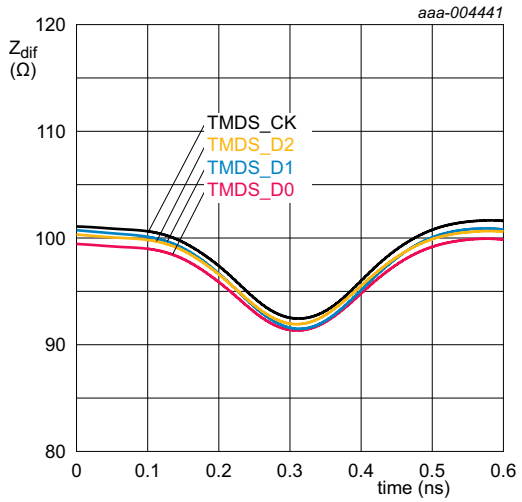
7. Dynamic characteristics

Table 9. Dynamic characteristics

$V_{CC(5V0)}$ = 5.0 V; $V_{CC(SYS)}$ = 1.8 V; GND = 0 V; T_{amb} = −25 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDC_DAT_SYS, DDC_CLK_SYS, DDC_DAT_CON, DDC_CLK_CON[1]						
t_{PLH}	LOW to HIGH propagation delay	system side to connector side Figure 16	-	80	-	ns
t_{PHL}	HIGH to LOW propagation delay	system side to connector side Figure 16	-	60	-	ns
t_{PLH}	LOW to HIGH propagation delay	connector side to system side Figure 17	-	120	-	ns
t_{PHL}	HIGH to LOW propagation delay	connector side to system side Figure 17	-	80	-	ns
t_{TLH}	LOW to HIGH transition time	connector side Figure 18	-	150	-	ns
t_{THL}	HIGH to LOW transition time	connector side Figure 18	-	100	-	ns
t_{TLH}	LOW to HIGH transition time	system side Figure 19	-	250	-	ns
t_{THL}	HIGH to LOW transition time	system side Figure 19	-	80	-	ns

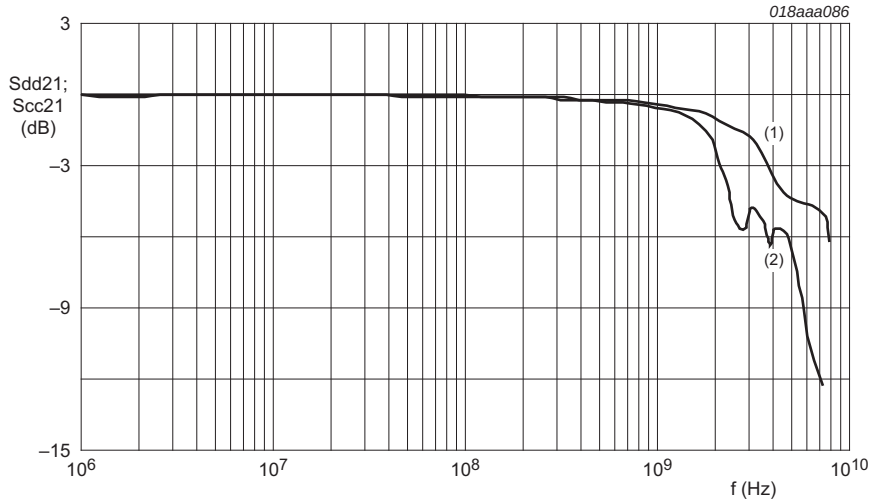
[1] All dynamic measurements are done with a 75 pF load. Rise times on system side are determined only by internal pull-up resistors. Rise times on connector side are determined by external 1.5 kΩ and internal pull-up resistors.



t_r = 200 ps; no filter; $V_{CC(5V0)}$ = 5 V

100 Ω differential (CH1 + CH2)

Fig 3. Differential TDR plot

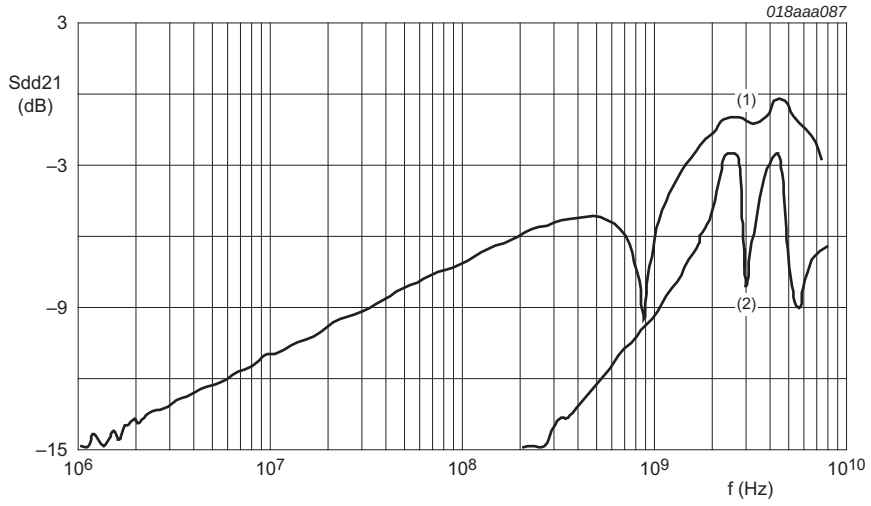


(1) Sdd21

(2) Scc21

Normalized to 100 Ω; differential pairs at signal pins.

Fig 4. Mixed-mode differential and common-mode insertion loss; typical values

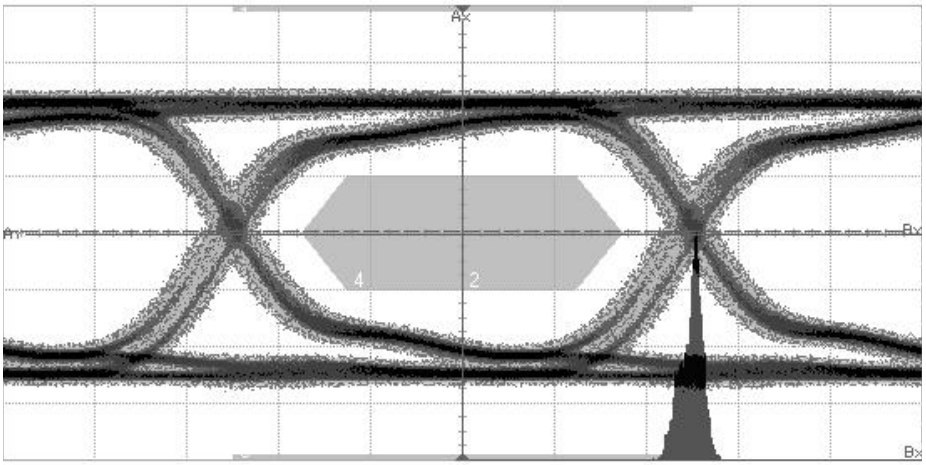


(1) Sdd21; Near End Crosstalk (NEXT)

(2) Sdd21; Far End Crosstalk (FEXT)

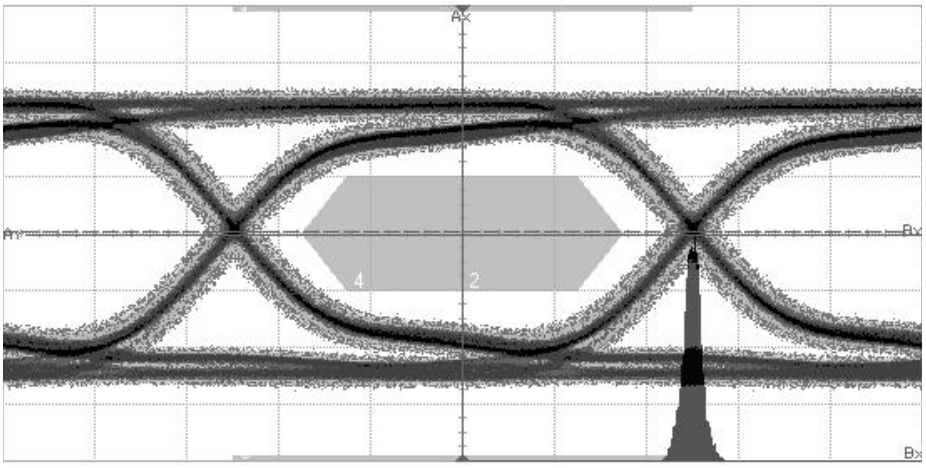
normalized to 100 Ω; differential pairs CH1/CH2 versus CH3/CH4

Fig 5. Mixed-mode differential and common-mode NEXT / FEXT; typical values



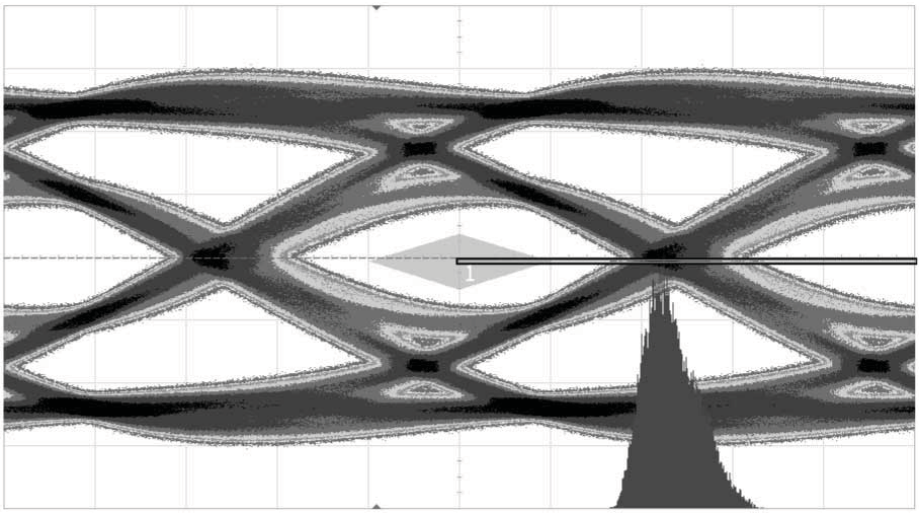
227 MHz pixel clock
Horizontal scale: 200 mV/div
Vertical scale: 90 ps/div
Offset: 42.6 mV

Fig 6. Eye diagram using IP4787CZ32 (1080p, 12 bit)



297 MHz pixel clock
Horizontal scale: 200 mV/div
Vertical scale: 67.5 ps/div
Offset: 42.6 mV

Fig 7. Eye diagram using IP4787CZ32 (1080p, 16 bit)



aaa-013775

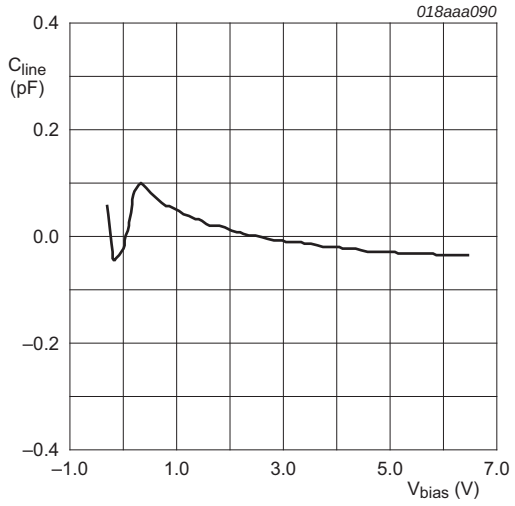
148.5 MHz test frequency

Horizontal scale: 53.8 ps/div

Vertical scale: 200 mV/div

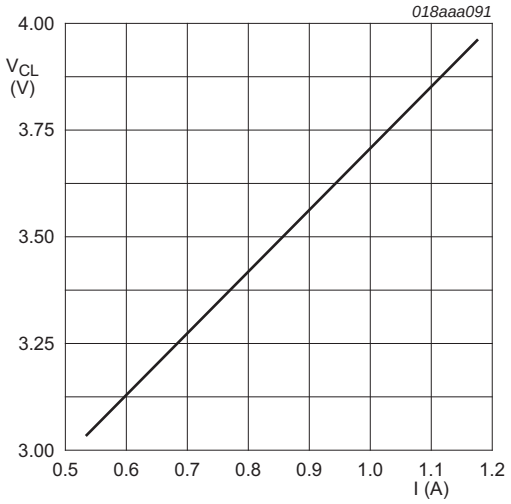
Measured at TP2 with worst cable emulator, reference cable equalizer and worst case negative skew

Fig 8. Eye diagram using IP4787CZ32 (2160p, 60 Hz)



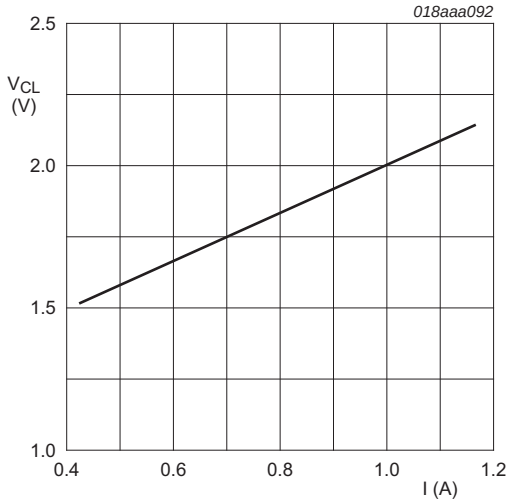
Deviation from typical capacitance normalized at V_{bias} = 2.5 V

Fig 9. Eye diagram using IP4787CZ32 (2160p, 60 Hz)



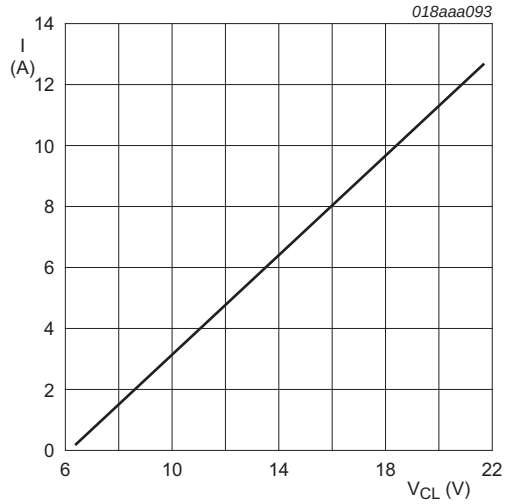
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 10. Dynamic resistance with positive clamping



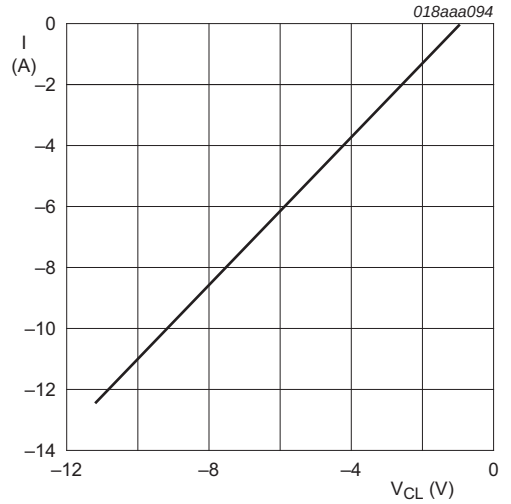
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 11. Dynamic resistance with negative clamping



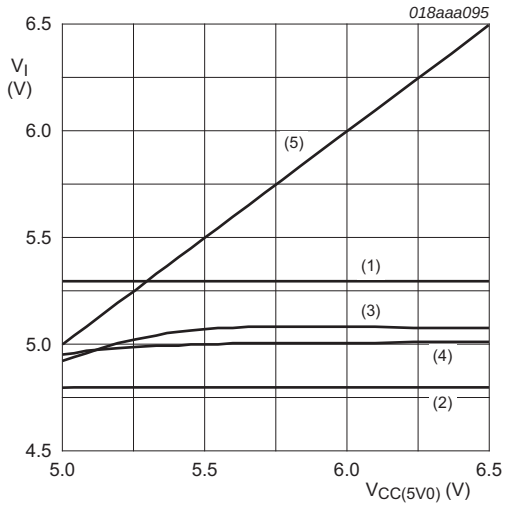
t_p = 100 ns; TLP; signal pins; typical values

Fig 12. Dynamic resistance with positive clamping



t_p = 100 ns; TLP; signal pins; typical values

Fig 13. Dynamic resistance with negative clamping



(1) 5.3 V; maximum values; HDMI CTS TID 7-11

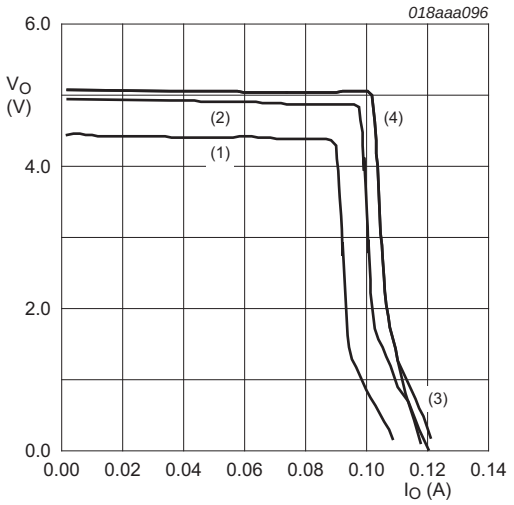
(2) 4.8 V; minimum values; HDMI CTS TID 7-11

(3) I = 0 mA

(4) I = 55 mA

(5) $V_{CC(5V0)}$ supply input; 4.925 V to 6.5 V

Fig 14. Overvoltage limiter function (HDMI_5V0_CON)



(1) $V_{CC(5V0)}$ = 4.5 V

(2) $V_{CC(5V0)}$ = 5.0 V

(3) $V_{CC(5V0)}$ = 5.5 V

(4) $V_{CC(5V0)}$ = 6.5 V

Fig 15. Overcurrent limiter function (HDMI_5V0_CON)

8. AC waveforms

8.1 DDC propagation delay

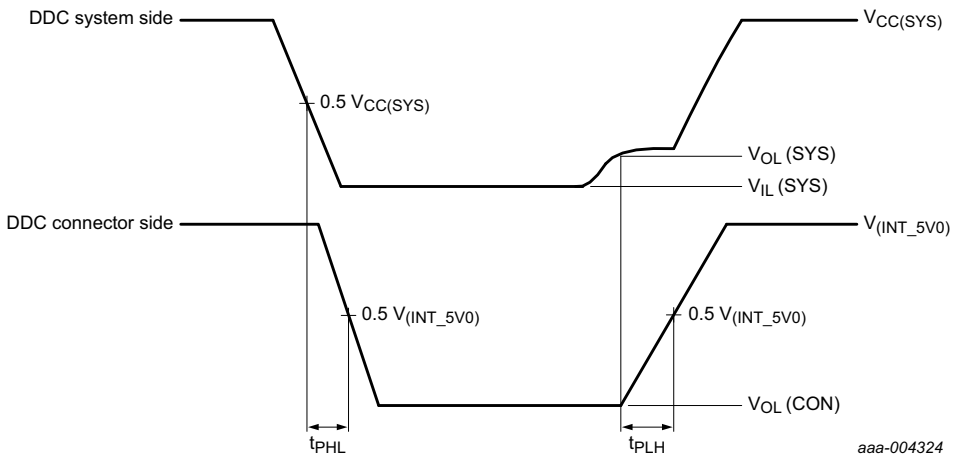


Fig 16. Propagation delay DDC, DDC system side to DDC connector side

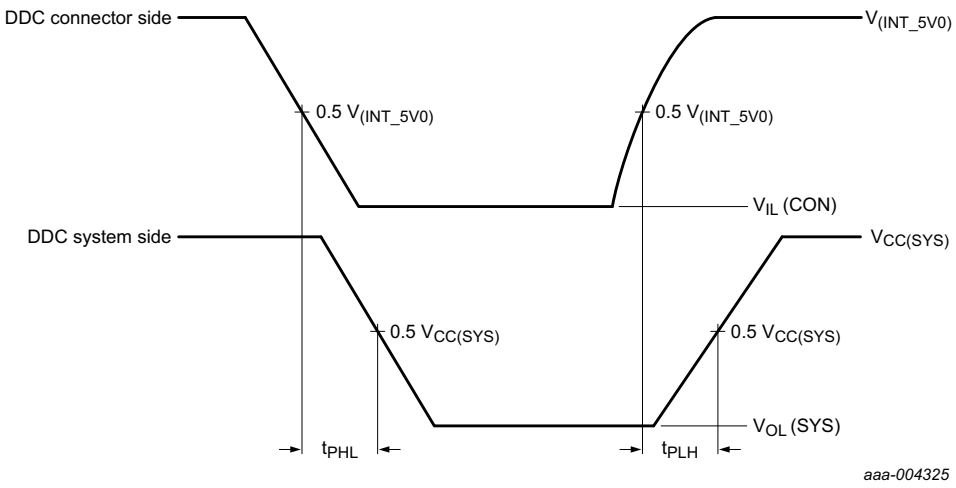


Fig 17. Propagation delay DDC, DDC connector side to DDC system side

8.2 DDC transition time

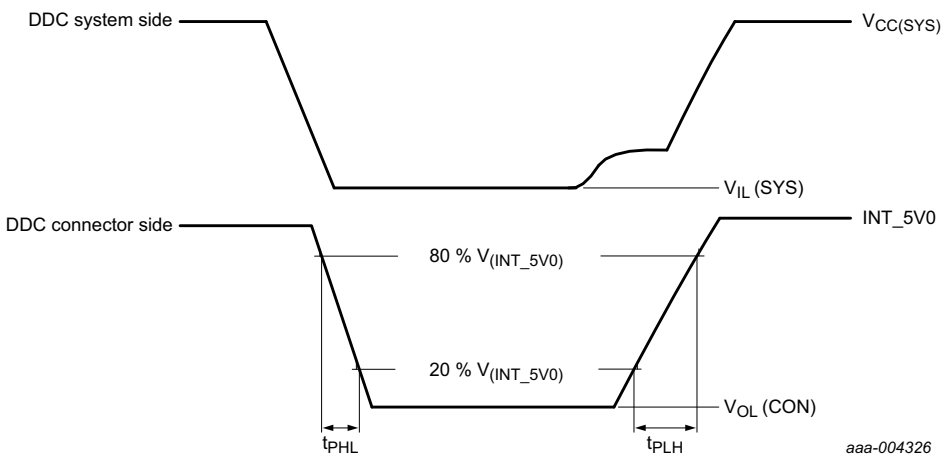


Fig 18. Transition time DDC connector side

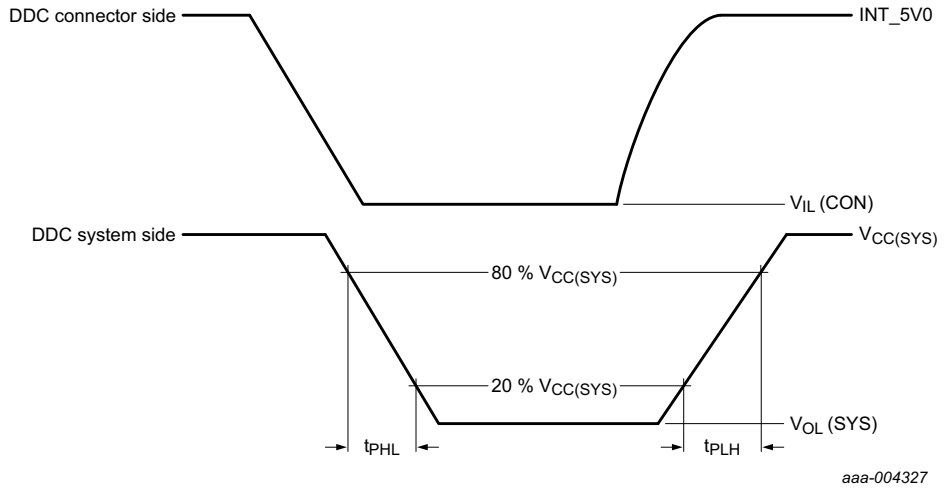


Fig 19. Transition time DDC system side

9. Application information

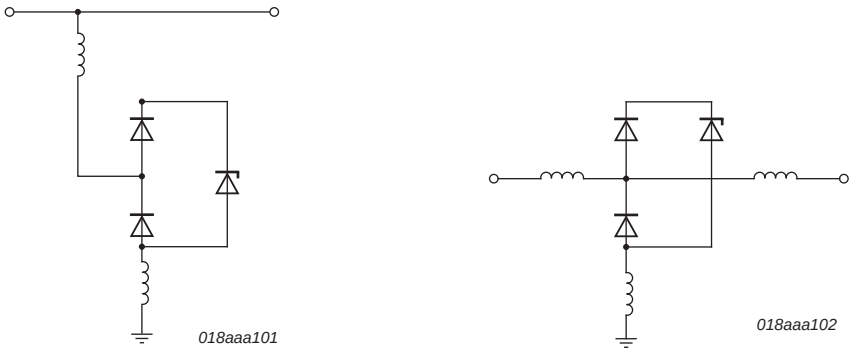
9.1 HDMI connector side ESD protection

All pins directly interfacing with the HDMI connector provide up to 12 kV contact ESD protection according to IEC 61000-4-2, exceeding level 4. In order to utilize the full scope of this protection it is recommended to connect all connector side pins to the HDMI connector.

9.2 TMDS ESD protection concept

To protect the TMDS lines and also to comply with the impedance requirements of the HDMI specification, the IP4787CZ32 provides ESD protection with matched TLC ESD structures. Typical Dual Rail Clamp (DRC) or rail-to-rail shunt structures are common for low-capacitance ESD protection (Figure 20; left side) where the dominant factor for the TMDS line impedance dip is determined by the capacitive load to ground. Parasitic lead inductances of the packaging in this case work against the ESD clamping performance by including the $\Delta I/\Delta t$ reactance of the inductance into the path of the ESD shunt.

The IP4787CZ32 utilizes these inherent inductances in series with the transmission line in order to present an effective capacitive load of roughly only 0.7 pF. This TLC structure minimizes the capacitive dip, for ideal signal integrity (Figure 20; right side) without complicated PCB pre-compensation. As a beneficial side effect, this enhances the ESD performance of the device as well, since the reactance of the series inductance attenuates the fast initial peak of the ESD pulse for a lower residual pulse delivered to the Application Specific Integrated Circuit (ASIC).



a. Classic parallel ESD shunt protection

b. Improved series shunt TLC clamping

Fig 20. TLC ESD protection of TMDS lines

9.3 Operating and standby modes

The operating mode of IP4787CZ32 depends on the availability of the $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supply voltages and on the state of the ACTIVE input signal. Without availability of both supplies, IP4787CZ32 is in Standby mode. As soon as $V_{CC(5V0)}$ and $V_{CC(SYS)}$ are within the range specified in Section 6, the part is in an operating mode that can be controlled via the ACTIVE input signal. In case ACTIVE is LOW, only the CEC buffer is active and enabled to receive or send CEC commands. All other outputs are in a high-ohmic state. A HIGH input signal enables all parts of IP4787CZ32 and puts the device into full operating mode.

Table 10. IP4787CZ32 operating modes

$V_{CC(SYS)}$	$V_{CC(5V0)}$	ACTIVE[1]	Mode	Description
< 1.1 V	< 4.5 V	X	Standby mode	all outputs high-ohmic
≥ 1.1 V	≥ 4.5 V	L	CEC Standby mode	CEC circuit active; all other outputs high-ohmic
		H	full operating mode	all functional blocks active

[1] X = Don't care (either LOW or HIGH level); L = LOW-level input; H = HIGH-level input

If no CEC Standby mode is required, or if no special Power-down modes are desired, the ACTIVE pin can be pulled HIGH to $V_{CC(5V0)}$ or $V_{CC(SYS)}$ for continuous HDMI and CEC operation as soon as the supplies are aviailable.

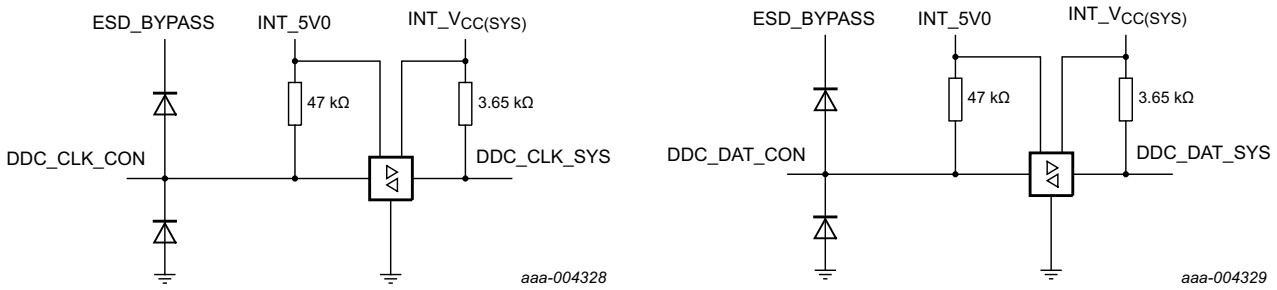
Strapping the ACTIVE = $V_{CC(SYS)}$ = V_{DD} of ASIC guarantees that all interface signals ending with the suffix '_SYS' on the system side are disabled when $V_{CC(SYS)}$ goes LOW, protecting the ASIC I/O signals from exceeding its local V_{DD}. In this mode, even if $V_{CC(5V0)}$ is powered, HDMI_5V0_CON goes active and hot plug events can be detected only when the ASIC power supply rail is on.

Strapping ACTIVE = $V_{CC(5V0)}$ is the most basic configuration where the buffers are enabled whenever the local $V_{CC(5V0)}$ and $V_{CC(SYS)}$ supplies reach minimum operating levels.

9.4 DDC circuit

The DDC bus circuit integrates all required pull-ups, and provides full capacitive decoupling between the HDMI connector and the DDC bus lines on the PCB. The capacitive decoupling ensures that the maximum capacitive load is well within the 50 pF maximum of the HDMI specification. No external pull-ups or pull-downs are required.

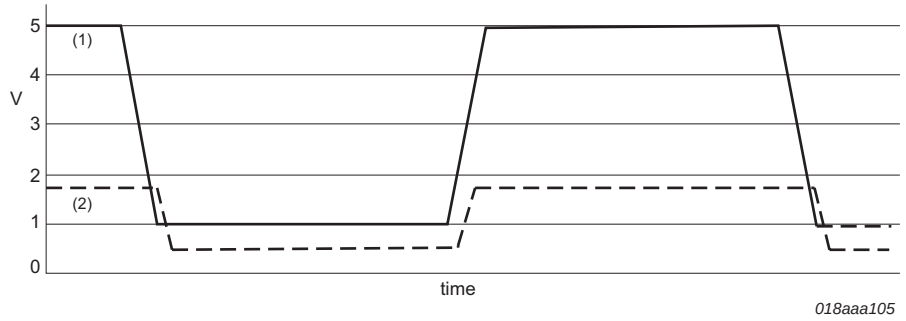
The bidirectional buffers support high-capacitive load on the HDMI cable-side. Various non-compliant but prevalent low-cost cables have been observed with a capacitive load of up to 6 nF on the DDC lines, far exceeding the 700 pF HDMI limit. The IP4787CZ32 can easily decouple this from the weaker ASIC I/O buffers, and drive the rogue cable successfully.



a. DDC clock

b. DDC data

Fig 21. DDC circuit



(1) Valid I^2C signaling example on the cable (connector side) from 5 V (HIGH) to approximately 1 V (LOW).

(2) Valid logic-level signaling example to the ASIC (system side) from 1.8 V (HIGH) to approximately 0.5 V (LOW).

Fig 22. DDC level shifting waveform example

9.5 CEC circuit

The logical multidrop topology of the CEC bus can include complex physical stubs, loading cables, and interconnects that may deteriorate signal quality.
The IP4787CZ32 includes a full bidirectional buffer to drive the CEC bus and isolate the CEC microcontroller or ASIC General-Purpose Input/Output (GPIO).

The CEC buffer derives power from an on-board 3.3 V regulator from the 5 V power domain (see Figure 23). This allows extensive system power management configurations and guarantees an HDMI-compliant $V_{(CEC\_CON)}$ on the connector, as well as a backdrive-protected 125 μA nominal CEC pull-up which does not degrade the bus when powered down.

By placing the CEC microcontroller and either $V_{CC(5V0)}$ or HDMI_5V_CON input on a 5 V rail as shown in Figure 28, the CEC microcontroller can communicate over CEC for power commands, and then enable the HDMI port via the ACTIVE pin, as well as the rest of the system as needed.

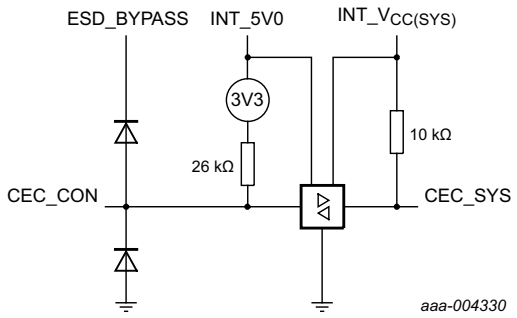
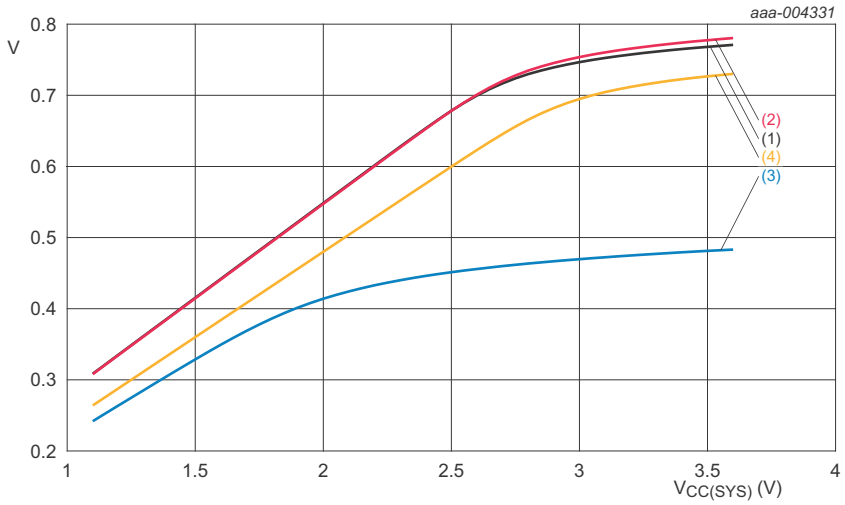


Fig 23. CEC module

9.6 Logic low I²C voltage shifter

The DDC buffers provide an additional feature commonly required for high-integration HDMI ASICs which are limited to CMOS or LVTTL LOW-level input voltage (V_{IL}) on their available I/O buffer cells. These I/Os are not strictly compliant with the 0.3 V_{DD} threshold voltage levels of I²C and may miss intended logic LOW levels on the cable between 0.8 V and 1.5 V (typical values).

This feature is also included in the CEC buffer thus allowing standard I/O buffer cells to be used in ASICs and microcontrollers connected to CEC_SYS.



(1) $V_{OL\_CEC(max)}$ maximum output voltage driven to system (ASIC) side when CEC is logic LOW

(2) $V_{OL\_DDC(max)}$ maximum output voltage driven to system (ASIC) side when DDC is logic LOW

(3) $V_{IL(max)}$ maximum input voltage on system (ASIC) side to drive DDC or CEC logic LOW

(4) $V_{IH(min)}$ minimum input voltage on system (ASIC) side to drive DDC or CEC logic HIGH

Fig 24. Logic voltage thresholds as a function of supply voltage; on connector (HDMI) side

9.7 Hot plug circuit

The IP4787CZ32 includes a hot plug drive circuit that simplifies the hot plug application. It drives an HDMI-compliant hot plug signal to the HDMI sink. By design, the hot plug drive circuit avoids glitches or short pulses on the hot plug line and is protected against shortage to the 5 V input.

In order to signal a HIGH level on the HOTPLUG_CON output pin, the HOTPLUG_CTRL input pin needs to be driven HIGH and a 5 V supply needs to be available on HDMI_5V0_CON. Driving HOTPLUG_CTRL LOW generates a LOW-level output on the HOTPLUG_CON pin. An integrated 100 kΩ resistor on the HOTPLUG_CTRL pin prevents from undefined (floating) state on HOTPLUG_CON.

In full accordance with the HDMI specification, the LOW and HIGH output levels generated on the HOTPLUG_CON output always show a proper impedance of 1 kΩ.

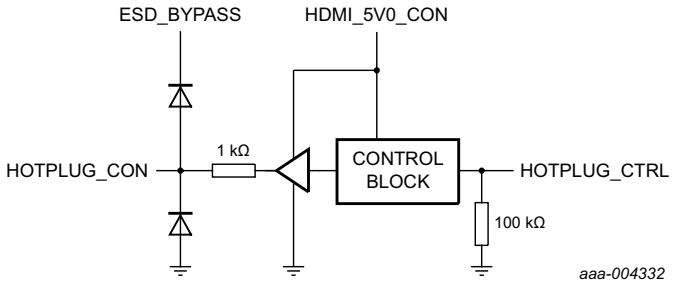


Fig 25. Hot plug circuit

9.8 HEAC support and utility pin

In addition to the ESD protection implemented at UTILITY_CON, IP4787CZ32 also includes a biasing output for HEAC functionality. This output buffer is closely tied to the output on the HOTPLUG_CON pin. A LOW-level output signal on HOTPLUG_CON also causes a low output on UTILITY_CON and a HIGH level on HOTPLUG_CON results in an identical high output on UTILITY_CON.

As for HOTPLUG_CON, the LOW and HIGH output levels generated on the UTILITY_CON output always show an impedance of 1 kΩ.

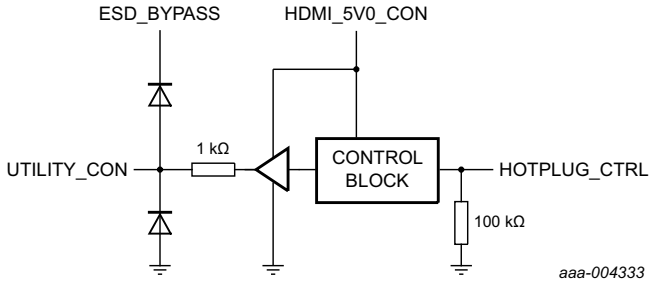


Fig 26. Utility circuit

9.9 EDID programming using ENABLE_LDO

IP4787CZ32 has a special mode providing an internal 5 V supply to the connector side power supply. This special mode allows programming of an Extended Display Identification Data Programmable Read-Only Memory (EDID PROM) placed on DDC bus between the device and the HDMI connector.

The EDID programming mode can be utilized by driving an active HIGH signal to the ENABLE_LDO input pin. This enables an internal 5 V Low DropOut (LDO) to provide the supply on $V_{CC(5V0)}$ to HDMI_5V0_CON pin in case no higher supply is available at this pin. An active LOW input to ENABLE_LDO disables the EDID programming mode.

9.10 Backdrive protection

The HDMI connector contains various signals which can partly supply current into an HDMI device that is powered down.

Typically, the DDC lines and the CEC signals can force significant current back into the powered-down rails as shown in Figure 27, causing power-on reset problems with the system, and possible damage. The IP4787CZ32 prevents this backdrive condition whenever the I/O voltage is greater than the local supply.

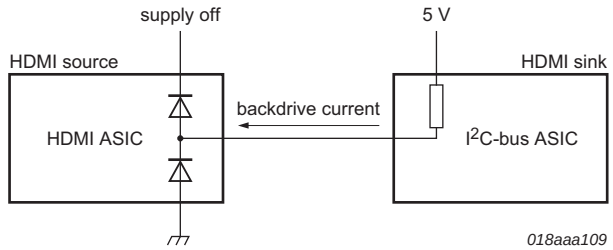


Fig 27. Generalized backdrive protection

9.11 Schematic view of application

Only a single external component (C_O = 1 µF) is required to protect and interface the ASIC to a complete and compliant HDMI port. The 100 nF ESD bypass capacitor is optional.

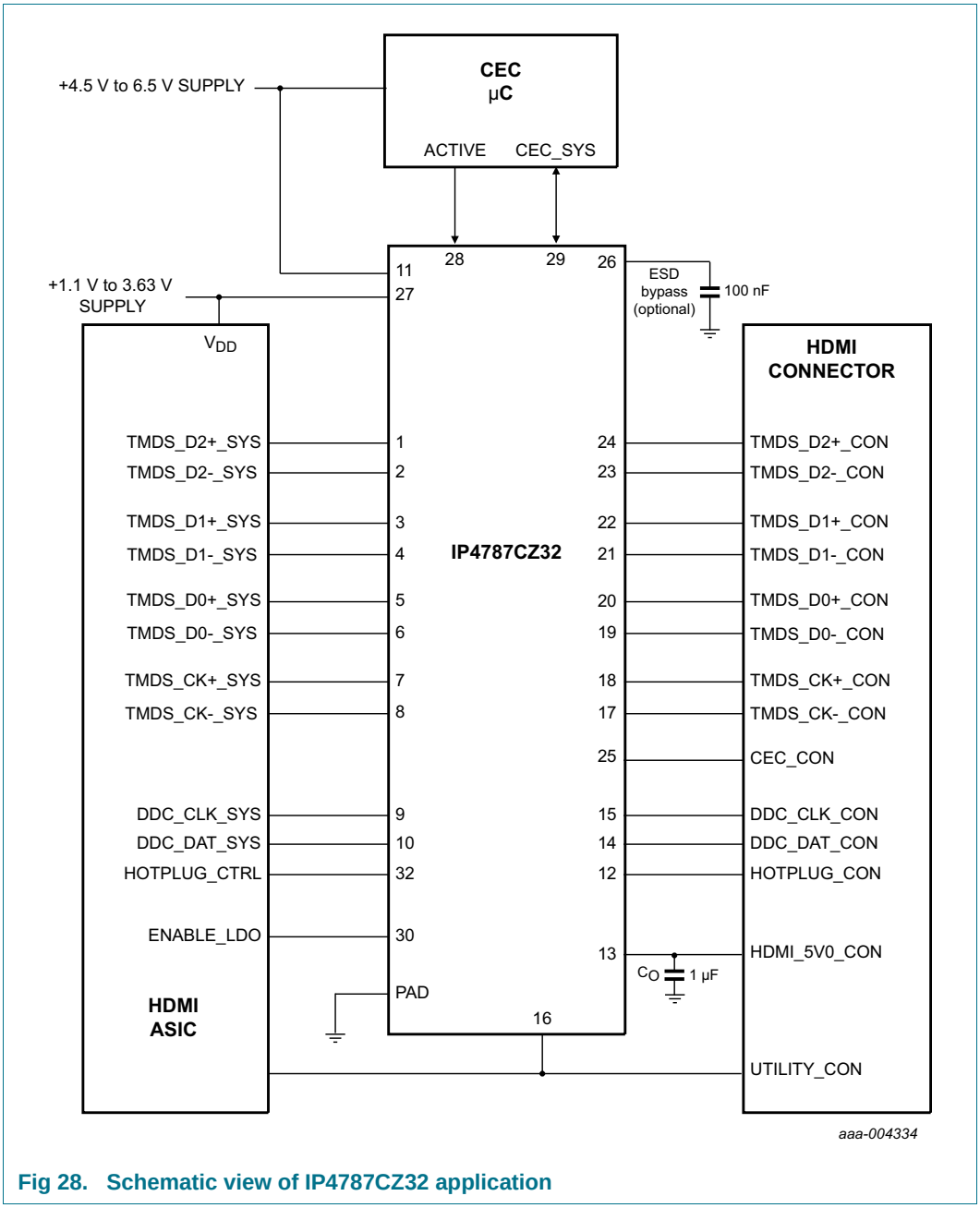


Fig 28. Schematic view of IP4787CZ32 application

9.12 Typical application

The IP4787CZ32 is designed to simplify routing to the HDMI connector, and ease the incorporation of high-level ESD protection into delicately balanced high-speed TMDS lines. These lines rely on tightly controlled microstrip or stripline transmission lines with minimal impedance discontinuities, which can deteriorate return loss, increase deterministic jitter and generally erode overall link signal integrity.

Normally, when designing a PCB with standard shunt ESD clamps, careful consideration must be given to manual pre-compensation of the additional load of the added ESD component. With the IP4787CZ32 TLCs, the ESD suppressor is designed to maintain the characteristic impedance of the PCB microstrip or stripline. Therefore the designer has to be concerned only with the standard-controlled impedance of the unloaded PCB lines. This simplifies the task of the PCB designer, and minimizes the tuning cycles, which are sometimes required when pre-compensation misses the mark. A basic application diagram for the ESD protection of an HDMI interface is shown in Figure 29 for a type-A HDMI connector.

The optimized HVQFN32 pinning simplifies the PCB design to keep the ESD protection close to the connector where it can minimize the coupling of the ESD pulse onto other lines in the system during a strike.

Due to the integrated pull-up and pull-down resistors, only two external capacitors are required to implement a fully compliant HDMI port.

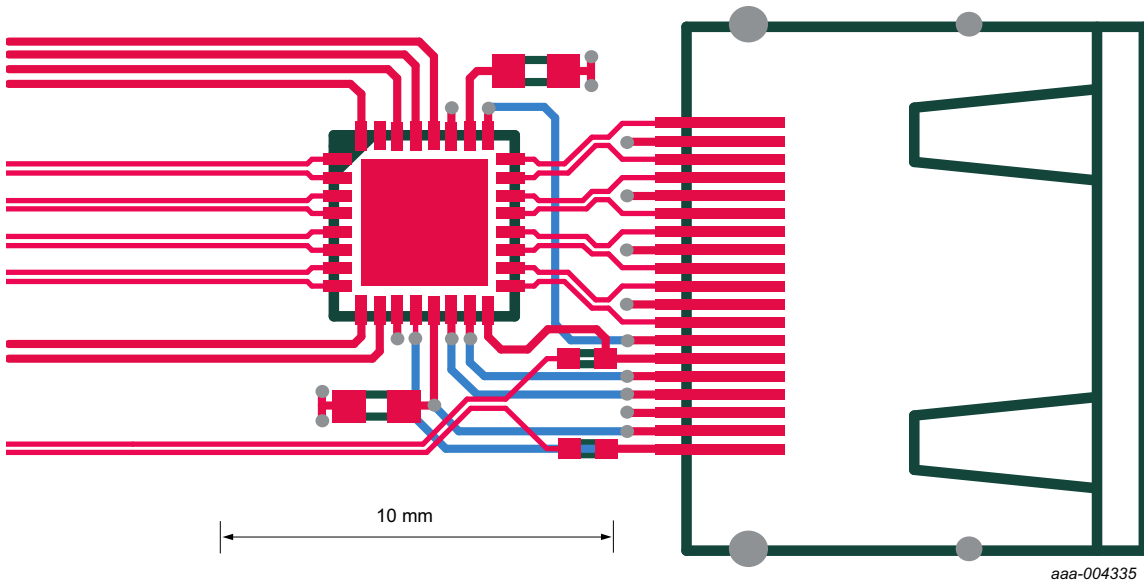
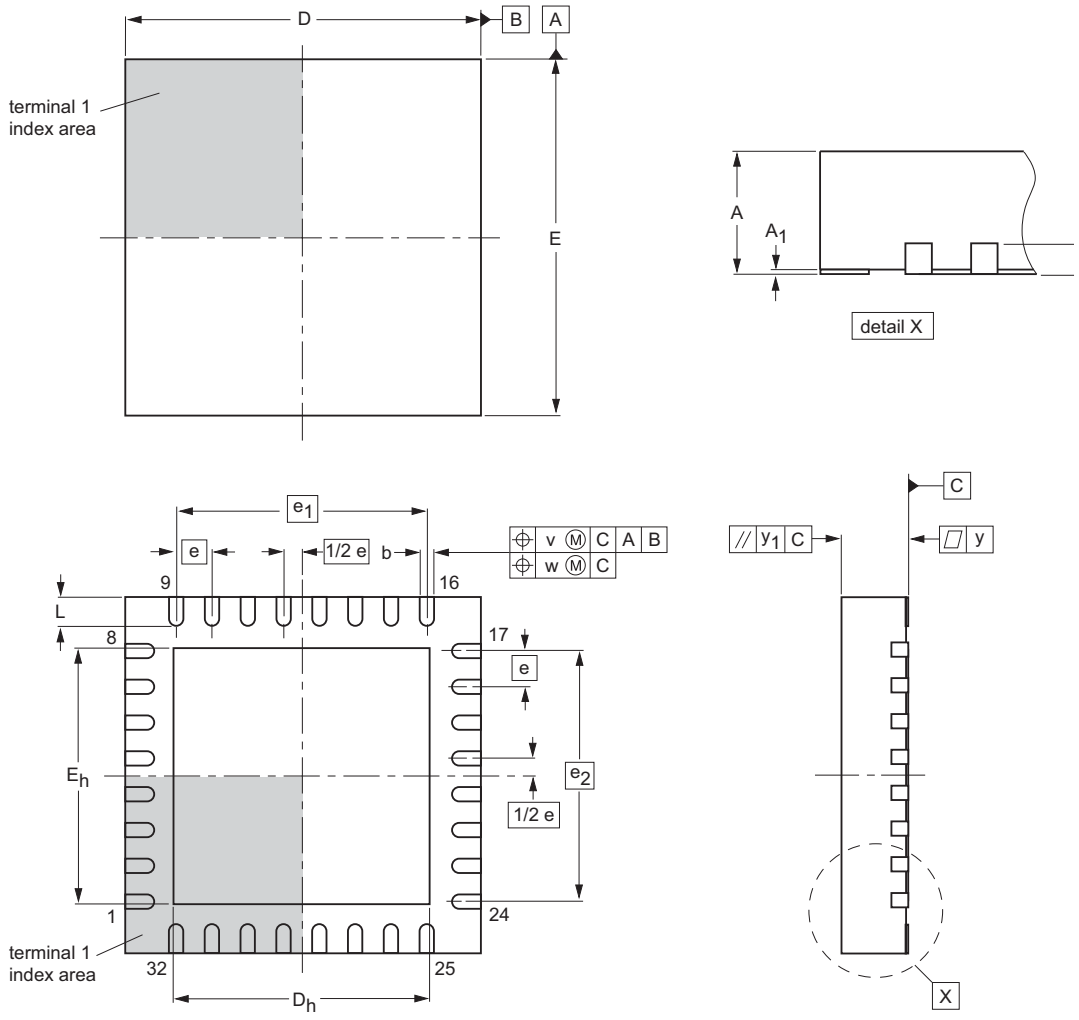


Fig 29. Application of the IP4787CZ32 showing optimized HDMI type-A connector routing

10. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit(1)		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 30. Package outline SOT617-3 (HVQFN32)

11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 31) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020D)

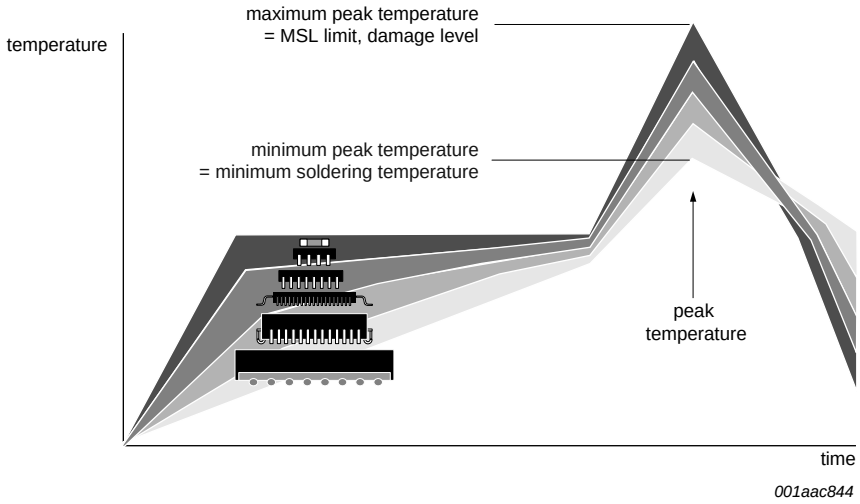
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 31.



MSL: Moisture Sensitivity Level

Fig 31. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

12. Glossary

HDMI sink — Device which receives HDMI signals for example, a TV set.

HDMI source — Device which transmits HDMI signal for example, DVD player.

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4787CZ32 v.3	20141219	Product data sheet	-	IP4787CZ32 v.2
Modifications:	• Added support for HDMI 2.0 display modes and updated ESD robustness			
IP4787CZ32 v.2	20121220	Product data sheet	-	IP4787CZ32 v.1
IP4787CZ32 v.1	20120730	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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