CRD5381

Audio A/D Converter w/ Asynchronous Decimation Filter Reference Design

Features

Analog Performance

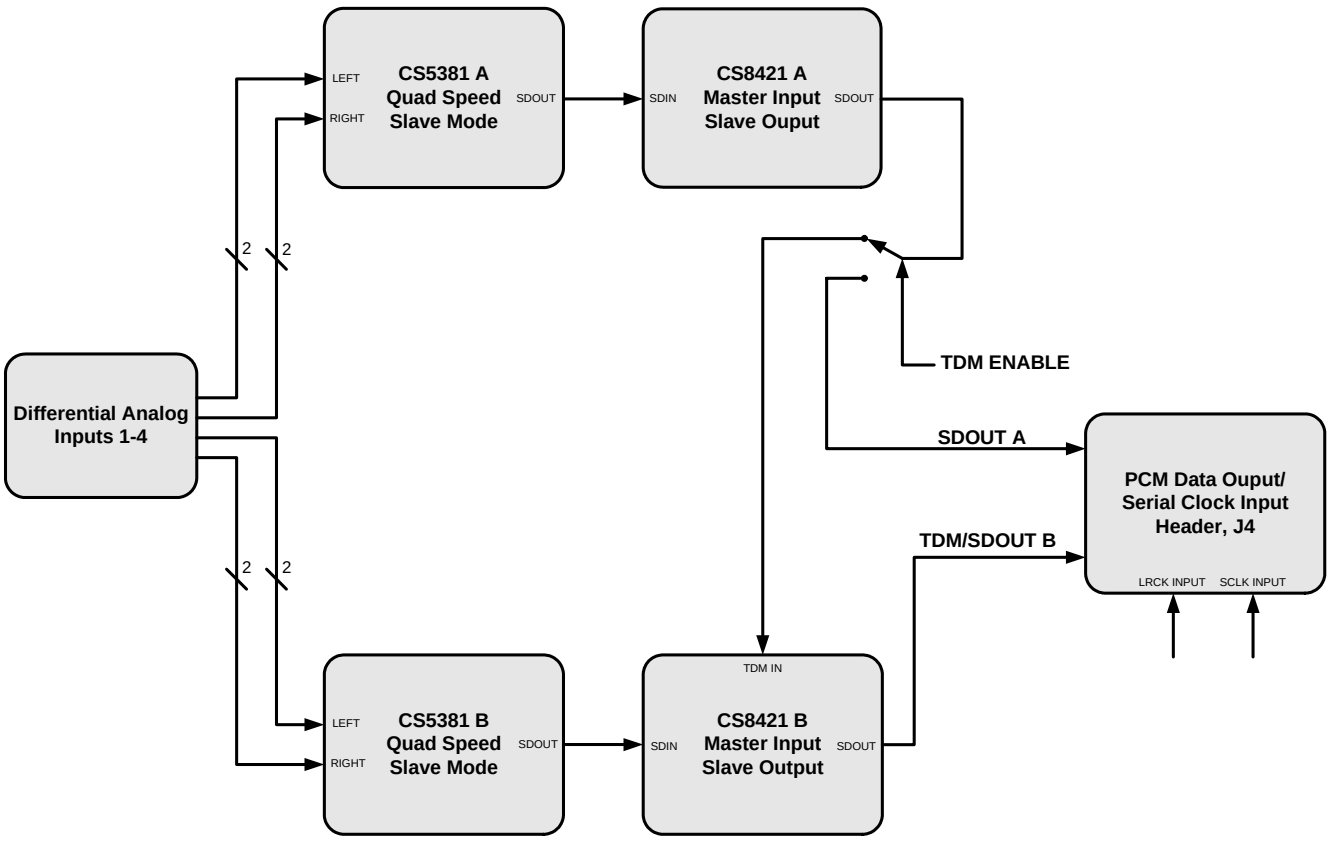
- Advanced Multi-bit Delta-sigma Architecture
- 24-bit Conversion
- 120 dB Dynamic Range
- -110 dB THD+N
- Performance insensitivity to Input Clock Jitter

Digital Filter Characteristics

- 125 dB Stop-band Rejection
- Phase-Matched Outputs

System Features

- Output Sample Rate Determined by Input Word, Left/Right, or Fsync Clock
- No External Master Clock Required
- Easily Scalable for Additional Channels
- Sample Rates from 27 kHz to 192 kHz
- Four-Channel Time-Division Multiplexed Output
- Two Independent Stereo, Left-Justified Outputs



Description

The combination of the CS5381 Analog-to-Digital Converter and CS8421 Asynchronous Sample Rate Converter creates an analog-to-digital conversion system with an asynchronous digital decimation filter that is virtually immune to interface or network jitter. In addition, the CS8421 adds a multi-channel Time Division Multiplexed (TDM) output format option. These unique features address many of the issues and design challenges associated with networked audio systems and other high-performance applications. In addition to the standard 24-bit audio data, the CS8421 adds the functionality to output properly dithered 32, 20, or 16-bit data.

The CRD5381 was designed as a platform for easy evaluation of the jitter rejection, sample rate conversion, and time-division multiplexing capabilities of the CS8421 in the context of a A/D conversion system with an asynchronous decimation filter. The CRD5381 accepts four channels of balanced, analog audio input and provides four channels of PCM data output. The data output can be either a four-channel TDM format or two independent stereo left-justified data outputs. The PCM data output is synchronous to the serial left-right clock and bit clock that the user supplies. The CRD5381 also provides status indicators including ADC overflow and SRC unlock, and it accepts an external reset signal. The only system power requirements for the design include +/- 12 Volts and +3.3 Volts. The required input signals are a left/right or word clock and serial clock for the audio data output.

This document includes operational instructions and schematics for the CRD5381 and is a companion document to the Cirrus Logic applications note AN270, “Audio A/D conversion with Asynchronous Decimation Filter” [1]. Please also refer to the CS5381 and CS8421 data sheets for specific product information and specifications [2,3]. Both documents, as well as AN270, are available online at *http://www.cirrus.com*

The CRD5381 schematic set is shown in Figures 9 through 14 and the board layout is shown in Figures 15 through 19. A block diagram of the CRD5381 is shown in Figure 8.

ORDERING INFORMATION

Product	Description	Order#
CRD5381	Audio A/D Converter w/ Asynchronous Decimation Filter Reference Design	CRD5381

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1.1 Sample Clock Domain

1.1.1 CS8421 Input Operational Mode

Serial Audio Interface - Left-Justified. The selection of the serial audio interface format is arbitrary, assuming the serial input format of the CS8421 is in agreement with the serial output format of the CS5381. The selection of the serial audio format is done by connecting a resistor (1.96 kΩ in this application) to either ground or the VL supply.

System Clocking - Master mode, LRCK = MCLK/128. In this mode, the CS8421 generates the Serial and Left/Right clocks within the sampling clock domain. This mode is selected by the resistor connected to the MS_SEL pin of the CS8421. In this application the MS_SEL pin is connected to ground (equivalent to connecting a 1 kΩ resistor to ground).

1.1.2 CS5381 Operational Mode

Serial Audio Interface - Left-Justified. The selection of the serial audio interface format is arbitrary, assuming the input format of the CS8421 is in agreement with the output format of the CS5381.

System Clocking - Slave mode. In this application the CS8421 generates the serial and Left/Right clocks within the sampling clock domain.

Operational Mode or Sample Rate Range - Configured for Quad-Speed Mode to support sample rates above 100 kHz.

High Pass Filter - Enabled

Master Clock Divide - Enabled to divide the master clock by 2.

1.1.3 Master Clock Frequency Generation

The CS8421 uses the clock supplied through its XTI pin as its master clock (MCLK). The CS5381 also uses this signal as its master clock (through the MCLK pin). Alternatively, the CS8421 can generate a master clock (via the MCLK_OUT pin) by connecting a crystal across its XTI-XTO pins, which can supply a MCLK to the CS5381.

In this application, MCLK_OUT pin is not being used and is pulled high through a 47 kΩ resistor to VL to disable it. If a crystal is not being used, as with the crystal oscillator in this application, XTO should be left unconnected or pulled low through a 47 kΩ resistor to ground.

1.1.4 Maximum Sample Rate

The maximum sample rate is limited by the maximum allowable master clock frequency of the CS8421, which is 27 MHz. The sample rate is this clock frequency divided by 128. This corresponds to a maximum sample rate of 210.937 kHz within the sample clock domain. In this application, we have chosen a master clock frequency of 25 MHz, which corresponds to a sample rate of approximately 195.312 kHz

1.1.5 Synchronization of Multiple Sections

In this application multiple CS8421 inputs are set to master mode, and it is important that their serial ports be aligned in time, with minimum possible phase error. To achieve this, their reset signals are tied together and routed for minimum skew. The amount of deviation between ILRCKs generated by the respective parts is typically either 0 or 1 master clock period, or between 0 and 40 ns.

1.2 CS8421 Output and the Interface Clock Domain

1.2.1 CS8421 Output System Clocking

The CS8421 serial output is configured as a system clock slave. The advantages are:

- Output sample rate is dependent on the frequency of the incoming word clock (OLRCK), set by the user.
- Outputs of multiple CS8421 devices are synchronous.
- Multiple devices can be configured in a Time Division Multiplexed (TDM) multi-channel interface format.

As mentioned in “CS8421 Input Operational Mode” on page 4, the input of the CS8421 is configured as a master, with the master clock frequency = 128*Fsi (or ILRCK). To accommodate this serial input mode, and to set the serial output to slave, the MS_SEL pin is connected to +3.3 V.

1.2.2 Serial Audio Output Port Options and Selection of Data Resolution and Dither

The CS8421 provides multiple options for the serial audio output port. These options include:

- Output Data Format of Left-Justified, Right-Justified, I²S or TDM
- Audio output data resolution of the SRC can be set to 16, 20, 24, or 32-bits. Dithering is applied and is automatically scaled to the selected output word length. This dither is not correlated between left and right channels.

Output word-length and serial data format are selected with either a pull-up or pull down resistor connected to the SAOF pin of the CS8421. Please refer to Table 3 in the CS8421 data sheet for details [3].

The serial audio output of the CRD5381 is configured to operate in either dual 24-bit Left-Justified formats or a 4-channel 24-bit TDM output.

1.2.3 Clocking

In order to ensure proper operation of the CS8421, the clock or crystal attached to XTI must simultaneously satisfy the requirements of LRCK for both the input and output as follows:

- If the input is set to master, Fsi ≤ XTI/128 and Fso ≤ XTI/130.
- If the output is set to master, Fso ≤ XTI/128 and Fsi ≤ XTI/130.
- If both input and output are set to slave, XTI ≥ 130*[maximum(Fsi,Fso)], XTI/Fsi < 3750, and XTI/Fso < 3750.

In the example application in this data sheet, the input serial port is set to master, and generates serial clocks for a sampling rate of XTI/128. The output serial port is set as slave, and can receive a left-right clock that is ≤ XTI/130. The serial bit-clock frequency is always 64*left-right clock.

1.2.4 SRC Locking and Varispeed

The SRC calculates the ratio between the input sample rate and the output sample rate, and uses this information to set up various parameters inside the SRC block. The SRC takes approximately 4200/Fso (8.75 ms at Fso of 48 kHz) to make this calculation.

The SRC_UNLOCK pin is used to indicate when the SRC is not locked. When $\overline{\text{RST}}$ is asserted, or if there is a change in Fsi or Fso, SRC_UNLOCK will be set high. The SRC_UNLOCK pin will continue to be high until the SRC has reacquired lock and settled, at which point it will transition low. When the SRC_UNLOCK pin is set low, SDOUT is outputting valid audio data. This can be used to signal a DAC to un-mute its output.

1.2.5 Latency or Group Delay

The system latency, or group delay, is the sum of the CS5381 group delay and the CS8421 group delay. The latency of the CS5381 is 5 samples (5/Fs), and the latency of the CS8421 depends on input and output sample rates, and can be found in the CS8421 data sheet [3]. Table 1 shows the combined group delay for typical output sample rates with a fixed input sampling rate of 195.3125 kHz.

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Output Sample Rate	Group Delay
48 kHz	1.48 ms
96 kHz	.895 ms
192 kHz	.605 ms

Table 1. System Latency

1.2.6 Phase Matching Between Multiple Sections

This phase delay is equal across multiple parts. Therefore, when multiple parts operate at the same Fsi and Fso and use a common XTI/XTO clock, their output data is phase matched.

1.3 Filter Response

The transition-band response of the CRD5381 is due to the combination of the digital filtering performed by both the CS5381 and the CS8421. Due to the superior stop-band rejection of the CS8421, the combination of the two parts yields a better stop-band rejection then the CS5381 alone. When the output sample rate is close to that of the CS5381, signals that fall within the transition-band spectrum will already have been aliased down into the pass-band prior to the CS8421's output filter. This can be seen in Figure 3 on page 8, where the signals above the notch at approximately 97.5 kHz represent signals that have been aliased downward prior to the action of the CS8421 output filter.

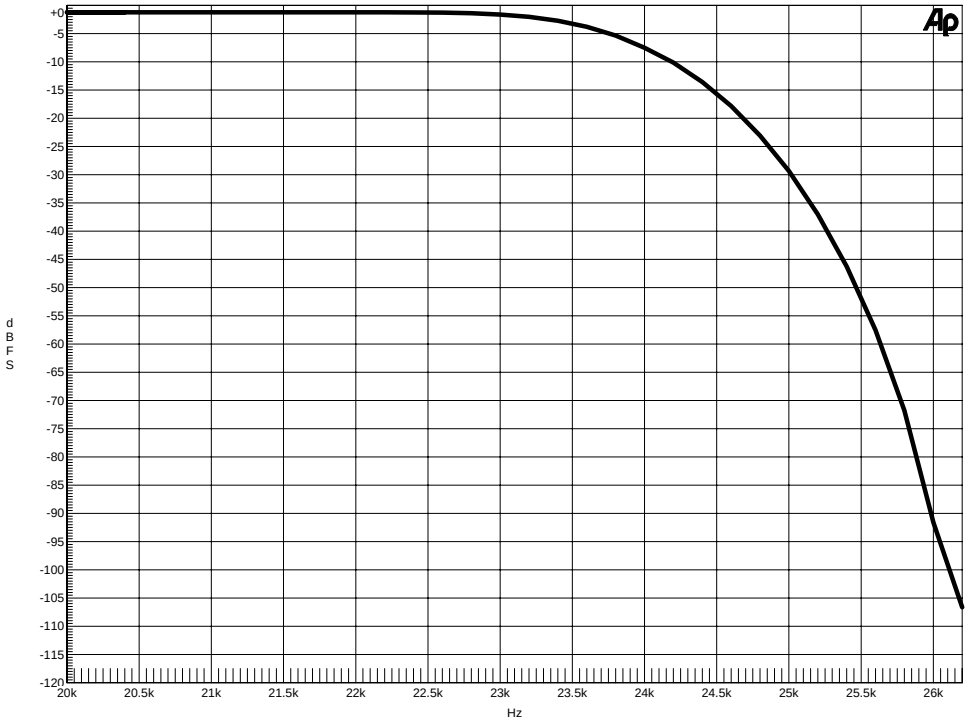

Figure 1. Transitional Band, 48 kHz Out

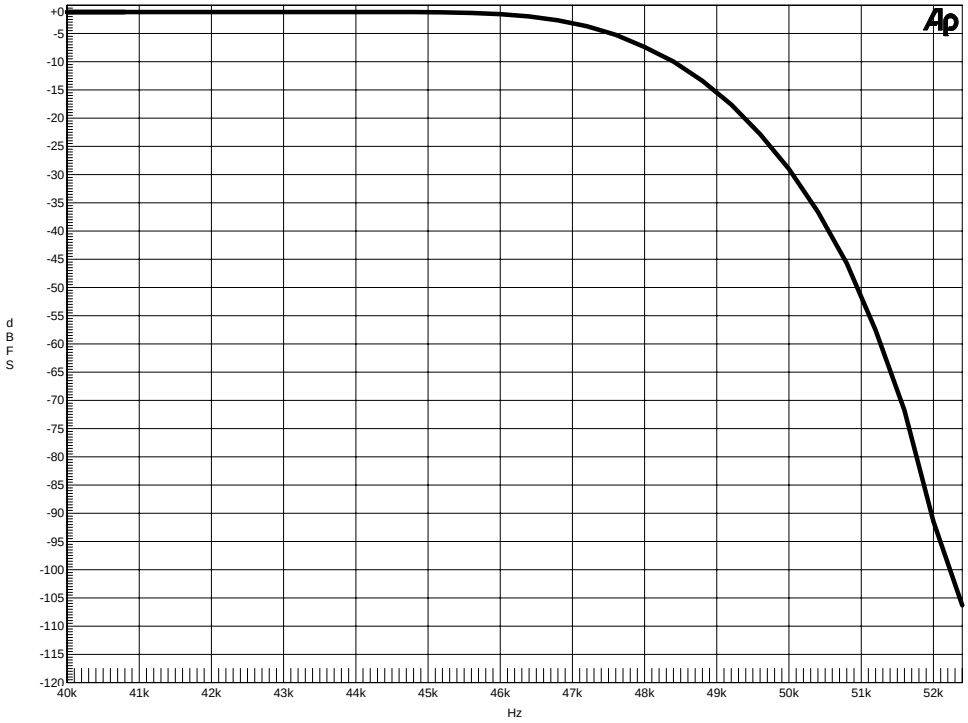

Figure 2. Transitional Band, 96 kHz Out

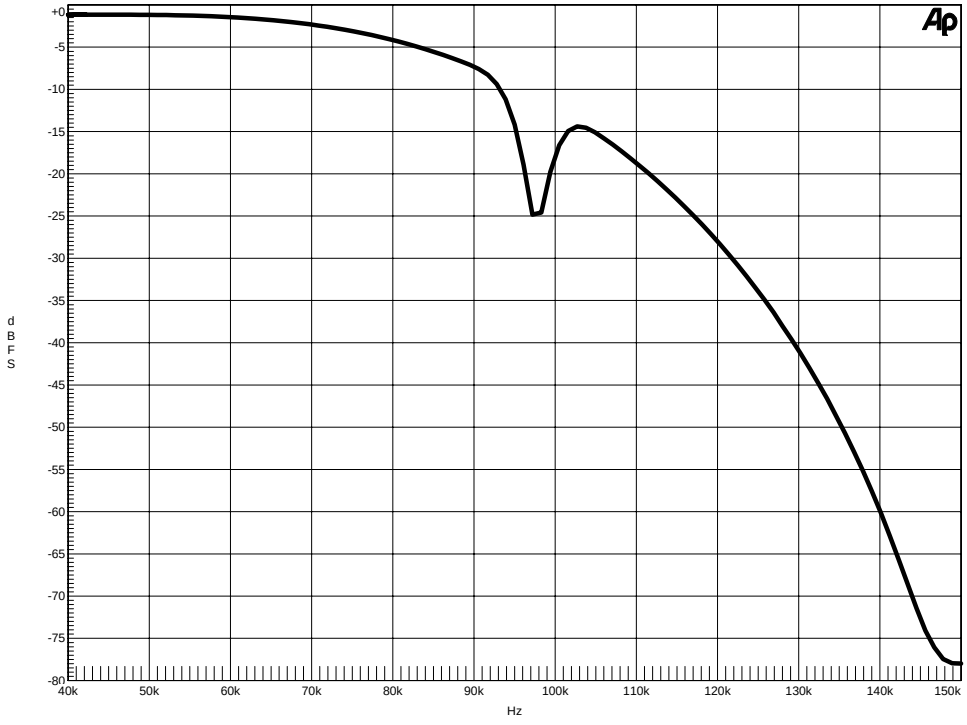

Figure 3. Transitional Band, 192 kHz Out

2. OPERATION

2.1 Sample Rate

Sampling Clock Domain - The Sampling clock domain includes the CS5381 A/D converter and the serial audio input to the CS8421 SRC. The sampling frequency in this clock domain is dictated by the ILRCK frequency of each CS8421, and is derived from the system master clock Y2. The sample rate within this clock domain is fixed at 195.312 kHz.

Interface Clock Domain - The Interface clock domain includes the output of the CS8421 SRC. The sample rate of this domain is dictated by the frequency of the Left/Right or Word clock. This signal is an input to the system and must be applied by the user through header J4.

2.2 Audio Data Output Format Selection

The CRD5381 allows selection of either a standard Left-Justified 3-wire serial audio interface with separate data lines for each ADC / SRC pair or a 4-channel TDM interface. Selection of either mode is accomplished via jumper J8. The two possible serial audio output formats are shown in Figures 4 and 5.

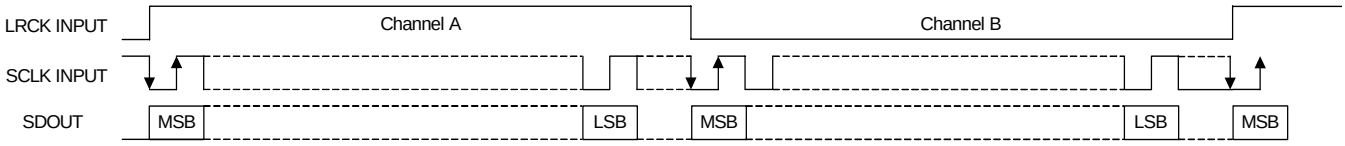

Figure 4. Left-Justified Serial Audio Interface

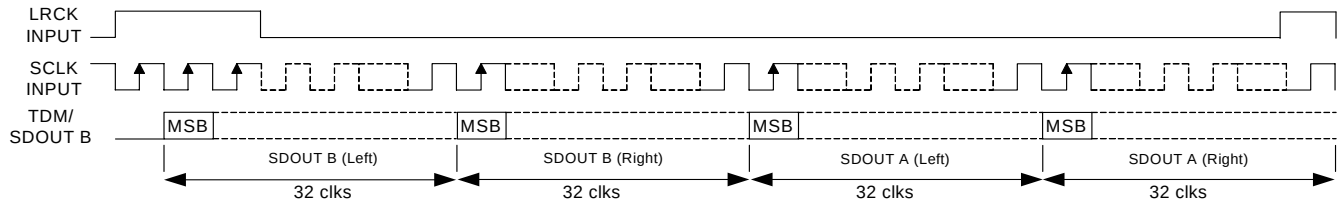

Figure 5. TDM Audio Interface

2.3 System Clocking and Data I/O

Serial Clock - The Serial Clock must be applied by the user through header J4 in both Left-Justified and TDM mode. In TDM mode, Serial Clock must be 128*Left/Right Clock.

Left /Right or Word Clock - The Left/Right Clock must be applied by the user through header J4 in both Left-Justified and TDM mode. The output sample rate is determined by the frequency of this clock.

Serial Data Output - The serial data is output on J4. Separate stereo data outputs are available as SDOUT A and TDM/SDOUT B when the Left-Justified format is selected. Four-channel TDM data is available on TDM/SDOUT B (J4) when the TDM mode is selected.

Figure 4 and Figure 5 illustrate Left-Justified and TDM data structures. Please refer to the “Slave Mode Switching Specifications” on page 8 of the CS8421 data sheet for the timing requirements of both the Left-Justified and TDM modes[3].

Figure 6 illustrates the clock and data connections to J4.

Table 2 indicates the jumper options for J8 with the associated output data formats and some common clock frequencies.

J8	SDOUTA Data Format	TDM/SDOUTB Data Format	LRCK INPUT Frequency	SCLK INPUT Frequency
LJ	24-bit Left-Justified	24-bit Left-Justified	48 kHz	3.072 MHz
LJ	24-bit Left-Justified	24-bit Left-Justified	96 kHz	6.144 MHz
LJ	24-bit Left-Justified	24-bit Left-Justified	192 kHz	12.288 MHz
TDM	-	4-Channel TDM	48 kHz	6.144 MHz
TDM	-	4-Channel TDM	96 kHz	12.288 MHz
TDM	-	4-Channel TDM	192 kHz	24.576 MHz

Table 2. Clock and Data Formatting Options

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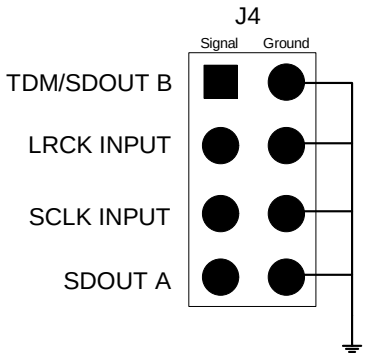

Figure 6. Clock and Data Header Connections, J4

2.4 System Status Indicators

ADC Overflow - Overflow indicators are provided for each CS5381. Overflow is indicated by the LED labeled ADC OVERFLOW A (D4) or ADC OVERFLOW B (D5) being lit. These control signals are also available as outputs on header J16, labeled OVERFLOW A and OVERFLOW B as shown in Figure 7 on page 11.

SRC Unlock - SRC unlock indicators are provided for each CS8421. SRC unlock is indicated by the LED labeled SRC UNLOCK A (D3) or SRC UNLOCK B (D2) being lit. These control signals are also available as outputs on header J16, labeled SRC UNLOCK A and SRC UNLOCK B as shown in Figure 7 on page 11.

2.5 System Reset

The CRD5381 provides an on-board reset and a connection for a user-applied reset signal through header J16.

On-board Reset - The on-board reset signal is activated either upon power-up or by pressing push-button S1. The reset signal is active-low, and is held low for approximately 350 ms after S1 has been pressed, or power has been applied to the CRD5381.

External Reset - A connection is provided for a user to apply an external reset to the CRD5381 through header J16 as shown in Figure 7 on page 11. The external reset should be an active-low, +3.3 V signal. When an external reset signal is connected to the CRD5381, the on-board reset is the logical OR of the power-up reset, the push-button reset, and the external reset.

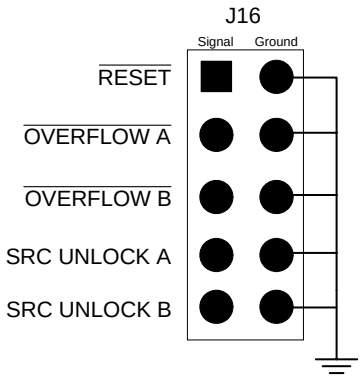

Figure 7. Status Indicator and Reset Header, J16

2.6 Analog Inputs

The CRD5381 provides four fully differential analog inputs via J9, J11, J7, and J12; shown in Figure 9 and Figure 10. Each analog input has the required analog circuitry to optimize the performance of each CS5381. The input buffer to each CS5381 device has unity gain, and the CRD5381 differential input amplitude required to generate a full-scale digital output is typically 5.65 Vpp.

If extra analog input circuitry is required in the user's design, it should drive a buffer equivalent to the contents of the dotted boxes shown in Figure 9 and in Figure 10 labeled "CS5381 Required Input Circuitry". In this case, all components outside the dotted boxes in Figure 9 and Figure 10 should be removed from the design.

2.7 Power

The CRD5381 requires the user to supply +3.3 V (J6) and ±12 V (J2 and J1) to the board. Onboard regulators supply the required +5 V and +2.5 V. All voltage inputs must be referenced to the single black banana-type ground connector (J5). Zener Diodes Z1 and Z2 (shown in Figure 14) are used to protect the CRD5381 circuitry from accidental connection of a reversed polarity supply or a supply of over ± 13 V to J1 and J2.

WARNING: Please refer to the CS5381 and CS8421 data sheet for allowable voltage levels.

2.8 Grounding and Power Supply Decoupling

The CS5381 and CS8421 require careful attention to power supply and grounding arrangements in order to optimize performance. Figure 8 provides an overview of the connections on the CRD5381; Figure 15 shows the component placement. Figure 16 shows the top layout, Figure 17 shows the bottom layout, Figure 18 shows the power plane, and Figure 19 shows the ground plane. The decoupling capacitors are located as close to the CS5381 and CS8421 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

3. BLOCK DIAGRAM

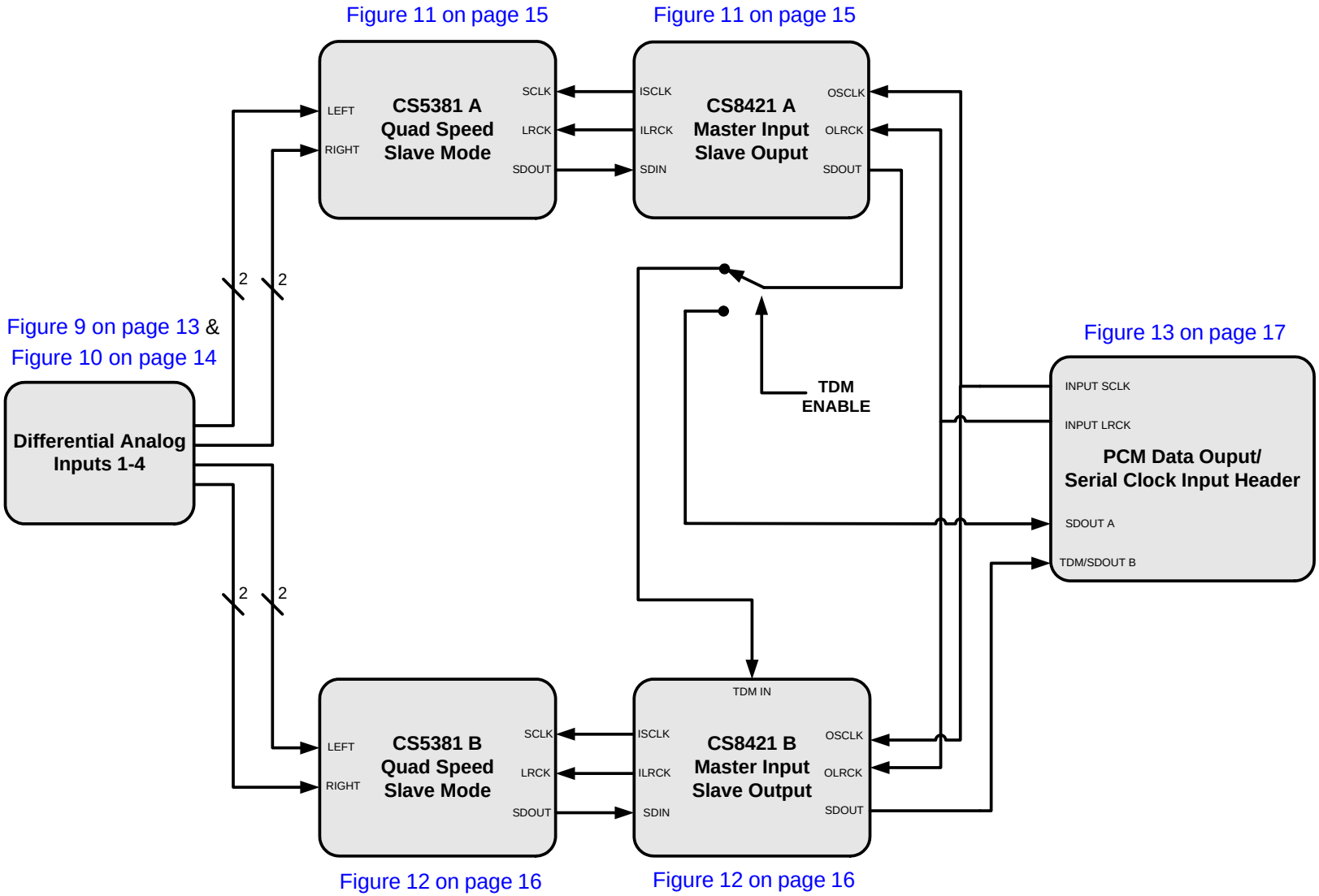

Figure 8. Block Diagram

4. SCHEMATICS

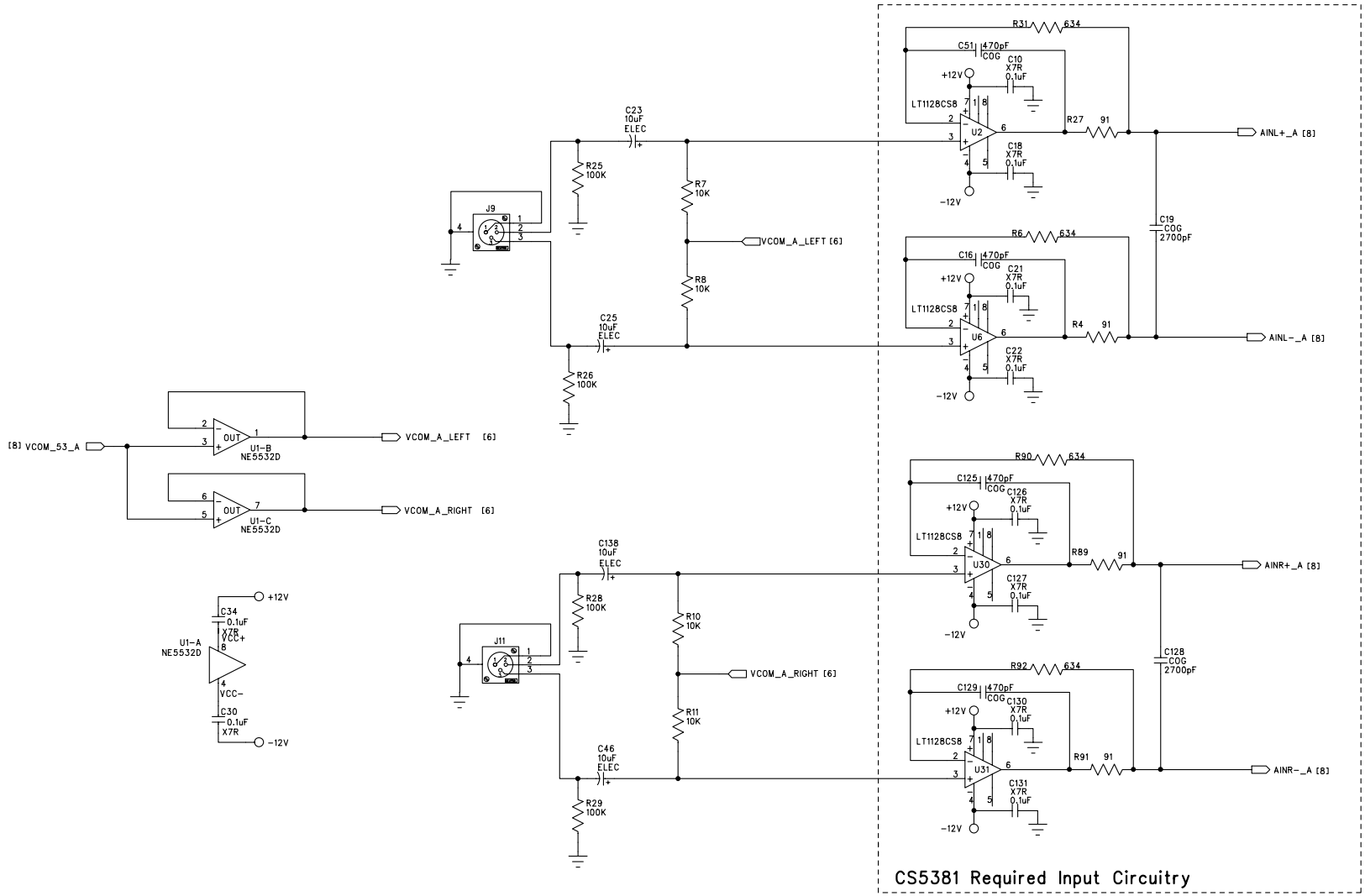

Figure 9. Analog Inputs 1 & 2

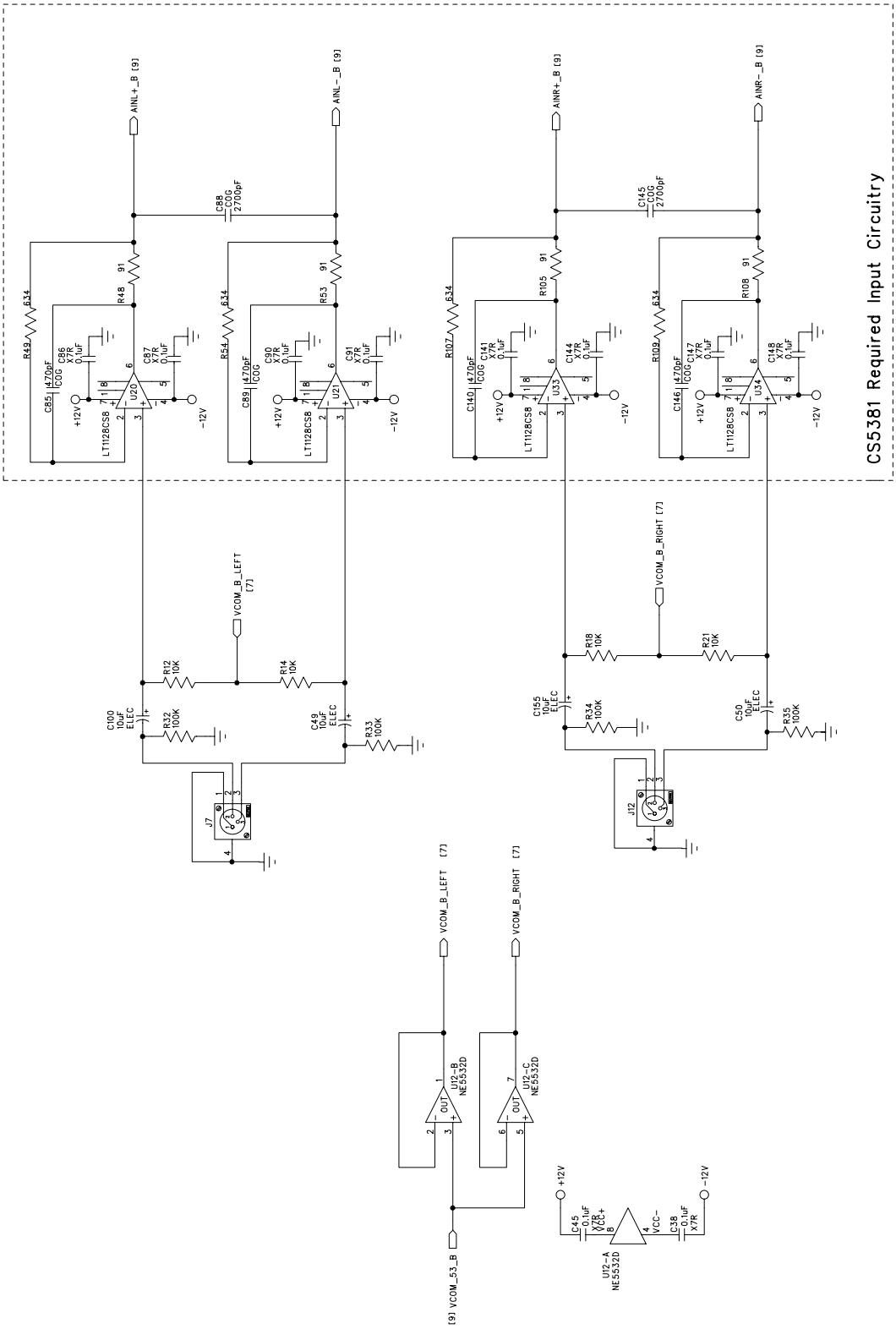

Figure 10. Analog Inputs 3 & 4

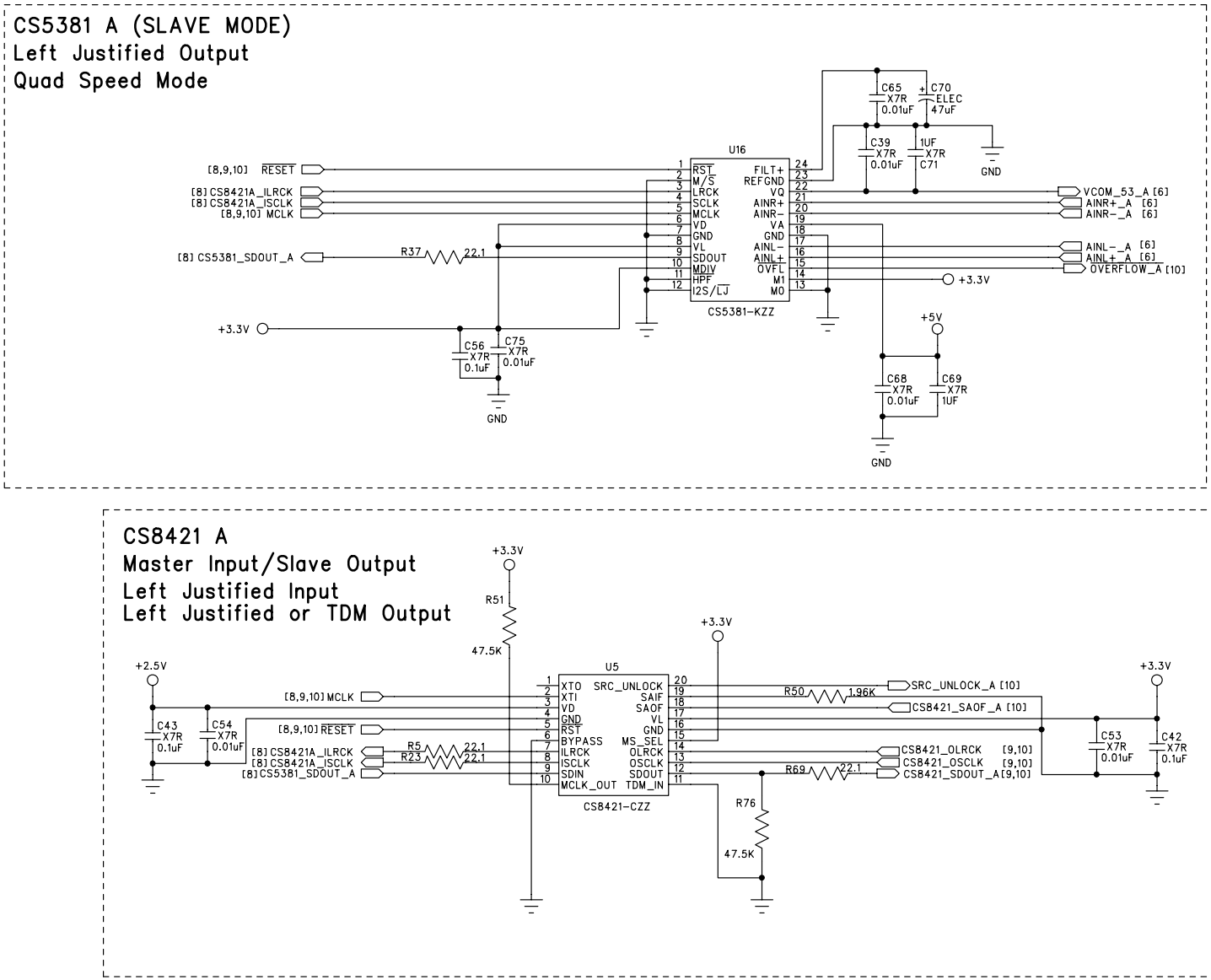

Figure 11. CS5381 & CS8421 Pair A

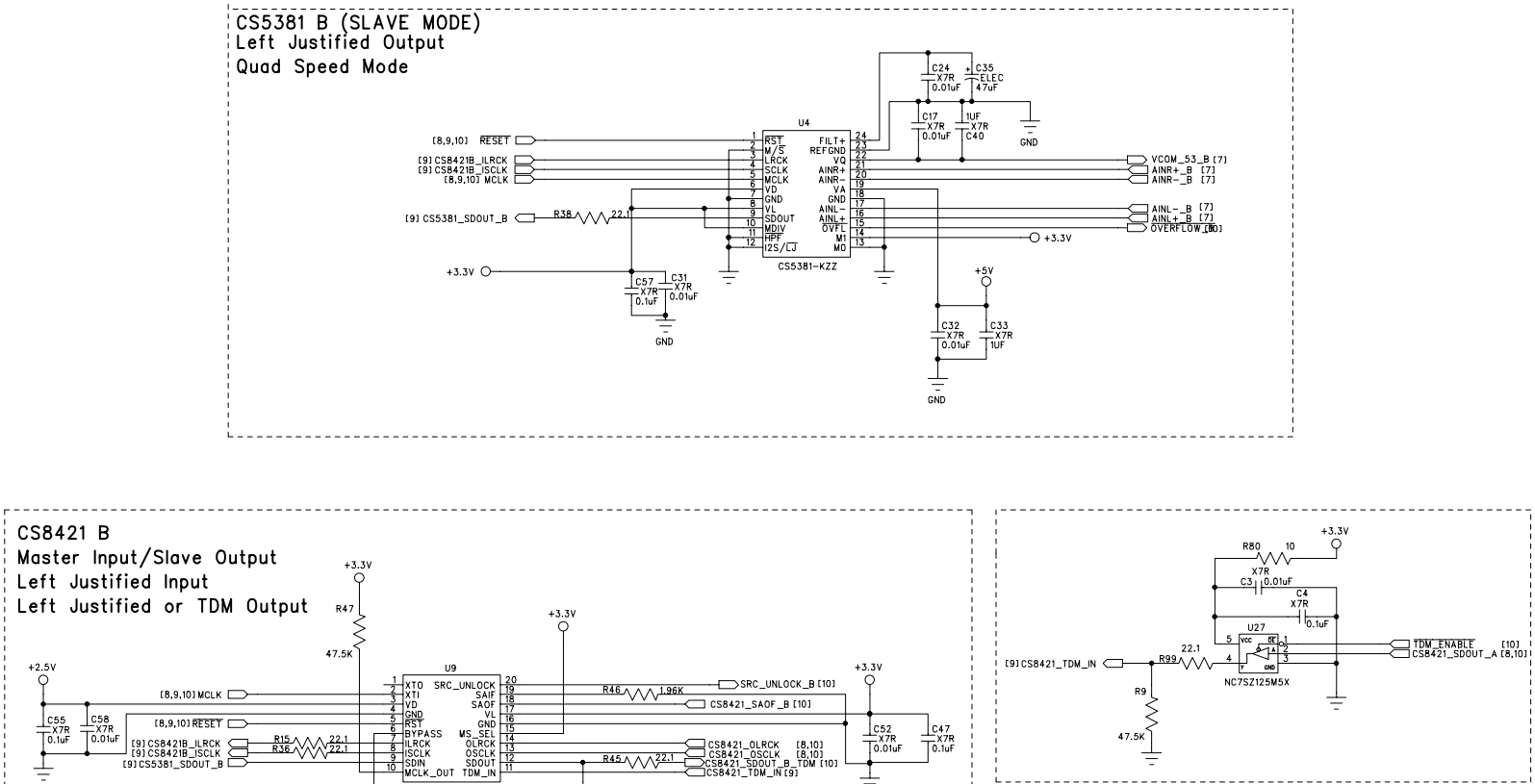

Figure 12. CS5381 & CS8421 Pair B

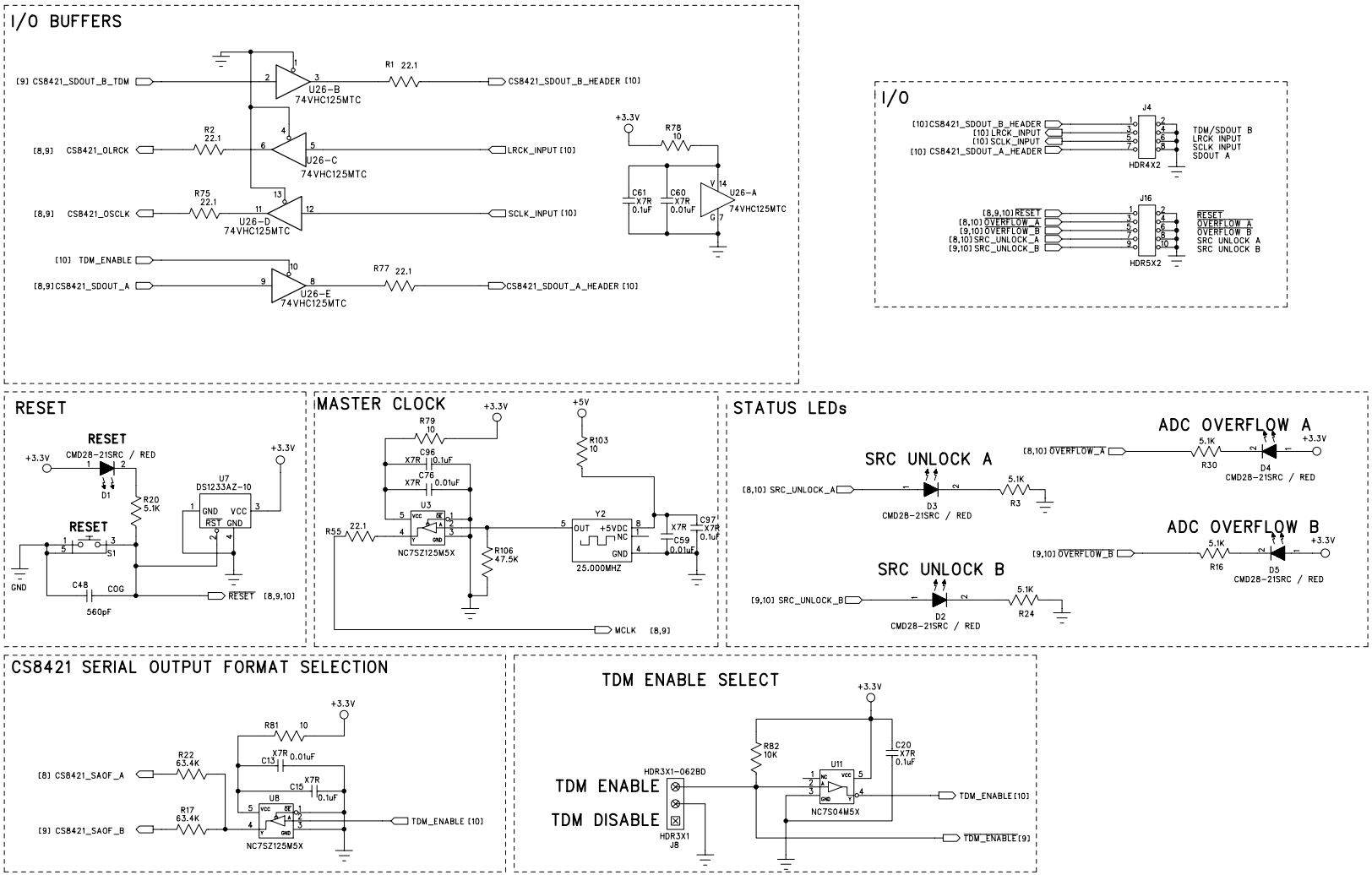

Figure 13. I/O Header and Miscellaneous

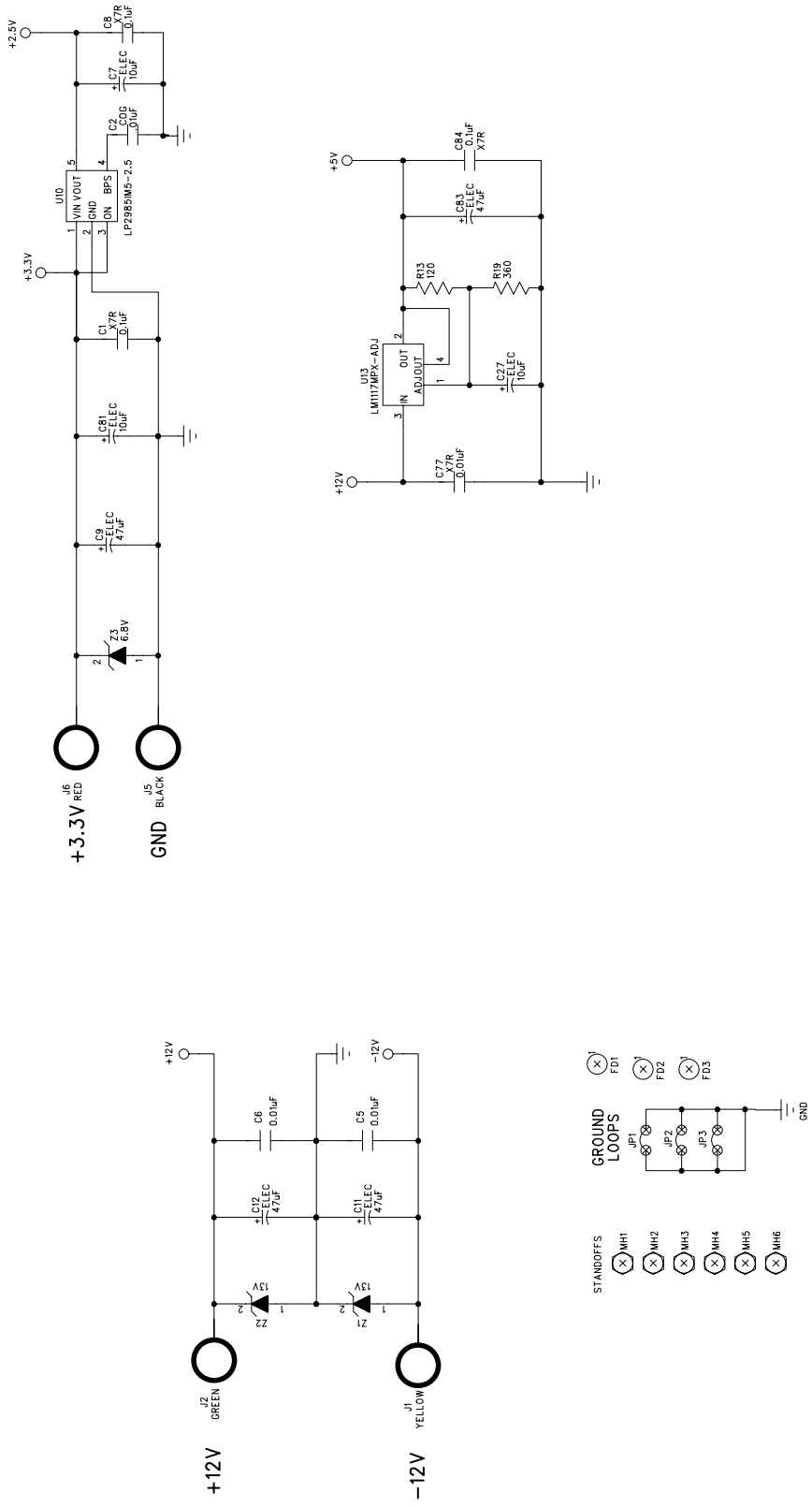

Figure 14. Power

5. LAYOUT

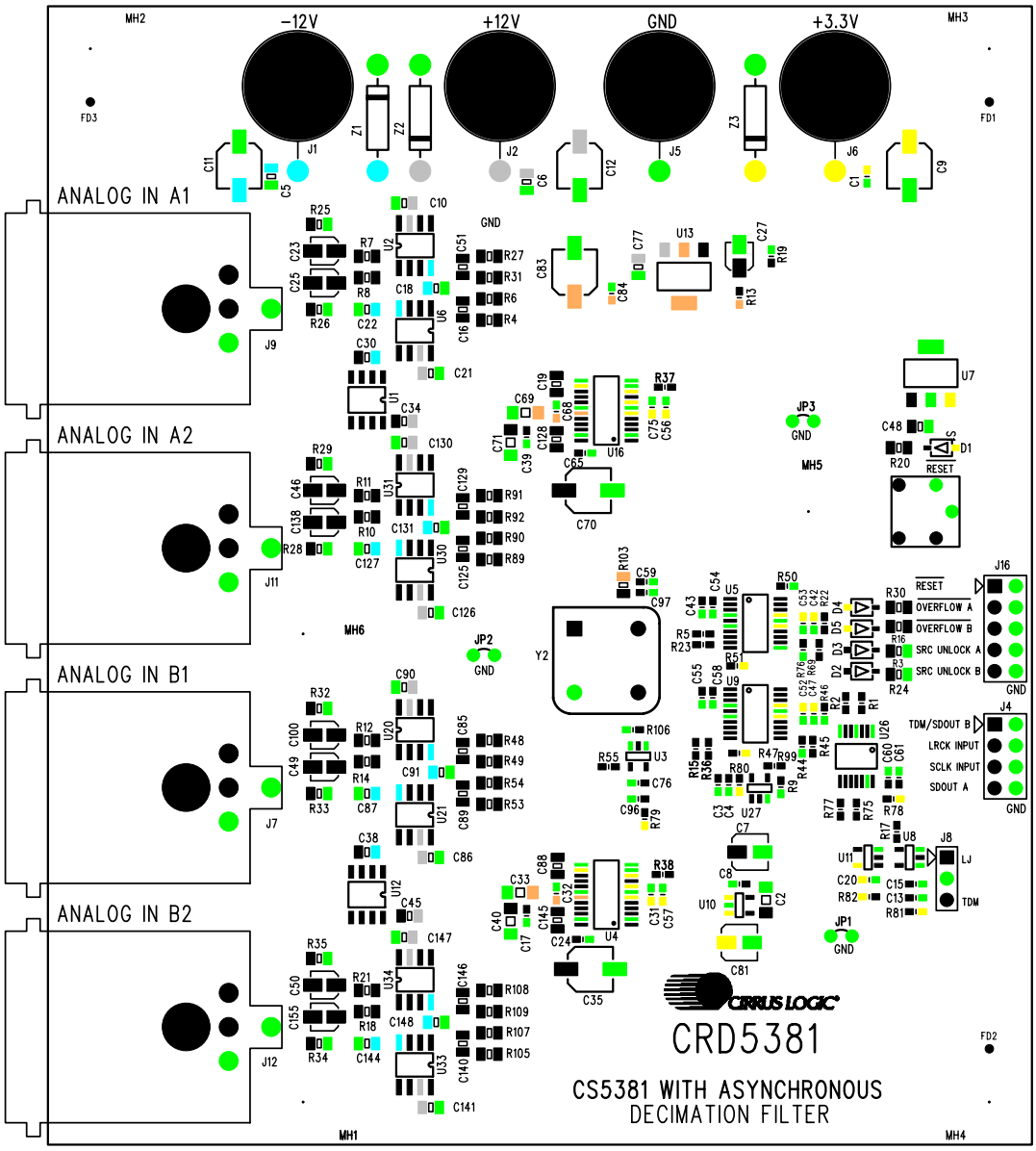

Figure 15. Silk Screen

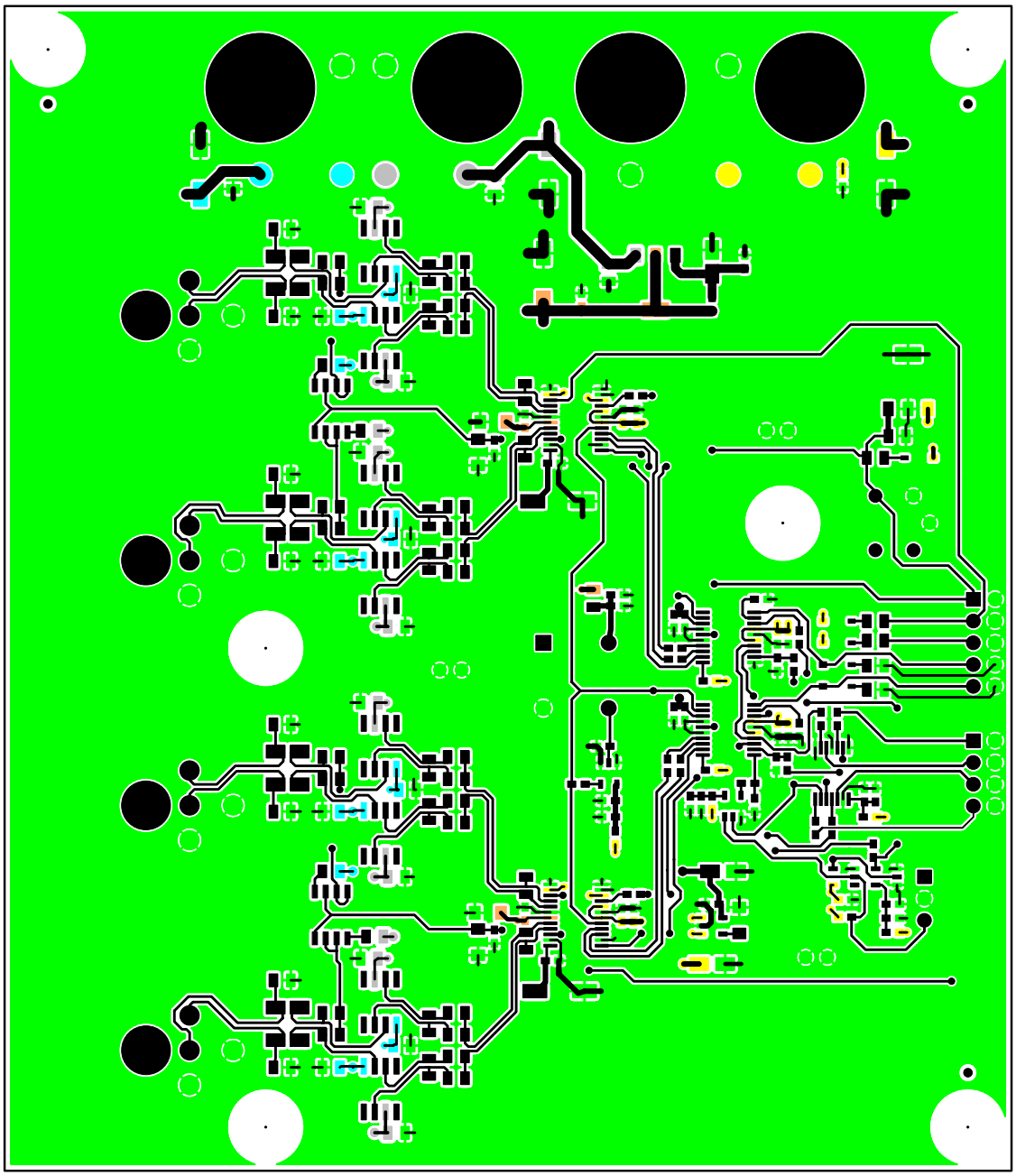

Figure 16. Top Layer

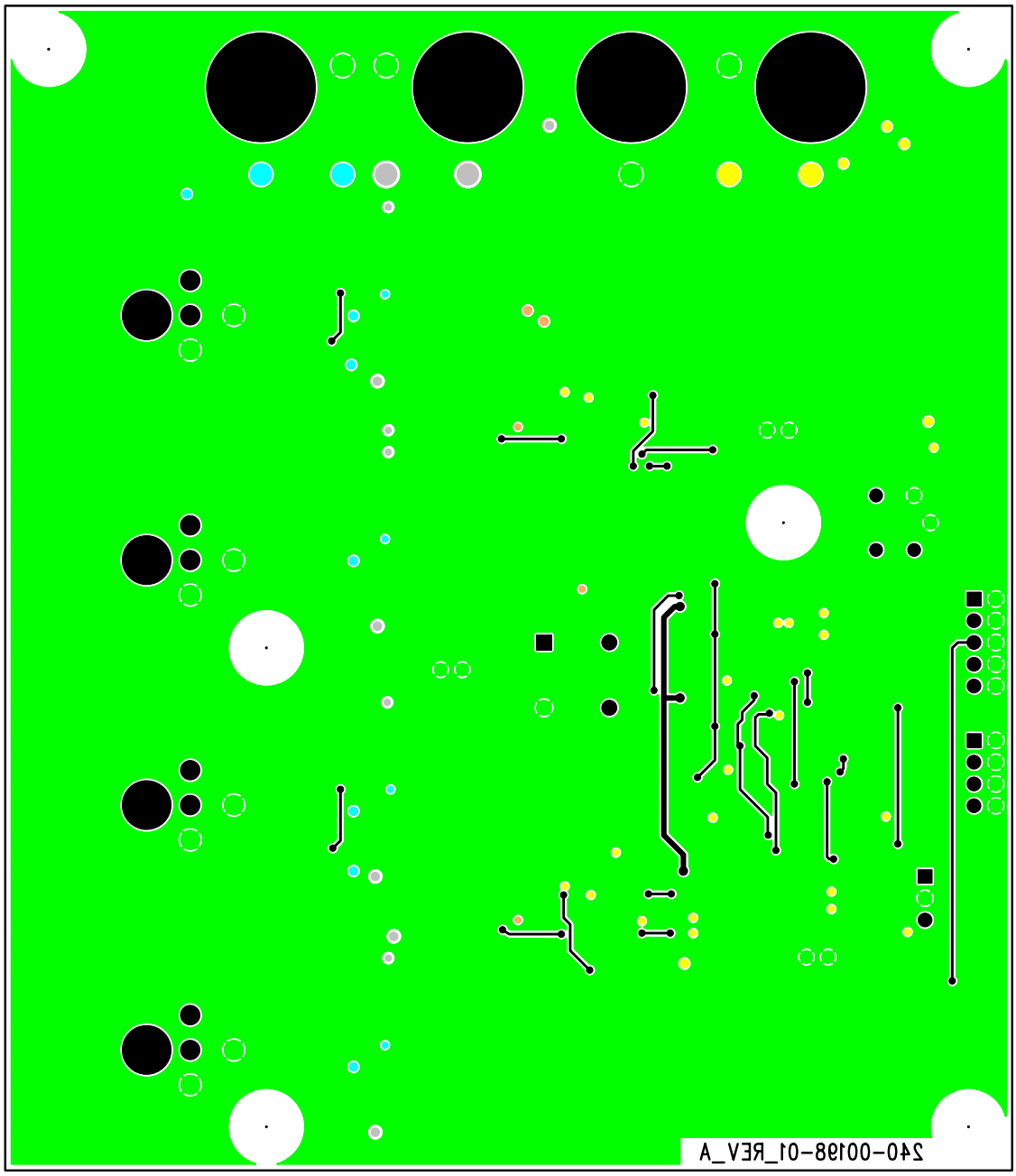

Figure 17. Bottom Layer

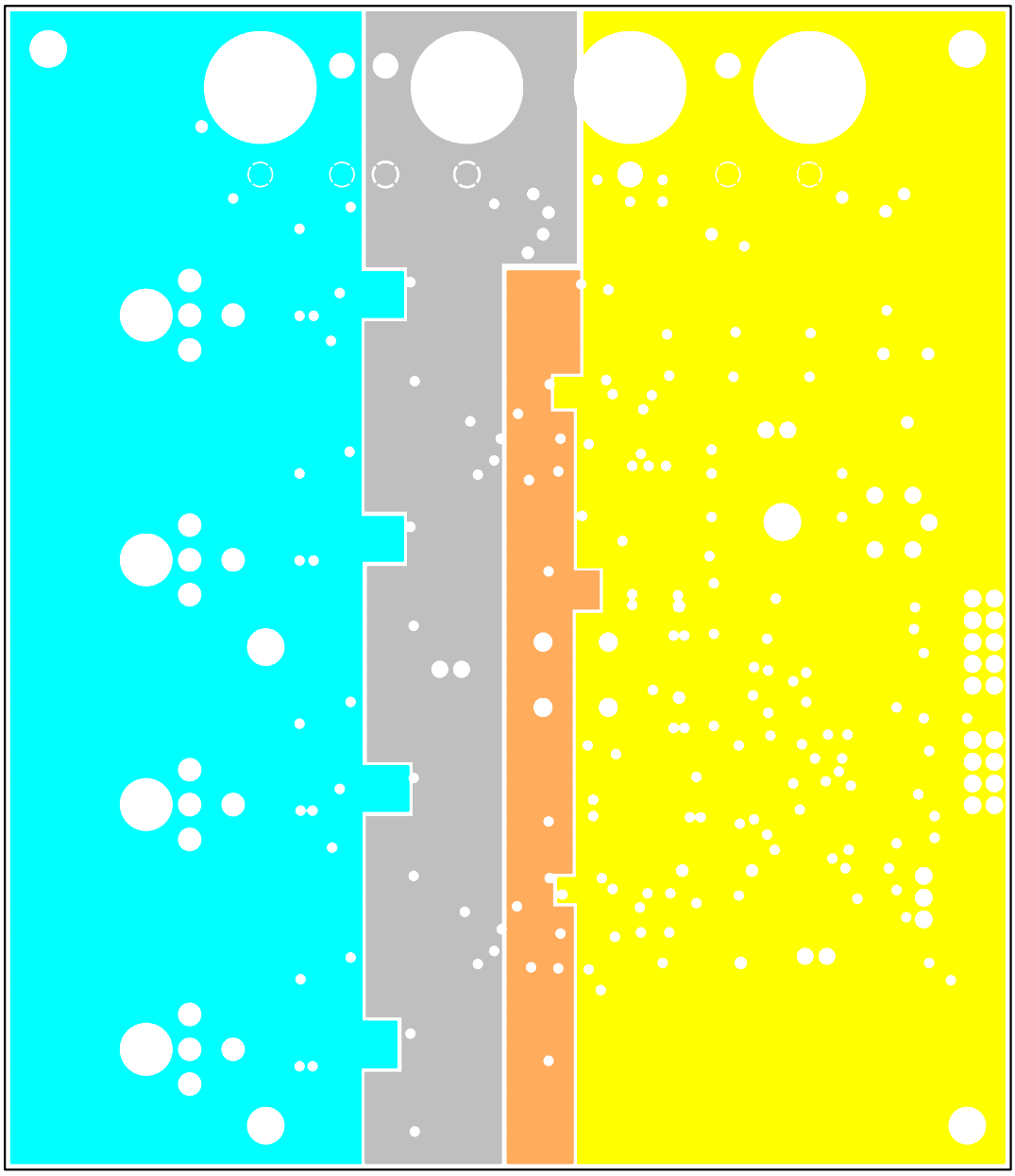

Figure 18. Power Plane

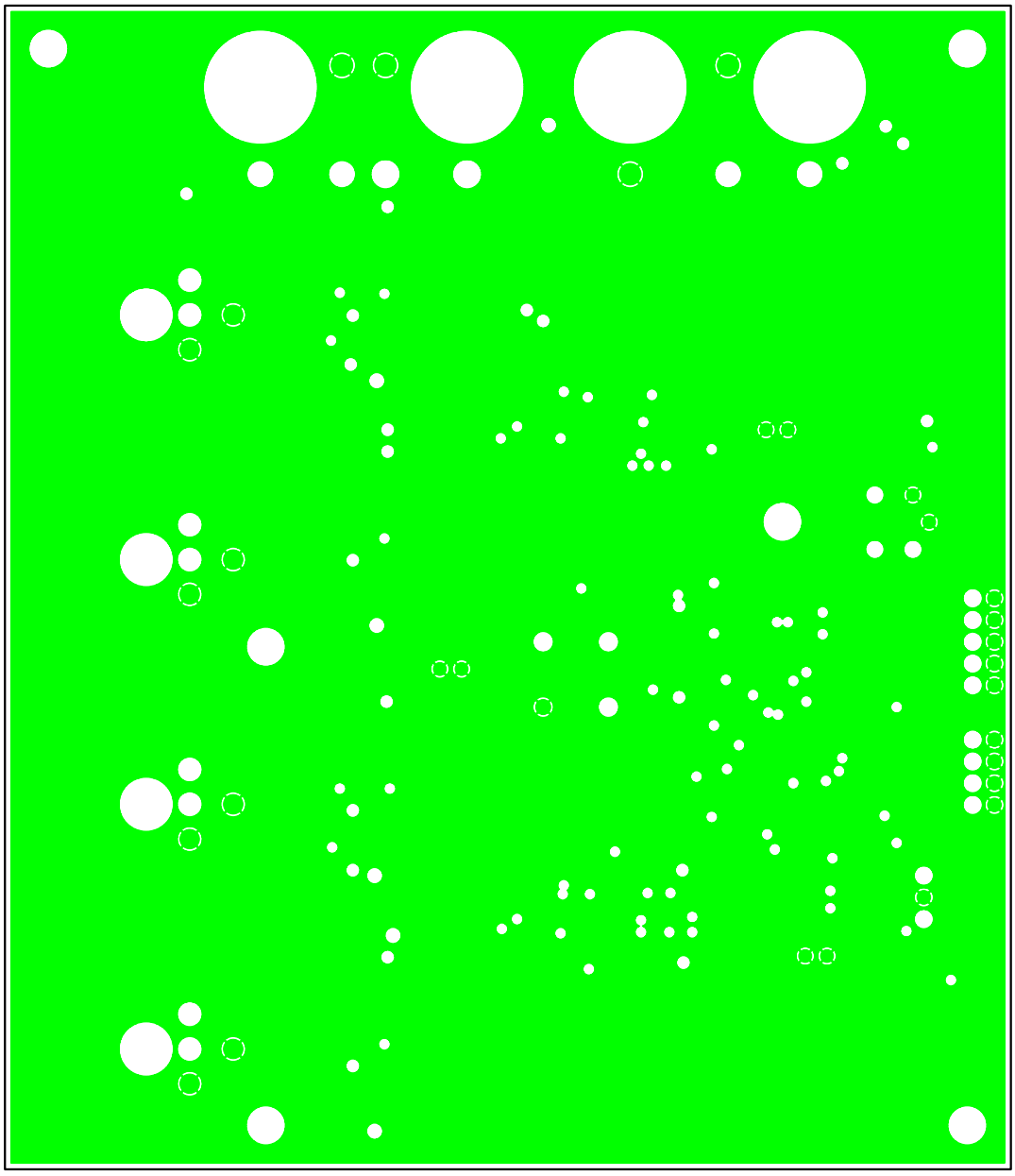

Figure 19. Ground Plane

6. REFERENCES

[1] **AN270- Audio A/D Conversion w/ Asynchronous Decimation Filter web page:**
http://www.cirrus.com

[2] **CS5381 - 120 dB, 192 kHz Stereo A/D Converter web page:**
http://www.cirrus.com/en/products/pro/detail/P1024.html

[3] **CS8421 - 32-bit, 192 kHz, Asynchronous, Stereo Sample Rate Converter web page:**
http://www.cirrus.com/en/products/pro/detail/P1082.html

7. REVISION HISTORY

Release	Date	Changes
DB1	MAY 2005	1st Release

Table 3. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to **www.cirrus.com**

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