



PSMN2R2-40BS

N-channel 40 V 2.2 mΩ standard level MOSFET in D2PAK

Rev. 1 — 20 March 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in SOT404 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC convertors
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

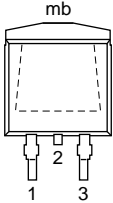
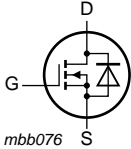
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	[1]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	306	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C};$ see Figure 6	-	2.73	3.2	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see Figure 6 ; see Figure 13	-	1.88	2.2	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 20\text{ V};$ see Figure 14 ; see Figure 15	-	25	-	nC
$Q_{G(tot)}$	total gate charge		-	130	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ $I_D = 100\text{ A}; V_{sup} \leq 40\text{ V};$ unclamped; $R_{GS} = 50\text{ Ω}$	-	-	1.24	J

[1] Continuous current is limited by package



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT404 (D2PAK)</p>	
2	D	drain ^[1]		
3	S	source		
mb	D	drain		

[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R2-40BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R2-40BS	PSMN2R2-40BS

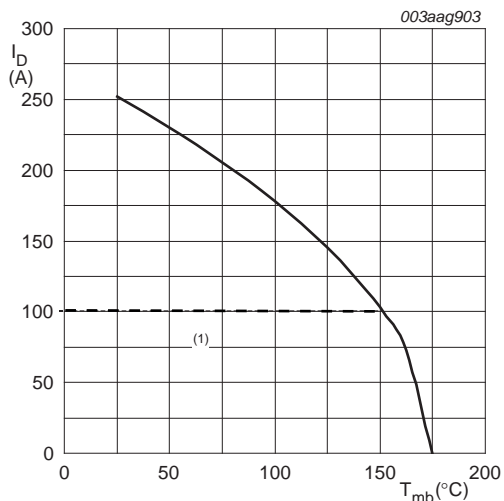
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

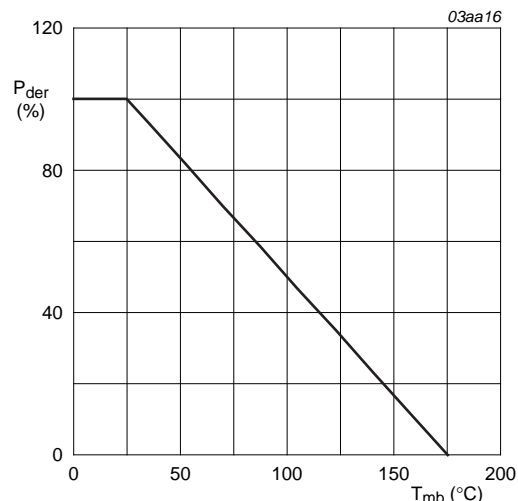
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	40	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; see Figure 1	[1]	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 1	[1]	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 3	-	962	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	306	W
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$
T_j	junction temperature		-55	175	$^{\circ}\text{C}$
$T_{sld(M)}$	peak soldering temperature		-	260	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	[1]	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$	-	962	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 40\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	1.24	J

[1] Continuous current is limited by package



$V_{GS} \geq 10\text{ V}$; (1) Capped at 100 A due to package

Fig 1. Continuous drain current as a function of mounting base temperature.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

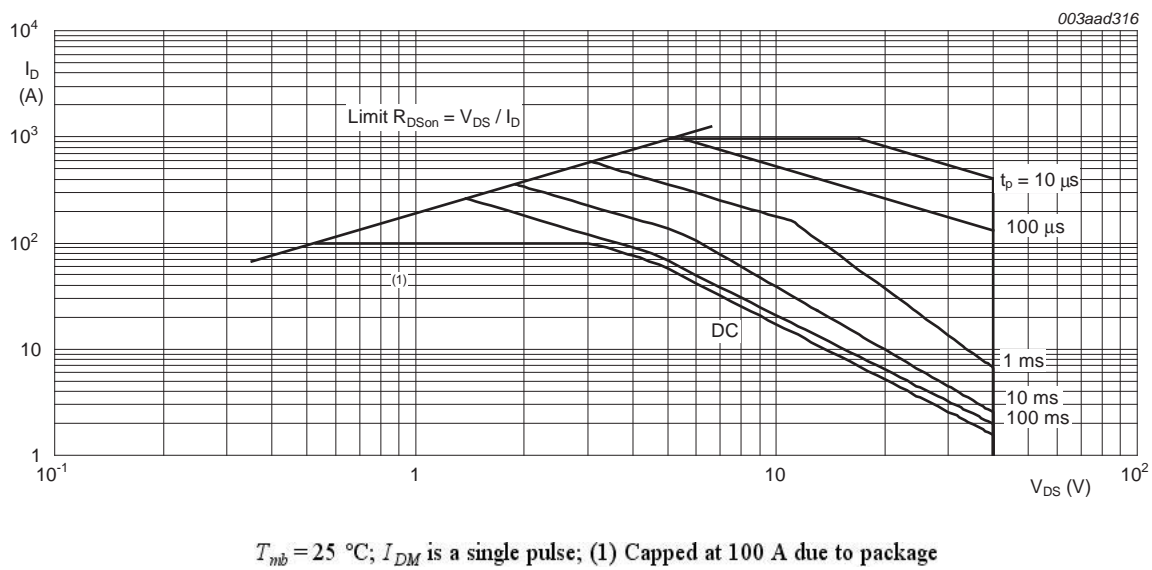


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.25	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum foot print; mounted in a printed circuit board	-	50	-	K/W

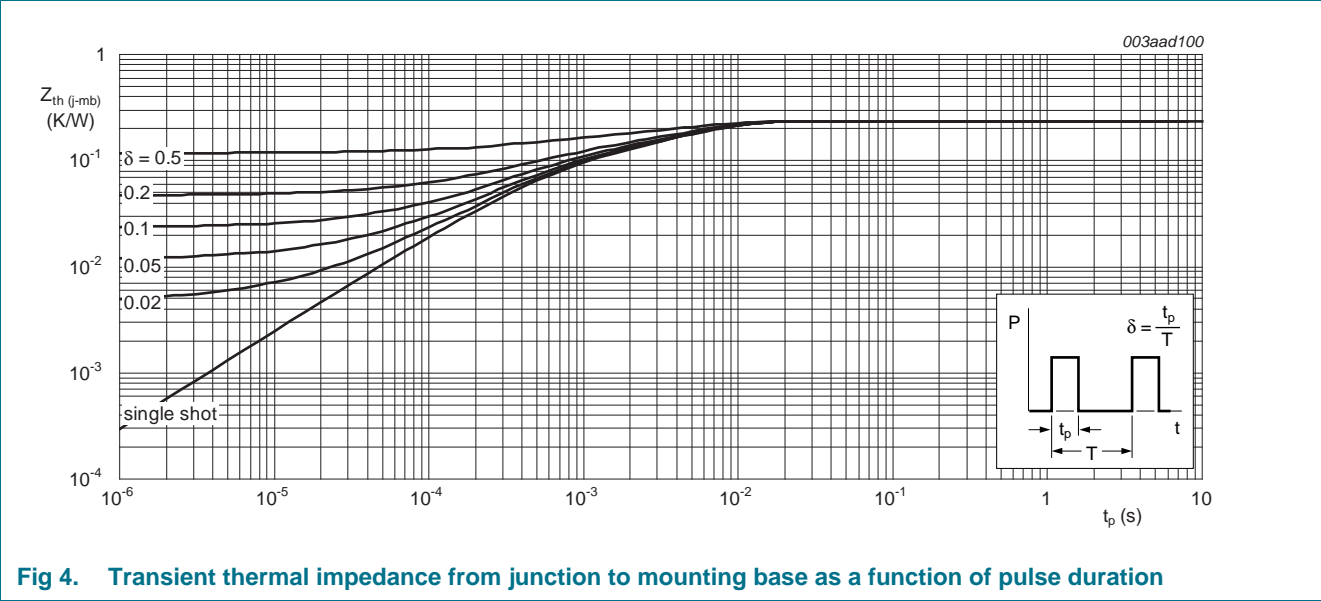


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$	36	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ C$; see Figure 11	-	-	4.6	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 175\ ^\circ C$; see Figure 11	1	-	-	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$; see Figure 12 ; see Figure 11	2	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 40\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	0.02	10	μA
		$V_{DS} = 40\ V$; $V_{GS} = 0\ V$; $T_j = 125\ ^\circ C$	-	-	200	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
		$V_{GS} = -20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 100\ ^\circ C$; see Figure 6	-	2.73	3.2	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 175\ ^\circ C$; see Figure 13 ; see Figure 6	-	3.76	4.4	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; see Figure 6 ; see Figure 13	-	1.88	2.2	mΩ
R_G	internal gate resistance (AC)	$f = 1\ MHz$	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$	-	110	-	nC
		$I_D = 25\ A$; $V_{DS} = 20\ V$; $V_{GS} = 10\ V$; see Figure 14 ; see Figure 15	-	130	-	nC
Q_{GS}	gate-source charge		-	42	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	24	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	18	-	nC
Q_{GD}	gate-drain charge		-	25	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\ A$; $V_{DS} = 20\ V$; see Figure 14 ; see Figure 15	-	4.95	-	V
C_{iss}	input capacitance	$V_{DS} = 20\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$;	-	8423	-	pF
C_{oss}	output capacitance	$T_j = 25\ ^\circ C$; see Figure 16	-	1671	-	pF
C_{rss}	reverse transfer capacitance		-	814	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\ V$; $R_L = 0.25\ \Omega$; $V_{GS} = 10\ V$;	-	33.2	-	ns
t_r	rise time	$R_{G(ext)} = 1.5\ \Omega$	-	40.4	-	ns
$t_{d(off)}$	turn-off delay time		-	66.6	-	ns
t_f	fall time		-	25.2	-	ns

Table 7. Characteristics ...continued
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$	-	53.7	-	ns
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	80.75	-	nC

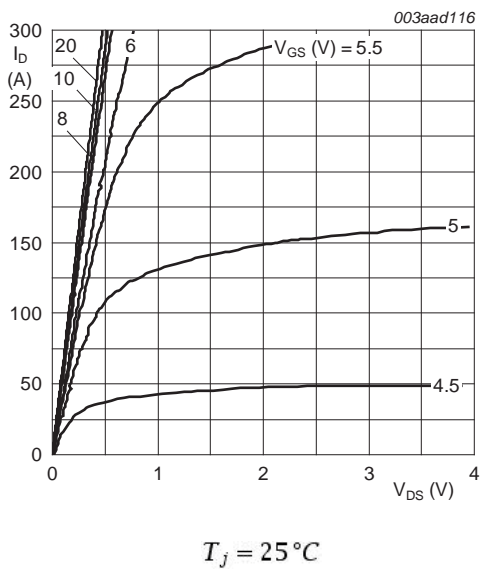


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

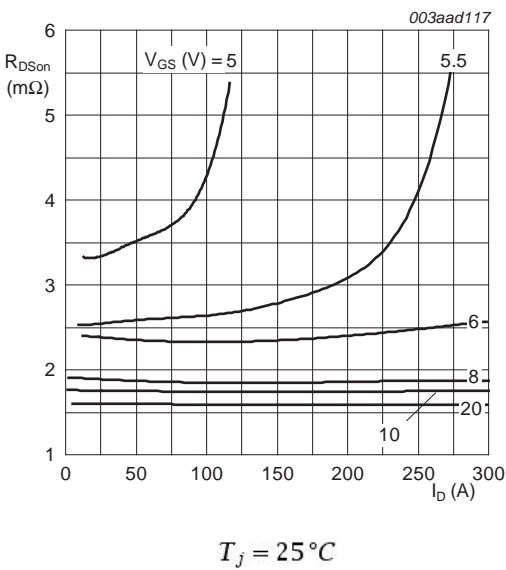
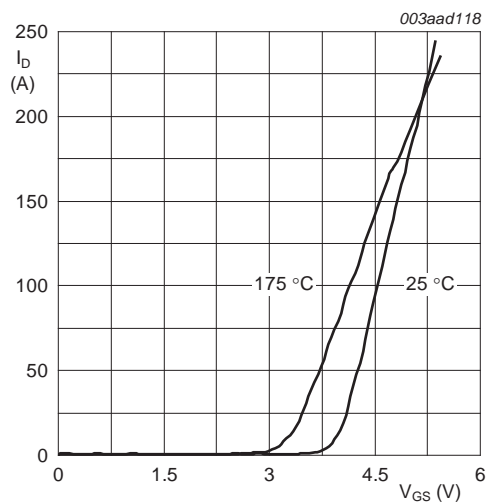
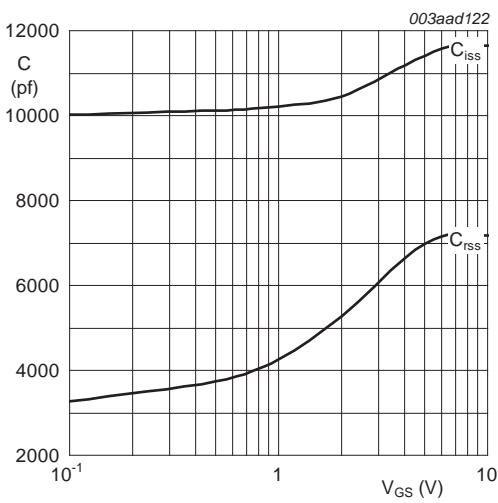


Fig 6. Drain-source on-state resistance as a function of drain current; typical values



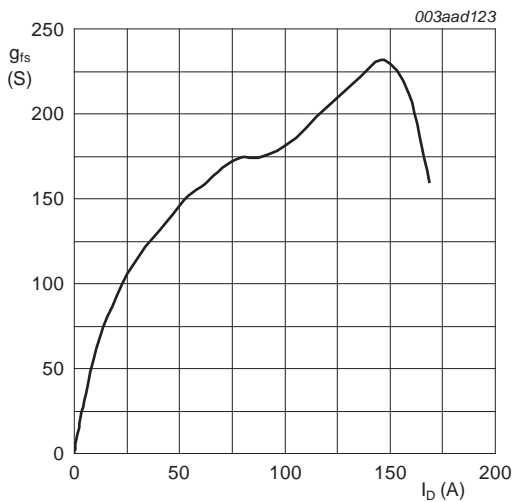
$V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



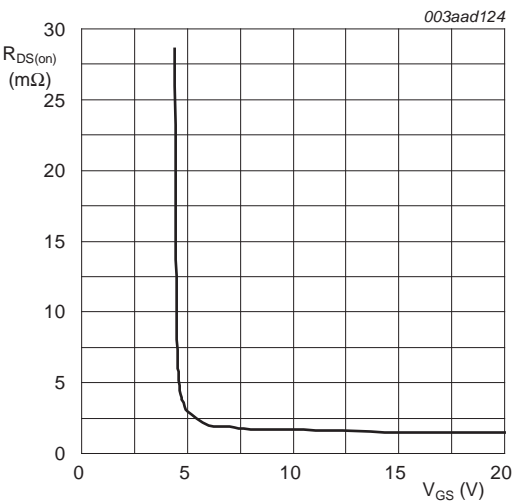
$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



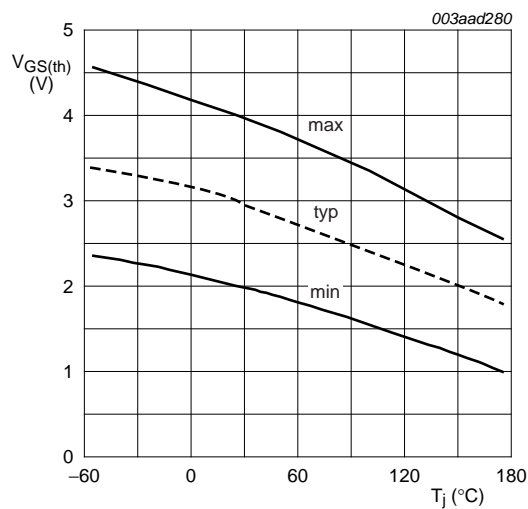
$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 25\text{ V}$

Fig 9. Forward transconductance as a function of drain current; typical values



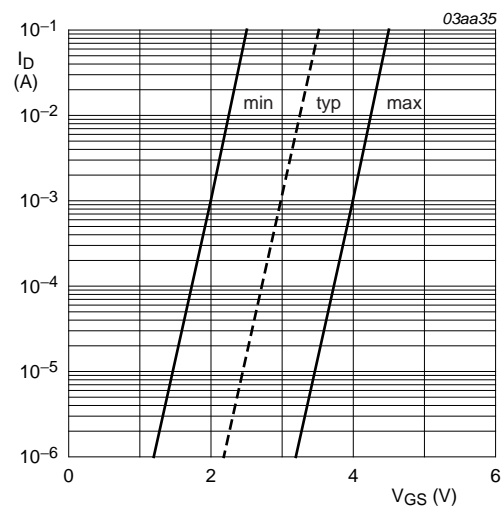
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



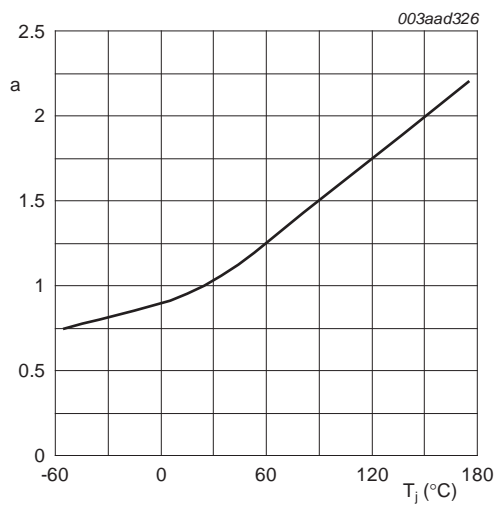
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ °C}; V_{DS} = 5V$

Fig 12. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^\circ\text{C}}}$$

Fig 13. Normalized drain-source on state resistance factor as a function of junction temperature

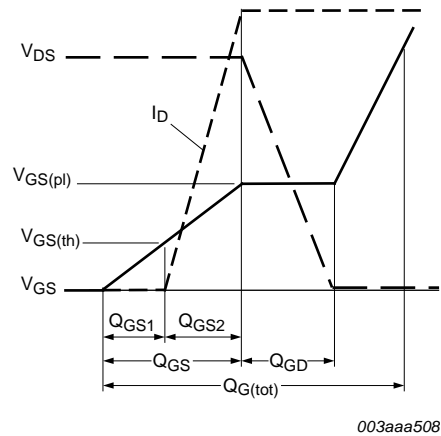


Fig 14. Gate charge waveform definitions

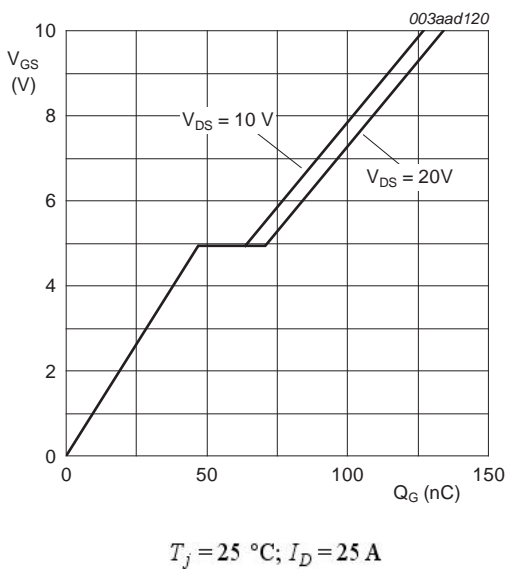


Fig 15. Gate-source voltage as a function of gate charge; typical values

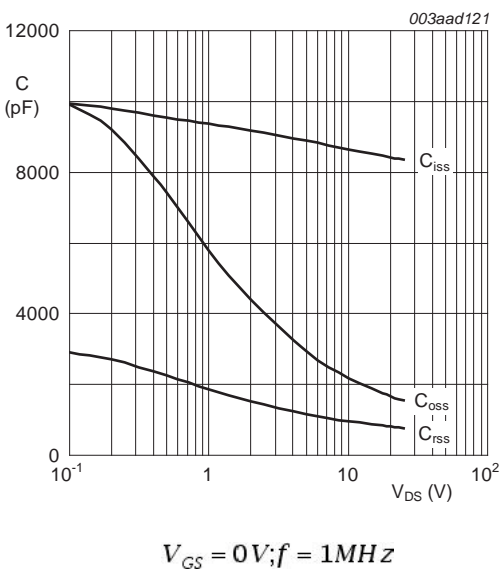


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

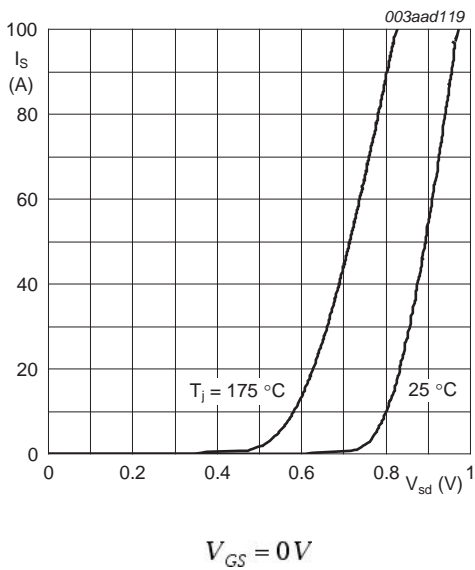


Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

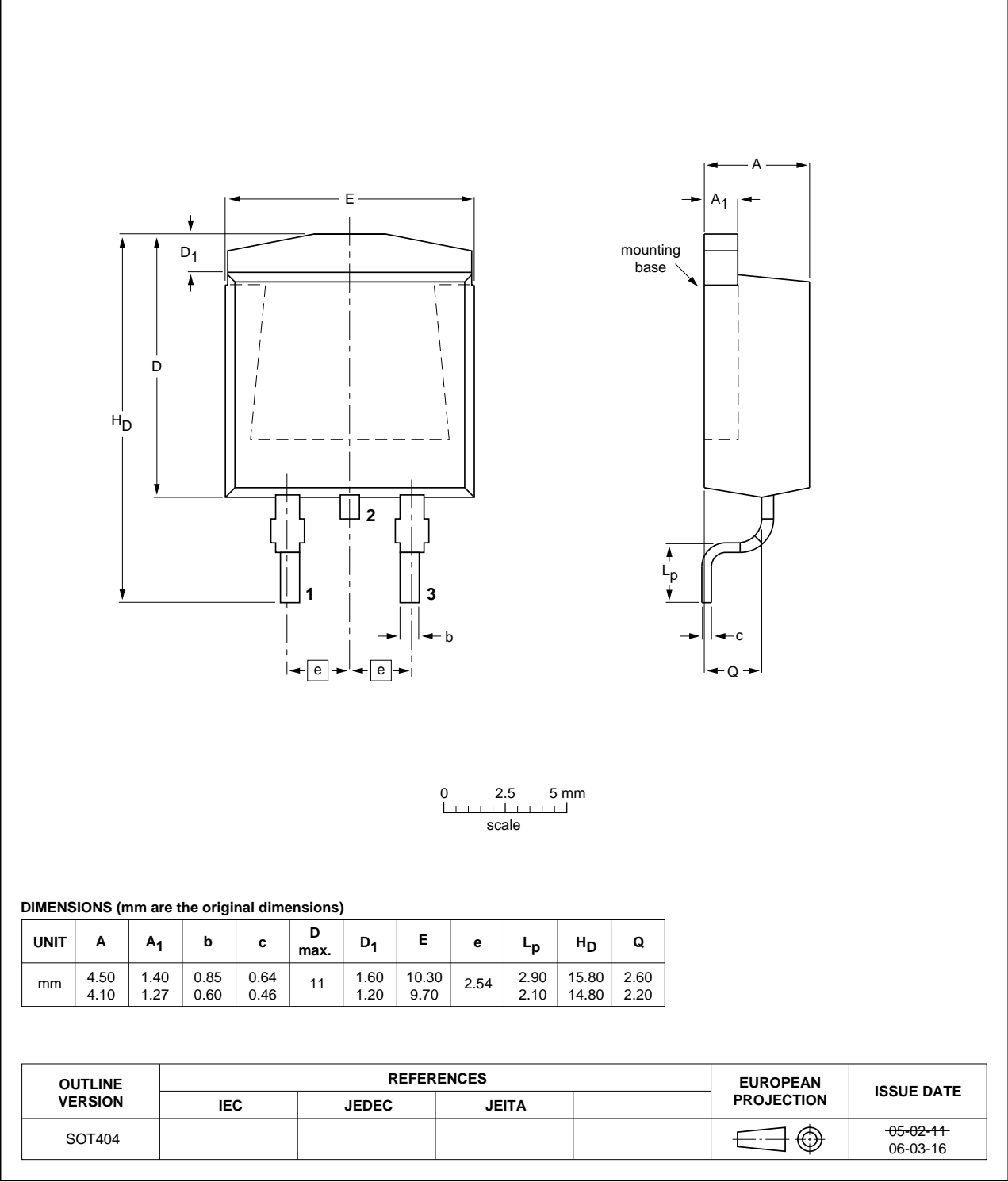


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R2-40BS v.1	20120320	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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12. Contents

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Date of release: 20 March 2012

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