LMV242 Dual Output, Quad-Band GSM/GPRS Power Amplifier Controller

Check for Samples: LMV242

FEATURES

- **Support of InGaP HBT, Bipolar Technology**
- **Quad-Band Operation**
- **Shutdown Mode for Power Save in R_X Slot**
- **Integrated Ramp Filter**
- **50 dB RF Detector**
- **GPRS Compliant**
- **External Loop Compensation Option**
- **Accurate Temperature Compensation**
- **WSON Package 3x3 mm and Fully Tested Die Sales**

APPLICATIONS

- **GSM/GPRS/TDMA/TD_SCDMA Mobile Phone**
- **Pulse RF Control**
- **Wireless LAN**
- **GSM/GPRS Power Amplifier Module**
- **Transmit Module**

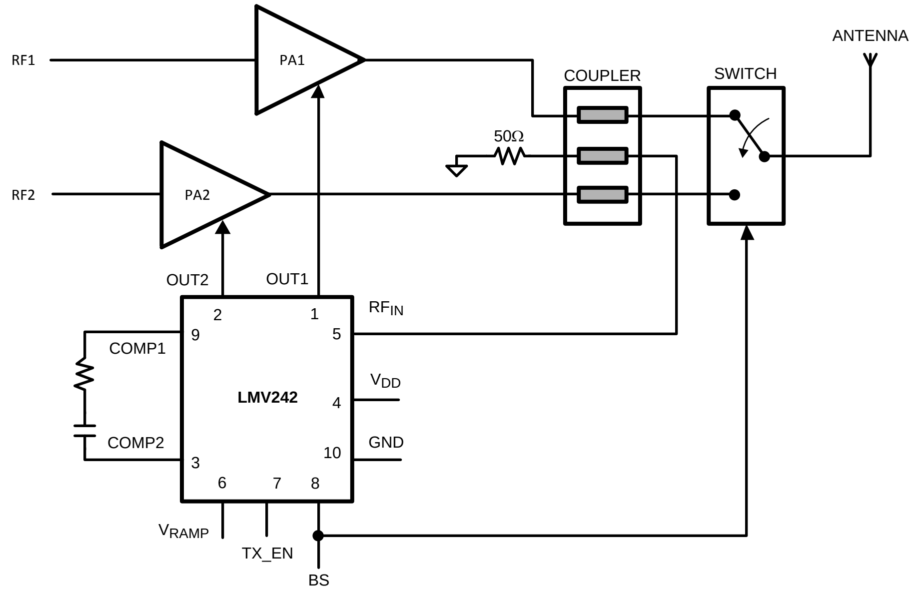
DESCRIPTION

The LMV242 is a power amplifier (PA) controller intended for use within an RF transmit power control loop in GSM/GPRS mobile phones. The LMV242 supports all single-supply PA's including InGaP, HBT and bipolar power amplifiers. The device operates with a single supply from 2.6V to 5.5V.

Included in the PA controller are an RF detector, a ramp filter and two selectable output drivers that function as error amplifiers for two different bands. The LMV242 input interface consists two analog and two digital inputs. The analog inputs are the RF input, Ramp voltage input. The digital inputs perform the function of "Band Select" and "Shutdown/Transmit Enable" respectively. The "Band Select" function enables either of two outputs, namely OUT1 when BS = High, or output OUT2 when BS = Low. The output that is not enabled is pulled low to the minimum output voltage. The LMV242 is active in the case TX_EN = High. When TX_EN = Low the device is in a low power consumption shutdown mode. During shutdown both outputs will be pulled low to the minimum output voltage. Individual PA characteristics are accommodated by a user selectable external RC combination.

The LMV242 is offered in fully tested die form as well as in a 10-lead WSON package and is therefore especially suitable for small footprint PA module solutions.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage	V_{DD} - GND	6.5V Max
ESD Tolerance (3)	Human Body Model	2 kV
	Machine Model	200V
Storage Temperature Range		−65°C to 150°C
Junction Temperature (4)		150°C Max
Mounting Temperature	Infrared or convection (20 sec)	235°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the 2.6V ELECTRICAL CHARACTERISTICS.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model: 1.5 kΩ in series with 100 pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

OPERATING RATINGS (1)

Supply Voltage	2.6V to 5.5V
Operating Temperature Range	−40°C to +85°C
V_{RAMP} Voltage Range	0V to 2V
RF Frequency Range	450 MHz to 2 GHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the 2.6V ELECTRICAL CHARACTERISTICS.

2.6V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified to T_J = 25°C. V_{DD} = 2.6V. **Boldface** limits apply at temperature extremes (1).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Supply Current	V_{OUT} = (V_{DD} - GND)/2		6.9	9 **12**	mA
		In Shutdown (TX_EN = 0V) V_{OUT} = (V_{DD} - GND)/2		0.2	**30**	μA
V_{HIGH}	Logic Level to Enable Power	See (2)	**1.8**			V
V_{LOW}	Logic Level to Disable Power	See (2)			**0.8**	V
T_{ON}	Turn-on-Time from Shutdown			3.6	6	μs
I_{EN}, I_{BS}	Current into TX_EN and BS Pin			0.03	**5**	μA
RAMP Amplifier						
V_{RD}	V_{RAMP} Deadband		155	206	265	mV
$1/R_{RAMP}$	Transconductance	See (3)	**70**	96	**120**	μA/V
$I_{OUT\ RAMP}$	Ramp Amplifier Output Current	V_{RAMP} = 2V	**100**	162		μA
RF Input						
P_{IN}	RF Input Power Range (4)	20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−50 0		dBm
				−63 −13		dBV
	Logarithmic Slope (5)	@ 900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−1.74		μA/dB
		@ 1800 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−1.62		
		@ 1900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−1.60		
		@ 2000 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−1.59		
	Logarithmic Intercept (5)	@ 900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–50.4		dBm
		@ 1800 MHz, 20 kΩ // 68 if between V_{COMP1} and V_{COMP2}		–52.3		
		@ 1900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–51.9		
		@ 2000 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–52.3		
R_{IN}	DC Resistance	See (3)		55.7		Ω
Error Amplifier						
GBW	Gain-Bandwidth Product	See (3)		5.1		MHz
V_O	Output Swing from Rail	From Positive Rail, Sourcing, I_O = 7 mA		47	90 **115**	mV
		From Negative Rail Sinking, I_O = −7 mA		52	90 **115**	
I_O	Output Short Circuit Current (6)	Sourcing, V_O = 2.4V	**10**	29.5		mA
		Sinking, $V_{O.}$ = 0.2V	**10**	27.1		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are specified by design or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Power in dBV = dBm + 13 when the impedance is 50Ω.
(5) Slope and intercept are calculated from graphs "V_{OUT} vs. RF input power" where the current is obtained by division of the voltage by 20 kΩ.
(6) The output is not short circuit protected internally. External protection is necessary to prevent overheating and destruction or adverse reliability.

2.6V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified to T_J = 25°C. V_{DD} = 2.6V. **Boldface** limits apply at temperature extremes (1).

Symbol	Parameter	Condition	Min	Typ	Max	Units
e_n	Output Referred Noise	$f_{MEASURE}$ = 10 KHz, RF Input = 1800 MHz, -10 dBm, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}, V_{OUT} =1.4V, set by V_{RAMP}, (3)		700		nV/√Hz
SR	Slew Rate		2.1	4.4		V/μs

5.0V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified to T_J = 25°C. V_{DD} = 5.0V. **Boldface** limits apply at temperature extremes (1).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Supply Current	V_{OUT} = (V_{DD} - GND)/2		7.8	12 **15**	mA
		In Shutdown (TX_EN = 0V) V_{OUT} = (V_{DD} - GND)/2		0.4	**30**	μA
V_{HIGH}	Logic Level to Enable Power	See (2)	**1.8**			V
V_{LOW}	Logic Level to Disable Power	See (2)			**0.8**	V
T_{ON}	Turn-on-Time from Shutdown			1.5	6	μs
I_{EN}, I_{BS}	Current into TX_EN and BS Pin			0.03	**5**	μA
RAMP Amplifier						
V_{RD}	V_{RAMP} Deadband		155	206	265	mV
$1/R_{RAMP}$	Transconductance	See (3)	**70**	96	**120**	μA/V
$I_{OUT\ RAMP}$	Ramp Amplifier Output Current	V_{RAMP} = 2V	**100**	168		μA
RF Input						
P_{IN}	RF Input Power Range (4)	20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−50 0		dBm
				−63 −13		dBV
	Logarithmic Slope (5)	@ 900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−1.79		μA/dB
		@ 1800 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–1.69		
		@ 1900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		−1.67		
		@ 2000 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–1.65		
	Logarithmic Intercept (5)	@ 900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–50.2		dBm
		@ 1800 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–52.5		
		@ 1900 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–52.5		
		@ 2000 MHz, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}		–52.9		
R_{IN}	DC Resistance	See (3)		55.7		Ω
Error Amplifier						

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are specified by design or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Power in dBV = dBm + 13 when the impedance is 50Ω.
(5) Slope and intercept are calculated from graphs "V_{OUT} vs. RF input power" where the current is obtained by division of the voltage by 20 kΩ.

5.0V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified to T_J = 25°C. V_{DD} = 5.0V. **Boldface** limits apply at temperature extremes [1].

Symbol	Parameter	Condition	Min	Typ	Max	Units
GBW	Gain-Bandwidth Product	See [3]		5.7		MHz
V_O	Output Swing from Rail	From Positive Rail, Sourcing, I_O = 7 mA		31	80 **105**	mV
		From Negative Rail Sinking, I_O = −7 mA		35	80 **105**	mV
I_O	Output Short Circuit Current [6]	Sourcing, V_O = 4.8V	**15**	31.5		mA
		Sinking, V_O = 0.2V	**15**	31.5		mA
e_n	Output Referred Noise	$f_{MEASURE}$ = 10 kHz, RF Input = 1800 MHz, -10dBm, 20 kΩ // 68 pF between V_{COMP1} and V_{COMP2}, V_{OUT} = 1.4V, set by V_{RAMP}, [3]		770		nV/√Hz
SR	Slew Rate		2.5	4.9		V/μs

(6) The output is not short circuit protected internally. External protection is necessary to prevent overheating and destruction or adverse reliability.

CONNECTION DIAGRAM

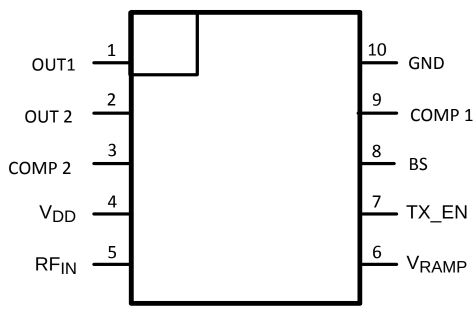


Figure 1. WSON-10 Top View

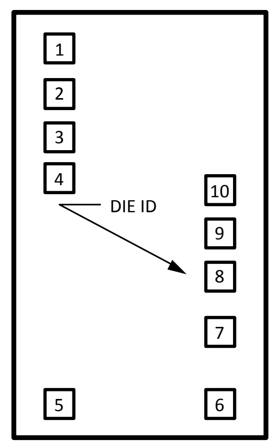


Figure 2. Bond Pad Layout Top View

BOND PAD MECHANICAL DIMENSIONS(1)

		X/Y Coordinates		Pad Size	
Signal Name	**Pad Number**	**X**	**Y**	**X**	**Y**
Out 1	1	−281	617	92	92
Out 2	2	−281	490	92	92
Comp2	3	−281	363	92	92
V_{DD}	4	−281	236	92	92
RF_{IN}	5	−281	−617	92	92
V_{RAMP}	6	281	−617	92	92
TX_EN	7	281	−360	92	92
BS	8	281	−118	92	92
Comp1	9	281	20	92	92
GND	10	281	187	92	92

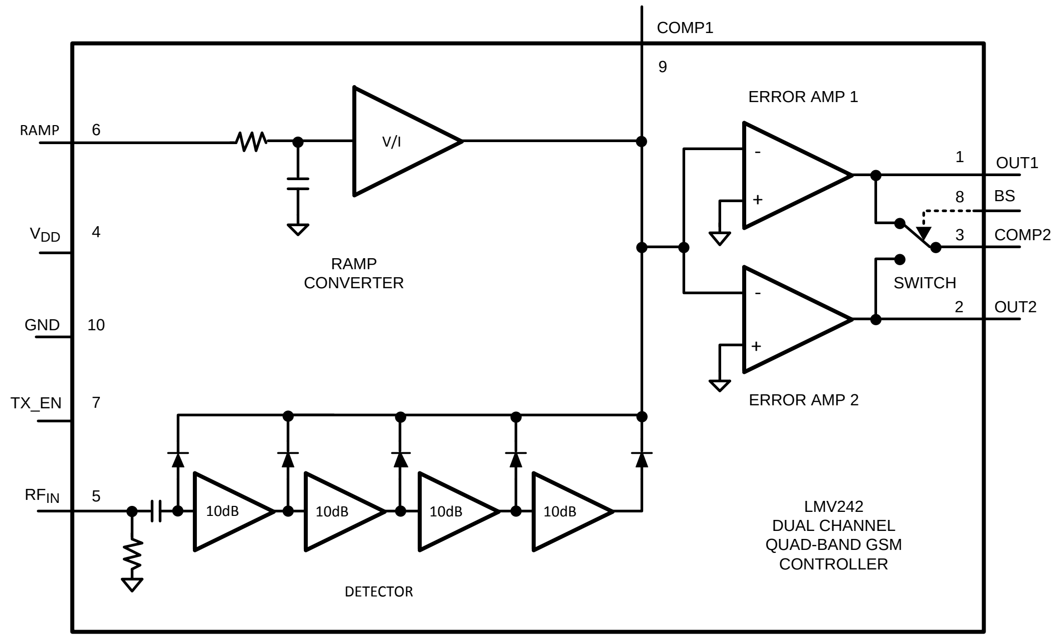
(1) Dimensions of the bond pad coordinates are in µm Origin of the coordinates: center of the die Coordinates refer to the center of the bond pad

PIN DESCRIPTIONS(1)

	Pin	Name	Description
Power Supply	4	V_{DD}	Positive Supply Voltage
	10	GND	Power Ground
Digital Inputs	7	TX_EN	Schmitt-triggered logic input. A LOW shuts down the whole chip for battery saving purposes. A HIGH enables the chip.
	8	BS	Schmitt-triggered Band Select pin. When BS = H, channel 1 (OUT1) is selected, when BS = L, channel 2 (OUT2) is selected.
Analog Inputs	5	RF_{IN}	RF Input connected to the Coupler output with optional attenuation to measure the Power Amplifier (PA) / Antenna RF power levels.
	6	V_{RAMP}	Sets the RF output power level. The useful input voltage range is from 0.2V to 1.8V, although voltages from 0V to V_{DD} are allowed.
Compensation	9	Comp1	Connects an external RC network between the Comp1 pin and the Comp2 pin for an overall loop compensation and to control the closed loop frequency response. Conventional loop stability techniques can be used in selecting this network, such as Bode plots. A good starting value for the RC combination will be C = 68 pF and R = 0Ω.
	3	Comp2	Frequency compensation pin. The BS signal switches this pin either to OUT1 or to OUT2.
Output	1	Out1	This pin is connected to the PA of either channel 1 or channel 2.
	2	Out2	

(1) 1. All inputs and outputs are referenced to GND (pin 10).
2. For the digital inputs, a LOW is < 0.8V and a HIGH is > 1.8V.
3. RF power detection is performed internally in the LMV242 and only an RF power coupler with optional extra attenuation has to be used.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_{DD} = +2.6V, T_J = 25°C.

Supply Current vs. Supply Voltage

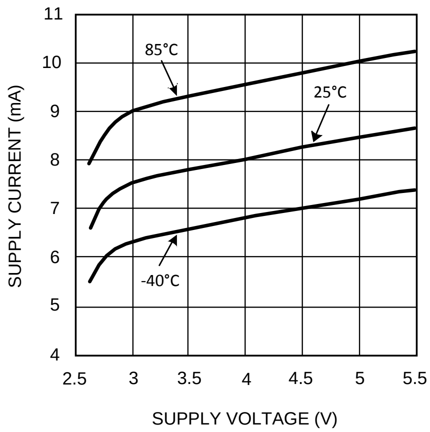


Figure 3.

V_{OUT} and Log Conformance vs. RF Input Power

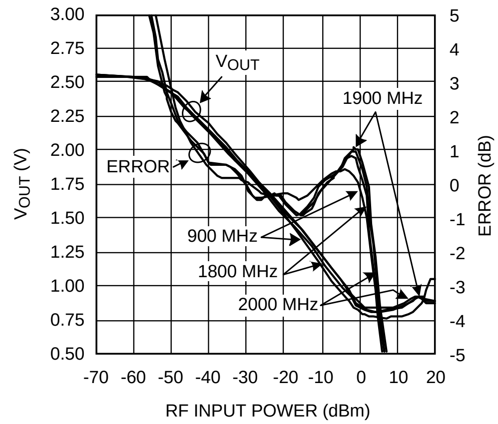


Figure 4.

V_{OUT} and Log Conformance vs. RF Input Power @ 900 MHz

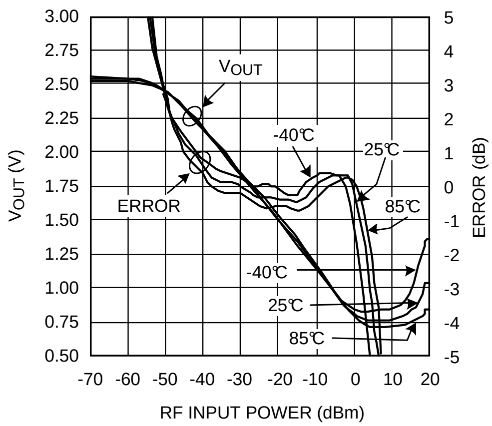


Figure 5.

V_{OUT} and Log Conformance vs. RF Input Power @ 1800 MHz

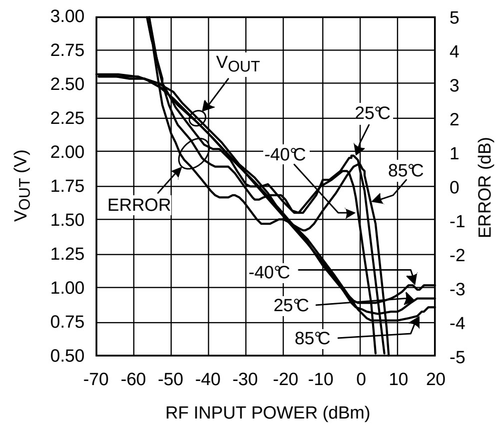


Figure 6.

V_{OUT} and Log Conformance vs. RF Input Power @ 1900 MHz

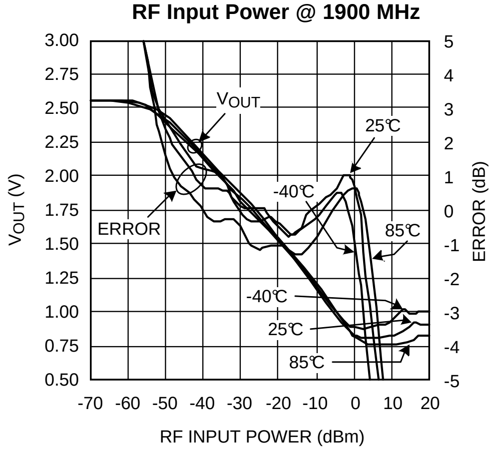


Figure 7.

V_{OUT} and Log Conformance vs. RF Input Power @ 2000 MHz

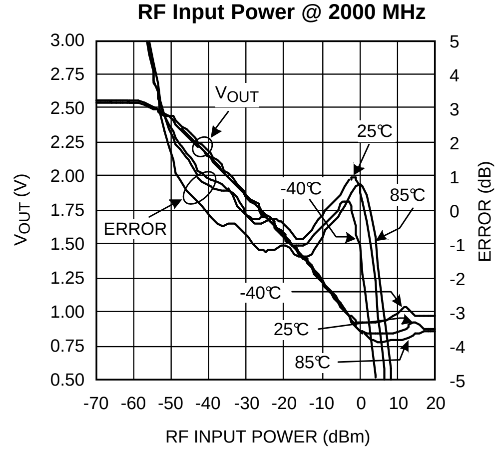


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{DD} = +2.6V, T_J = 25°C.

Logarithmic Slope vs. Frequency

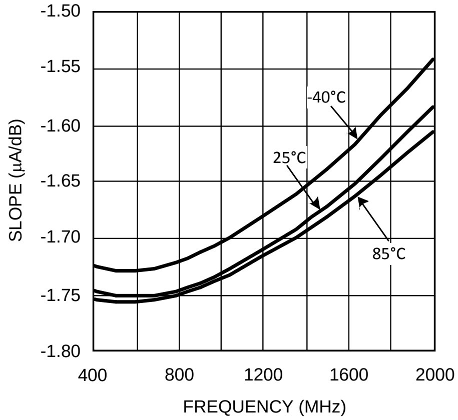


Figure 9.

Logarithmic Intercept vs. Frequency

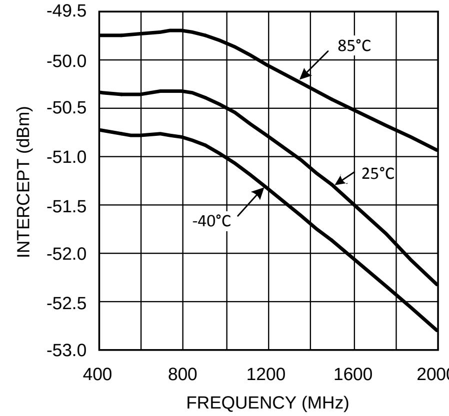


Figure 10.

RF Input Impedance vs. Frequency @ Resistance and Reactance

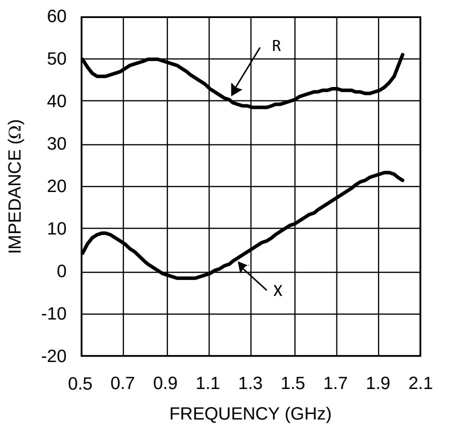


Figure 11.

Gain and Phase vs. Frequency

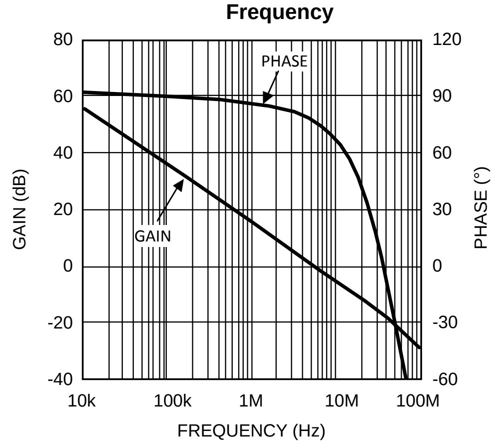


Figure 12.

I_{COMP} vs. V_{RAMP}

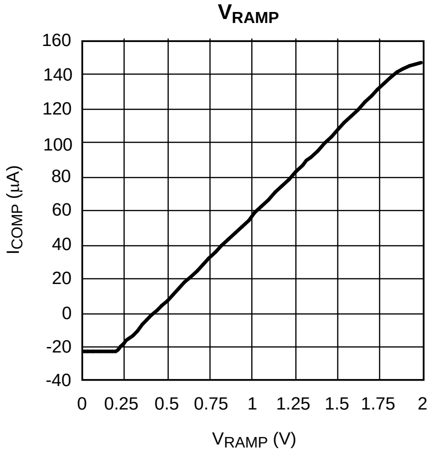


Figure 13.

P_{IN} vs. V_{RAMP}

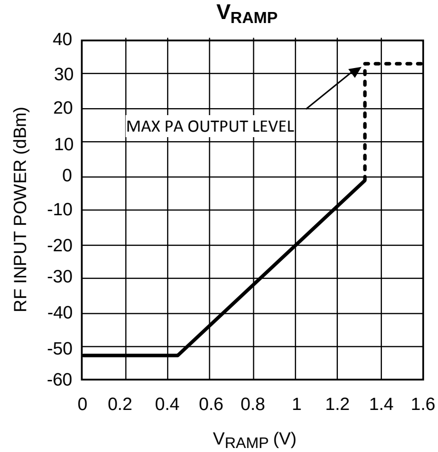


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{DD} = +2.6V, T_J = 25°C.

Sourcing Current vs. Output Voltage

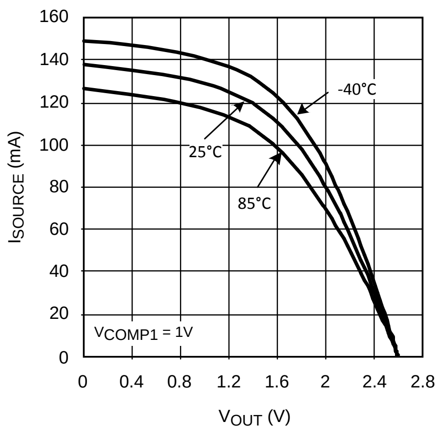


Figure 15.

Sinking Current vs. Output Voltage

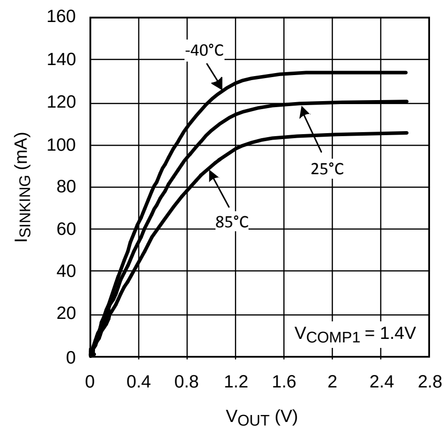


Figure 16.

Output Voltage vs. Sourcing Current

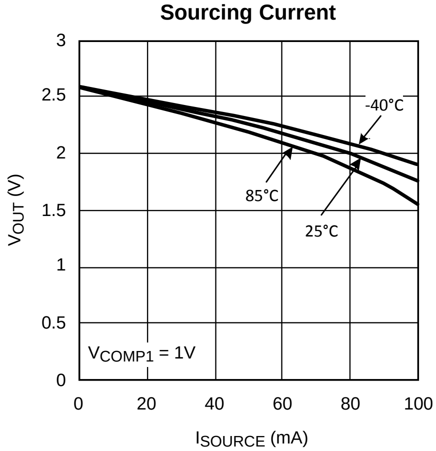


Figure 17.

Output Voltage vs. Sinking Current

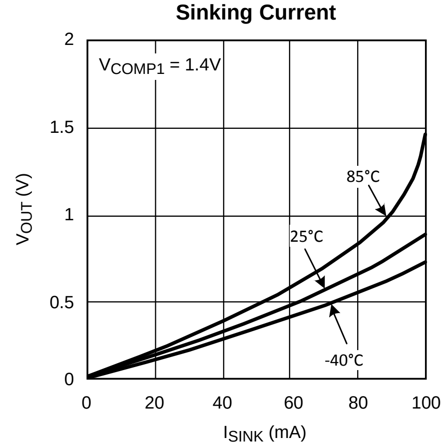


Figure 18.

Closed Loop P_{OUT} (PA) vs. V_{RAMP} @ GSM 900 MHz Band

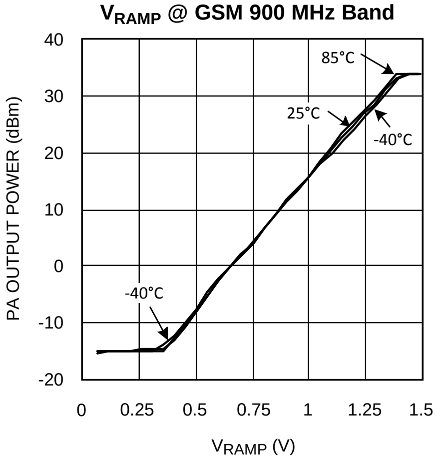


Figure 19.

Closed Loop P_{OUT} (PA) vs. V_{RAMP} @ DCS 1800 MHz Band

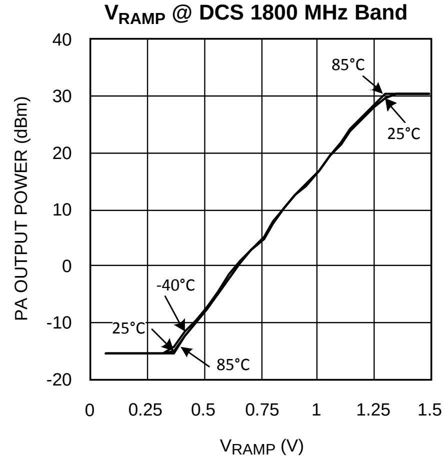


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{DD} = +2.6V, T_J = 25°C.

Closed Loop P_{OUT} (PA) vs. V_{RAMP} @ PCS 1900 MHz Band

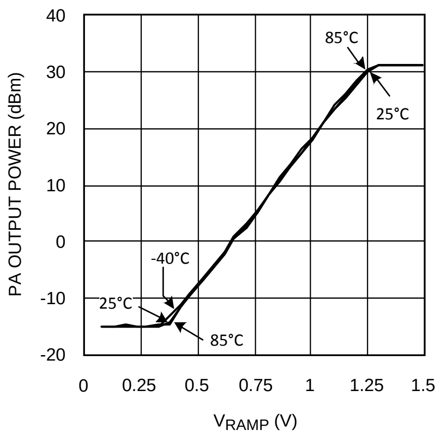


Figure 21.

Closed Loop GSM- 900 MHz Band

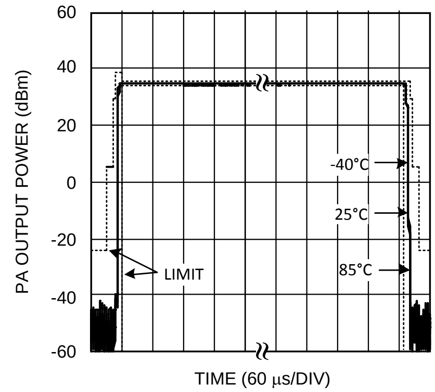


Figure 22.

Closed Loop DCS-1800 MHz Band

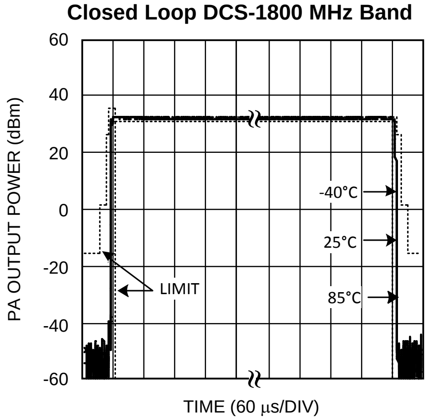


Figure 23.

Closed Loop PCS-1900 MHz Band

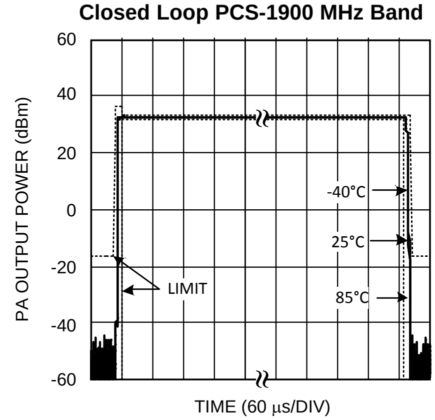


Figure 24.

APPLICATION SECTION

POWER CONTROL PRINCIPLES

The LMV242 is a member of the power loop controller family of TI, for quad-band TDMA/GSM solutions. The typical application diagram demonstrates a basic approach for implementing the quad-band solution around an RF Power Amplifier (PA). The LMV242 contains a 50 dB Logamp detector and interfaces directly with the directional coupler.

The LMV242 Base Band (control-) interface consists of 3 signals: TX_EN to enable the device, BS to select either output 1 or output 2 and V_{RAMP} to set the RF output power to the specified level. The LMV242 gives maximum flexibility to meet GSM frequency- and time mask criteria for many different single supply Power Amplifier types like HBT or MesFET in GaAs, SiGe or Si technology. This is accomplished by the programmable Ramp characteristic from the Base Band and the TX_EN signal along with the external compensation capacitor.

POWER AMPLIFIER CONTROLLED LOOP

This section gives a general overview and understanding of how a typical Power Amplifier control loop works and how to solve the most common problems confronted in the design.

General Overview

The key benefit of a PA control loop circuit is its immunity to changes in the PA gain control function. When a PA controller is used, the relationship between gain and gain control voltage (V_{APC}) of the PA is of no consequence to the overall transfer function. It is a function of the controller's V_{RAMP} voltage. Based upon the value of V_{RAMP}, the PA controller will set the gain control voltage of the PA to a level that is necessary to produce the desired output level. Any temperature dependency in the PA gain control function will be eliminated. Also, non-linearity's in the gain transfer function of the PA do not appear in the overall transfer function (P_{OUT} vs. V_{RAMP}). The only requirement is that the gain control function of the PA has to be monotonic. To achieve this, it is crucial, that the LMV242's detector is temperature stable.

Typical PA Closed Loop Control Setup

A typical setup of PA control loop is depicted in Figure 25. Beginning at the output of the Power Amplifier (PA), this signal is fed, usually via a directional coupler, to a detector. The error between the detector output current I_{DET} and the ramp current I_{RAMP}, representing the selected power setting, drives the inverting input of an op amp, configured as an integrator. A reference voltage drives the non-inverting input of the op amp. Finally the output of the integrator op amp drives the gain control input of the power amplifier, which sets the output power. The loop is stabilized when I_{DET} is equal to I_{RAMP} . Lets examine how this circuit works in detail.

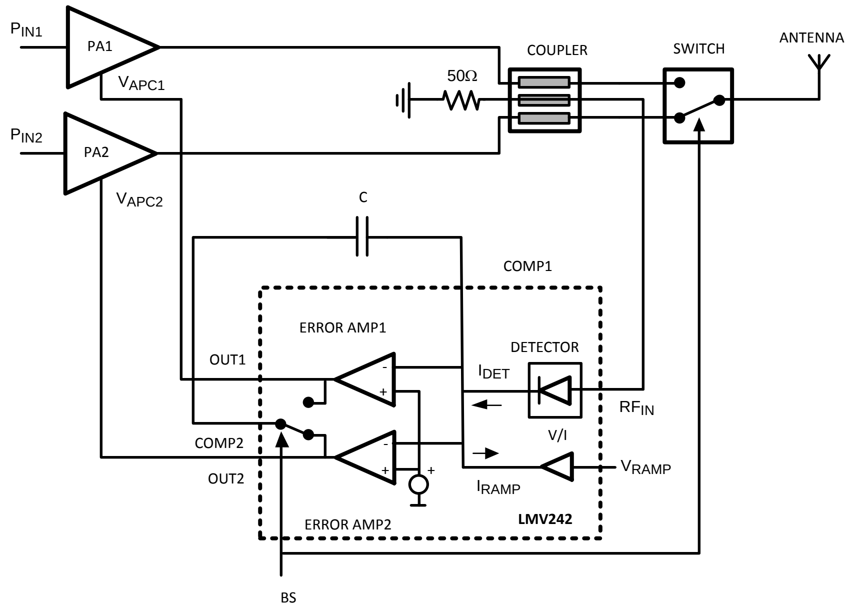


Figure 25. PA Control Loop

We will assume initially that the output of the PA is at some low level and that the V_{RAMP} voltage is at 1V. The V/I converter converts the V_{RAMP} voltage to a sinking current I_{RAMP}. This current can only come from the integrator capacitor C. Current flow from this direction increases the output voltage of the integrator. The output voltage, which drives the V_{APC} of the PA, increases the gain (we assume that the PA's gain control input has a positive sense, that is, increasing voltage increases gain). The gain will increase, thereby increasing the amplifier's output level until the detector output current equals the ramp current I_{RAMP}. At that point, the current through the capacitor will decrease to zero and the integrator output will be held constant, thereby settling the loop. If capacitor charge is lost over time, output voltage will decrease. However, this leakage will quickly be corrected by additional current from the detector. The loop stabilizes to $I_{DET} = I_{RAMP}$ thereby creating a direct relation between the V_{RAMP} set voltage and the PA output power, independent of the PA's V_{APC}-P_{OUT} characteristics.

Power Control Over Wide Dynamic Range

The circuit as described so far, has been designed to produce a temperature independent output power level. If the detector has a high dynamic range, the circuit can precisely set PA output levels over a wide power range. To set a PA output power level, the reference voltage, V_{RAMP}, is varied. To estimate the response of P_{OUT} vs. V_{RAMP}, P_{IN} vs. V_{RAMP} of the LMV242 should be known ($P_{OUT} = P_{IN}$ + attenuation as discussed in ATTENUATION BETWEEN COUPLER AND LMV242 DETECTOR).

The relation between P_{IN} and V_{RAMP} can be constructed out of 2 curves:

- I_{COMP} vs, V_{RAMP}
- V_{OUT} vs. RF Input Power (detection curve)

I_{OUT} can be calculated by dividing the V_{OUT} of the detection curve by the feedback resistor used for measuring. With the knowledge that $I_{COMP} = I_{OUT}$ in a closed loop the resulting function P_{IN} vs. V_{RAMP} is shown in Figure 26. Extra attenuation should be inserted between PA output and LMV242's P_{IN} to match their dynamic ranges.

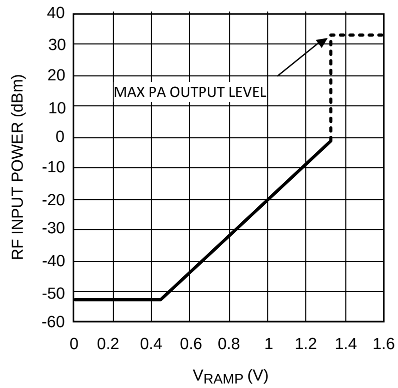


Figure 26. P_{IN} vs. V_{RAMP}

Using a closed loop to control the PA has benefits over the use of a directly controlled PA. Non-linearity's and temperature variations present in the PA transfer function do not appear in the overall transfer function, P_{OUT} vs. V_{RAMP} The response of a typical closed loop is given in Figure 27. The shape of this curve is determined by the response of the controller's detector. Therefore the detector needs to be accurate, temperature stable and preferably linear in dB to achieve a accurately controlled output power. The only requirement for the control loop is that the gain control function of the PA has to be monotonic. With a linear in dB detector, the relation between V_{RAMP} and PA output power becomes linear in dB as well, which makes calibration of the system easy.

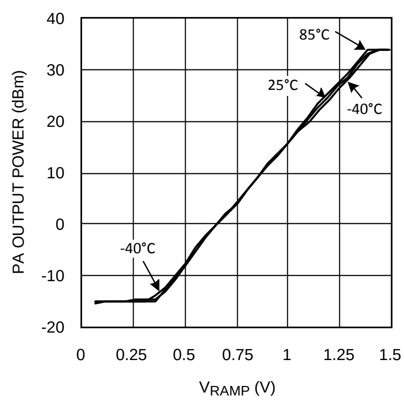


Figure 27. Closed Loop Response

The response time of the loop can be controlled by varying the RC time constant of the integrator. Setting this at a low level will result in fast output settling but can result in ringing in the output envelope. Setting the RC time constant to a high value will give the loop good stability but will increase settling time.

ATTENUATION BETWEEN COUPLER AND LMV242 DETECTOR

Figure 28 shows a practical RF power control loop realized by using TI's LMV242 with integrated RF detector. The RF signal from the PA passes through a directional coupler on its way to the antenna. Directional couplers are characterized by their coupling factor, which is in the 10 dB to 30 dB range, typical 20 dB. Because the coupled output must in its own right deliver some power (in this case to the detector), the coupling process takes some power from the main output. This manifests itself as insertion loss, the insertion loss being higher for lower coupling factors.

It is very important to choose the right attenuation between PA output and detector input to achieve power control over the full output power range of the PA. A typical value for the output power of the PA is +35.5 dBm for GSM and +30 dBm for PCS/DCS. In order to accommodate these levels into the LMV242 detection range the minimum required total attenuation is about 35 dBm (please refer to typical performance characteristics in the datasheet and Figure 26). A typical coupler factor is 20 dB. An extra attenuation of about 15 dB should be inserted.

Extra attenuation Z between the coupler and the RF input of the LMV242 can be achieved by 2 resistors R_X and R_Y according to Figure 27, where

$$Z = 20 \text{ LOG } (R_{IN} / [R_{IN} + R_Y]) \quad (1)$$

or

$$R_Y = R_{IN} \cdot \left(10^{-\frac{Z}{20}} - 1\right) \quad (2)$$

e.g. $R_Y = 300\Omega$ results in an attenuation of 16.9 dB.

To prevent reflection back to the coupler the impedance seen by the coupler should be 50Ω (R_O). The impedance consists of R_X in parallel with $R_Y + R_{IN}$. R_X can be calculated with the formula:

$$R_X = [R_O * (R_Y + R_{IN})] / R_Y \quad (3)$$

$$R_X = 50 * [1 + (50 / R_Y)] \quad (4)$$

e.g. with $R_Y = 300\Omega$, $R_{IN} = 50\Omega \rightarrow R_X = 58\Omega$.

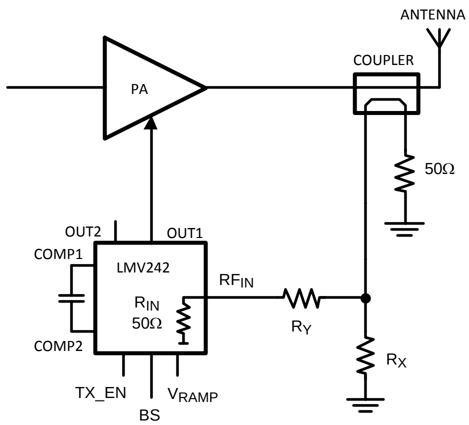


Figure 28. Simplified PA Control Loop with Extra Attenuation

BASEBAND CONTROL OF THE LMV242

The LMV242 has 3 baseband-controlled inputs:

- V_{RAMP} signal (Base band DAC ramp signal)
- TX_EN is a digital signal (performs the function “Shutdown/Transmit Enable”).
- Band Select (BS)

V_{RAMP} Signal

The actual V_{RAMP} input value sets the RF output power. By applying a certain mask shape to the “Ramp in” pin, the output voltage level of the LMV242 is adjusting the PA control voltage to get a power level (P_{OUT}/dBm) out of the PA, which is proportional to the single ramp voltage steps. The recommended V_{RAMP} voltage range for RF power control is 0.2V to 2.0V. The V_{RAMP} input will tolerate voltages from 0V to V_{DD} without malfunction or damage. The V_{RAMP} input does not change the output level until the level reaches about 206 mV, so offset voltages in the DAC or amplifier supplying the R_{AMP} signal will not cause excess RF signal output and increased power consumption.

Transmit Enable

Power consumption requirements are supported by the TX_EN function, which puts the entire chip into a power saving mode to enable maximum standby and talk time while ensuring the output does not glitch excessively during Power-up and Power-down. The device will be active in the case TX_EN = High, or otherwise go to a low power consumption shutdown mode. During shutdown the output is pulled low to minimize the output voltage.

Band Select

The LMV242 is especially suitable for PA control loops with 2 PA's. The 2 outputs to steer the V_{APCS} of the PA's can be controlled with the band select pin. When the band select is LOW output2 is selected, while output1 is selected when band select is HIGH. The not-selected output is pulled low.

Analog Output

The output is driven by a rail-to-rail amplifier capable of both sourcing and sinking. Several curves are given in the Typical performance characteristics section regarding the output. The output voltage vs. sourcing/sinking current curves show the typical voltage drop from the rail over temperature. The sourcing/sinking current vs. output voltage characteristics show the typical charging/discharging current, which the output is capable of delivering at a certain voltage. The output is free from glitches when enabled by TX_EN. When TX_EN is low, the selected output voltage is fixed or near GND.

FREQUENCY COMPENSATION

To compensate and prevent the closed loop arrangement from oscillations and overshoots at the output of the RF detector/error amplifier of the LMV242, the system can be adjusted by means of external RC components connected between Comp1 and Comp2. Exact values heavily depend on PA characteristics. A good starting point is R = 0Ω and C = 68 pF. The vast combination of PA's and couplers available preclude a generalized formula for choosing these components. Additional frequency compensation of the closed loop system can be achieved by adding a resistor (and if needed an inductor) between the LMV242's output and the V_{APC} input of the PA. Please contact TI for additional support.

TIMING DIAGRAM

In order to meet the timemask specifications for GSM, a good timing between the control signals and the RF signal is essential. According to the specifications the PA's RF output power needs to ramp within 28 µsec with minimum overshoot. To achieve this, the output of the PA controller should ramp at the same time as the RF signal from the Base Band. The ramp signal sets the controllers output to the required value, where the loop needs a certain time to set this output. Therefore the ramp should be set high some time before the output has to be high. How much time depends on the setup and the PA used. If the controllers shutdown functionality is used, the shutdown should be set high about 6 µsec before the ramp is set high.

The control loop can be configured by the following variables:

- Lead time TX_EN event vs. start GSM burst
- Lead time V_{RAMP} vs. start GSM burst
- Ramp profile
- Loop compensation

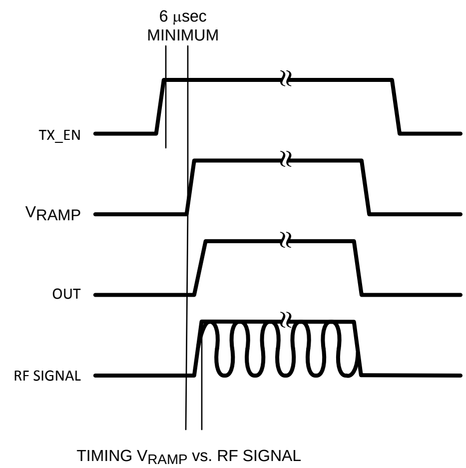


Figure 29. Timing V_{RAMP} vs. RF Signal

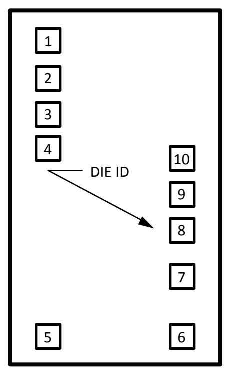


Figure 30. 10-Pad Bare Die

Die / Wafer Characteristics

Fabrication Attributes	
Physical Die Identification	LMV242A
Die Step	A

Physical Attributes	
Wafer Diameter	200 mm
Die Size (Drawn)	889 µm x 1562 µm
	35.0 mils x 61.5 mils
Thickness	216 µm Nominal
Min Pitch	123 µm Nominal

Table 1. General Die Information

Bond Pad Opening Size (min)	92 µm x 92µm
Bond Pad Metallization	0.5% Copper_Bal. Aluminum
Passivation	VOM Nitride
Back Side Metal	Bare Back
Back Side Connection	Floating

NOTE

Actual die size is rounded to the nearest micron

REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV242LD/NOPB	ACTIVE	WSON	NGY	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	242LD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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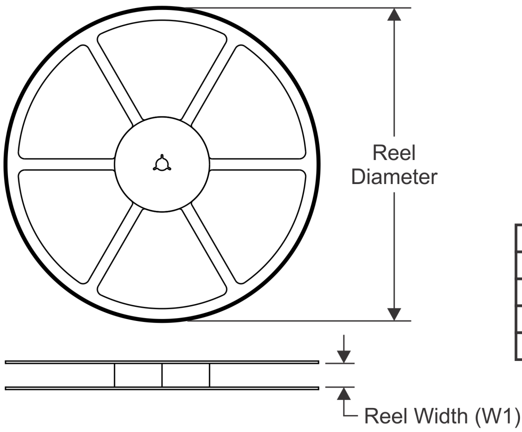
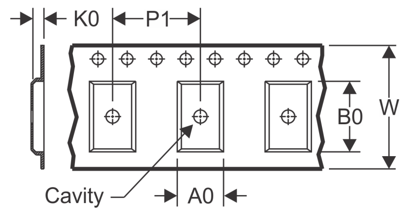
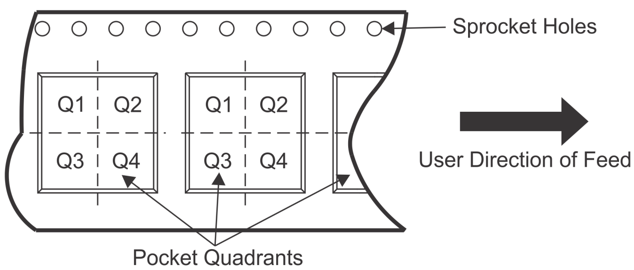


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

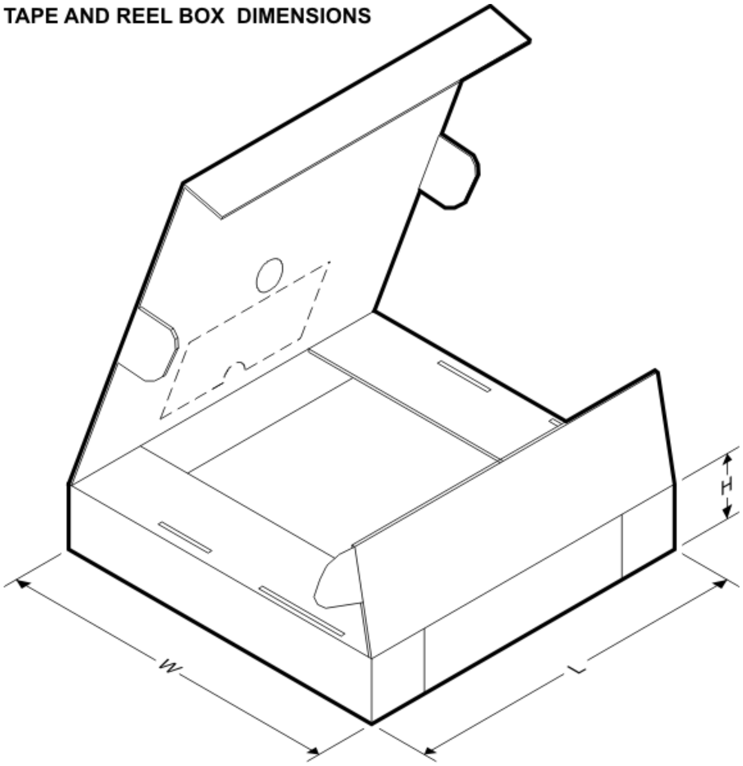
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

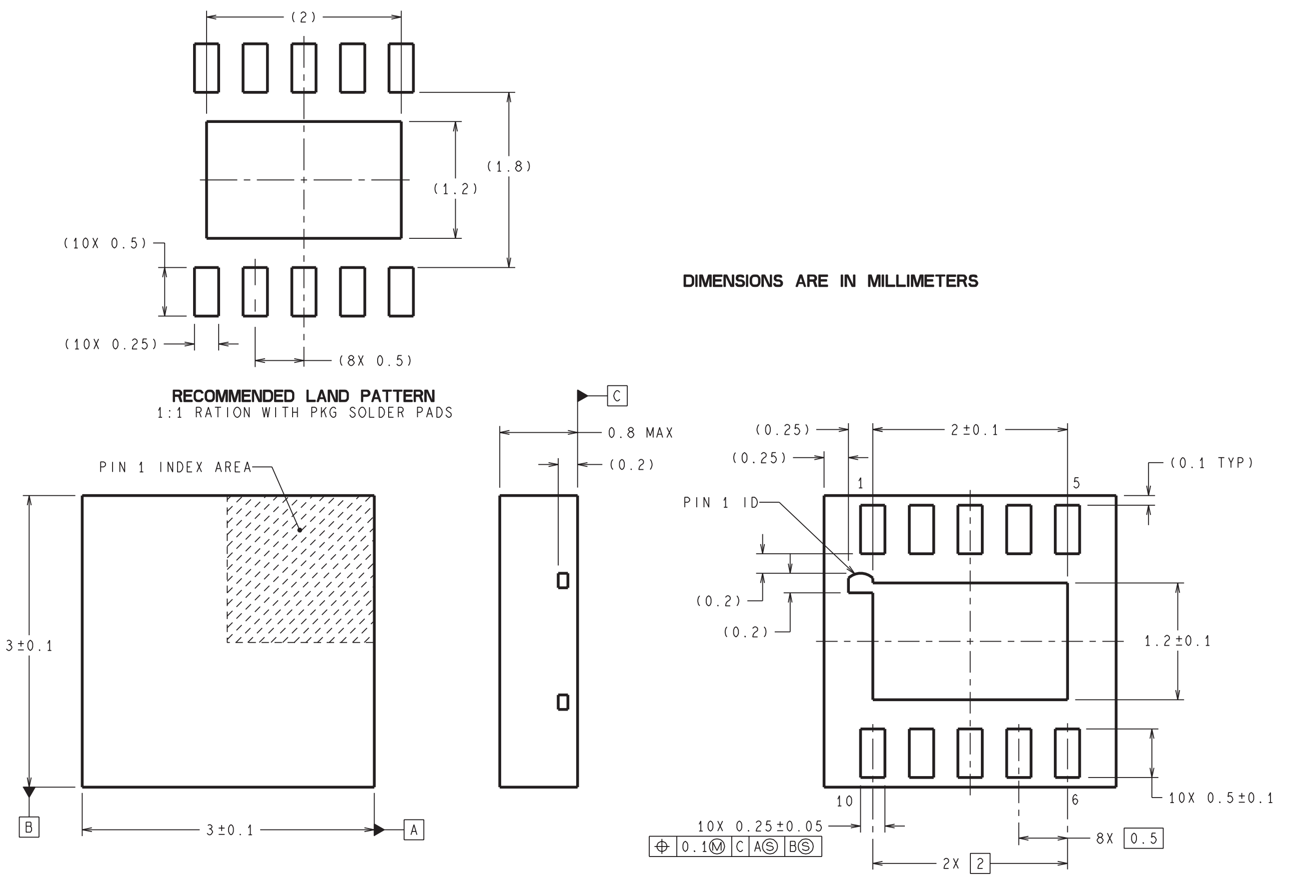
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV242LD/NOPB	WSON	NGY	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV242LD/NOPB	WSON	NGY	10	1000	210.0	185.0	35.0


(2)
(1.8)
(1.2)
(10X 0.5)
(10X 0.25)
(8X 0.5)
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS
DIMENSIONS ARE IN MILLIMETERS
PIN 1 INDEX AREA
3±0.1
B
3±0.1
A
C
0.8 MAX
(0.2)
(0.25)
(0.25)
2±0.1
(0.1 TYP)
1
5
PIN 1 ID
(0.2)
(0.2)
1.2±0.1
10
6
10X 0.5±0.1
10X 0.25±0.05
0.1 M C A S B S
8X 0.5
2X 2

LDA10A (Rev B)

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