CY7C1021DV33

1-Mbit (64 K × 16) Static RAM

Features

- Temperature ranges
  - Industrial: –40 °C to 85 °C
  - Automotive-A: –40 °C to 85 °C
- Pin-and function-compatible with CY7C1021CV33
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 60 mA @ 10 ns
- Low CMOS standby power
  - I_{SB2} = 3 mA
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages

Functional Description

The CY7C1021DV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

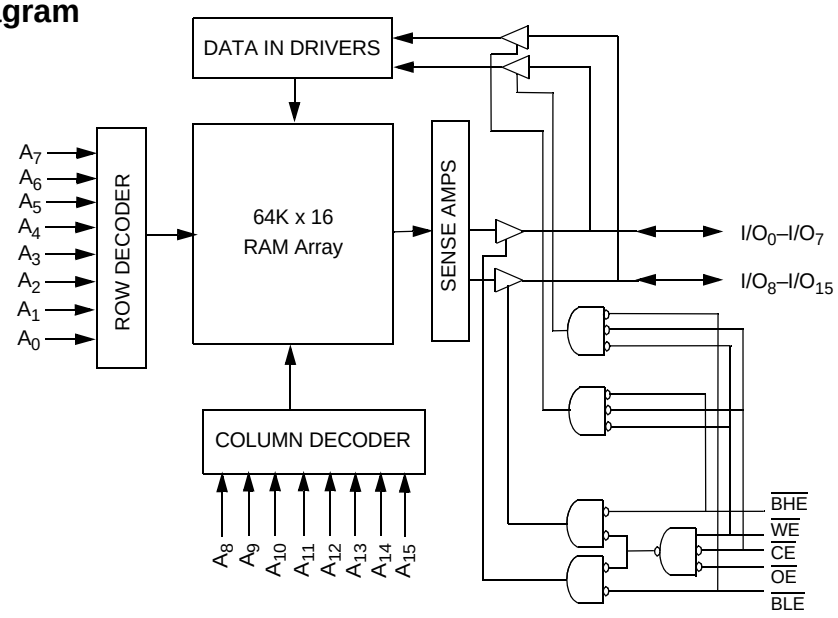
Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021DV33 is available in Pb-free 44-pin 400-Mil wide Molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages.

For a complete list of related resources, click here.

Logic Block Diagram



Contents

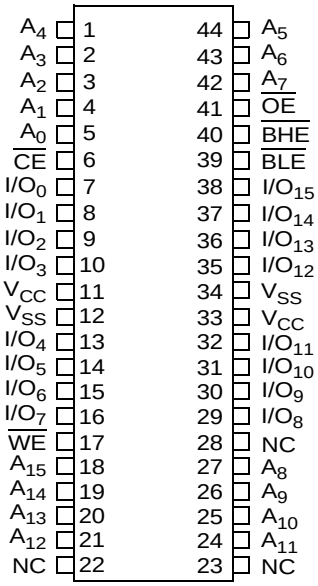
Selection Guide

Description	-10 (Industrial / Automotive-A)	Unit
Maximum access time	10	ns
Maximum operating current	60	mA
Maximum CMOS standby current	3	mA

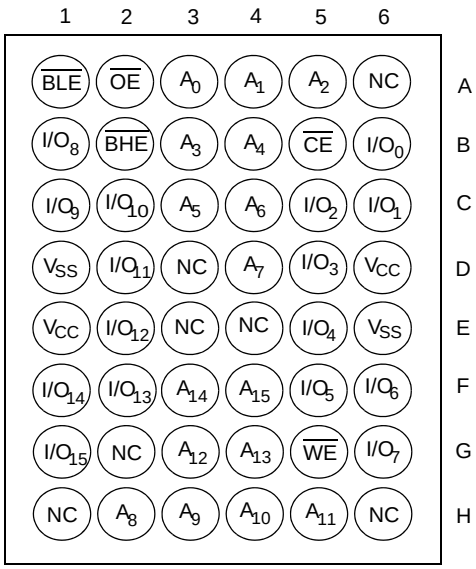
Pin Configurations

SOJ, TSOP II and VFBGA pinouts are as follows. [1]

SOJ/TSOP II
Top View



48-ball VFBGA
Top View



Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to Relative GND [2] .....–0.3 V to +4.6 V

DC Voltage applied to outputs in high Z State [2] ..... –0.3 V to V_{CC} + 0.3 V

DC input voltage [2] ..... –0.3 V to V_{CC} + 0.3 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V	10 ns
Automotive-A	–40 °C to +85 °C		10 ns

Electrical Characteristics

Over the Operating Range

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial / Automotive-A)		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage [2]			–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	100 MHz	–	60	mA
			83 MHz	–	55	mA
			66 MHz	–	45	mA
			40 MHz	–	30	mA
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	10	mA
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0		–	3	mA

Note
2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 1 V for pulse durations of less than 5 ns.

Capacitance

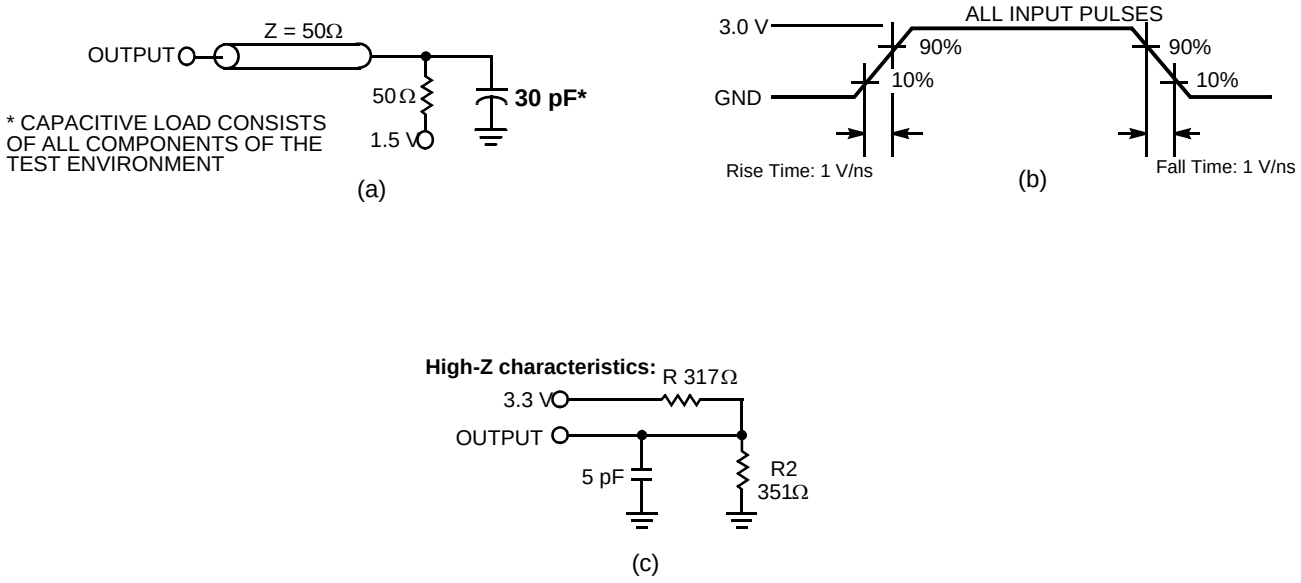
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	SOJ	TSOP II	VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	36	°C/W
Θ_{JC}	Thermal resistance (junction to case)		36.75	21.24	9	°C/W

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms [4]



Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High Z) are tested using the load conditions shown in Figure 1 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 1 (c).

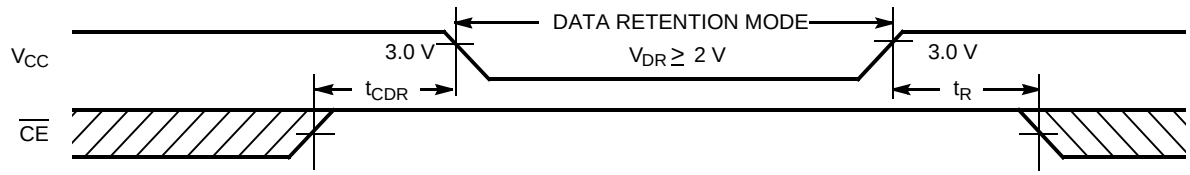
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Max	Unit
V_{DR}	V_{CC} for data retention			2	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	Industrial	–	3	mA
t_{CDR}[5]	Chip deselect to data retention time			0	–	ns
t_R[6]	Operation recovery time			t_{RC}	–	ns

Data Retention Waveform

Figure 2. Data Retention Waveform



Notes
5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

Switching Characteristics

Over the Operating Range

Parameter [7]	Description	-10 (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{power} [8]	V_{CC}(typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [9]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [9, 10]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [9]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [9, 10]	–	5	ns
t_{PU} [11]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD} [11]	$\overline{CE}$ HIGH to power-down	–	10	ns
t_{DBE}	Byte Enable to data valid	–	5	ns
t_{LZBE}	Byte Enable to low Z	0	–	ns
t_{HZBE}	Byte Disable to high Z	–	6	ns
Write Cycle [12, 13]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	8	–	ns
t_{AW}	Address set-up to write end	8	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data set-up to write end	5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [9]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [9, 10]	–	5	ns
t_{BW}	Byte enable to end of write	7	–	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
8. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of Figure 1 on page 5. Transition is measured when the outputs enter a high impedance state.
11. This parameter is guaranteed by design and is not tested.
12. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a Write and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
13. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

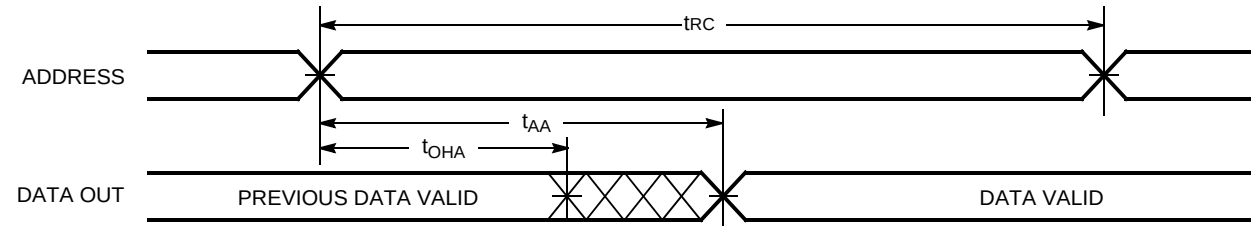
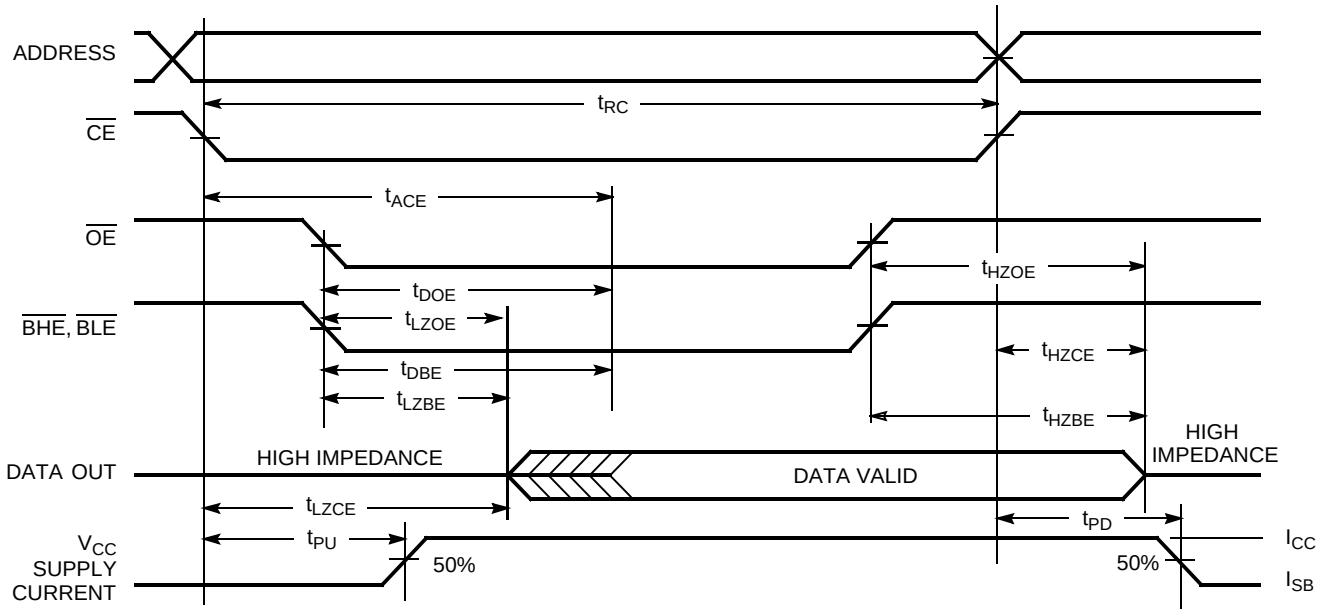


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16]



Notes
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
15. $\overline{WE}$ is HIGH for Read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18]

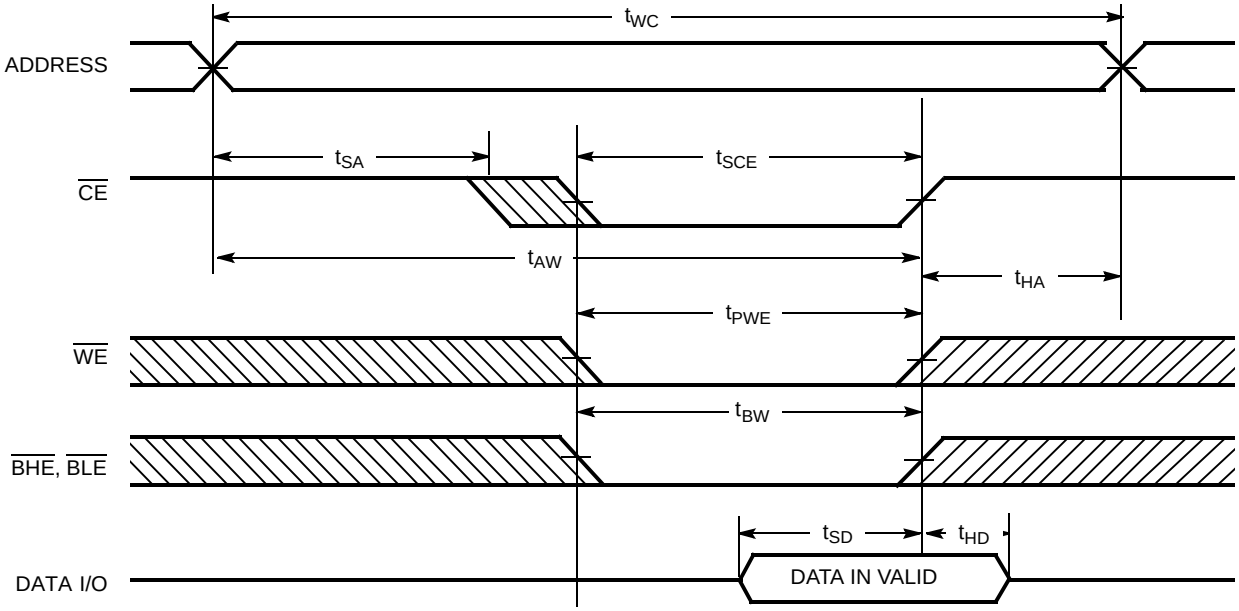
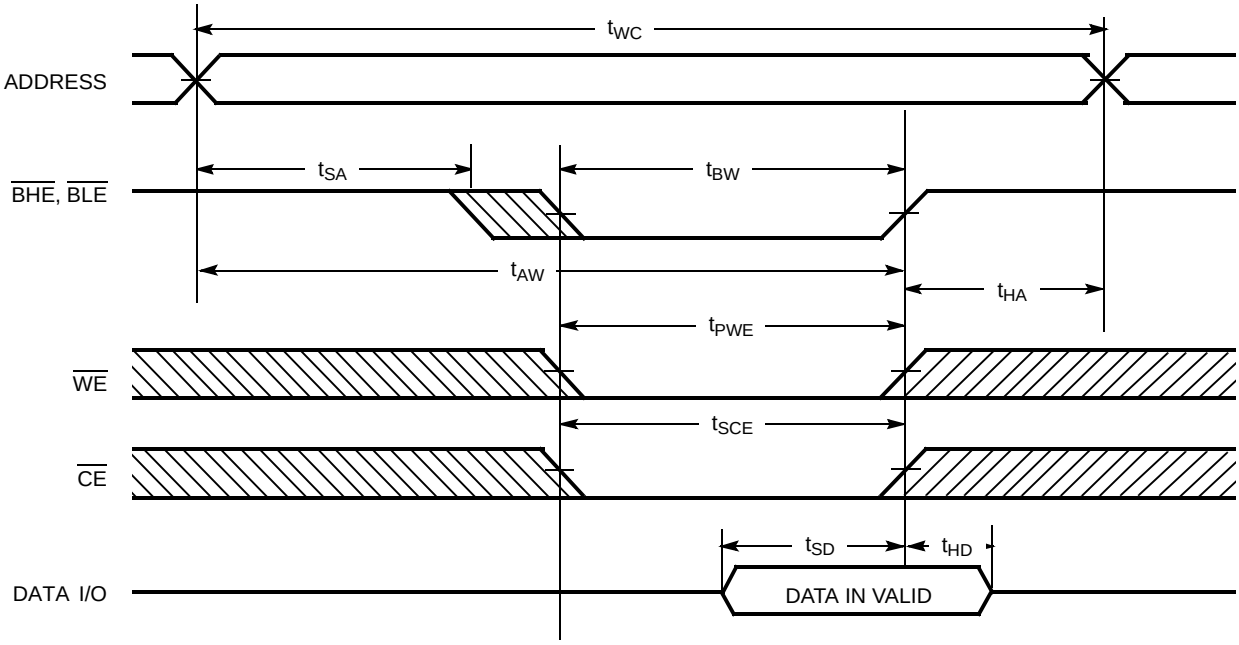


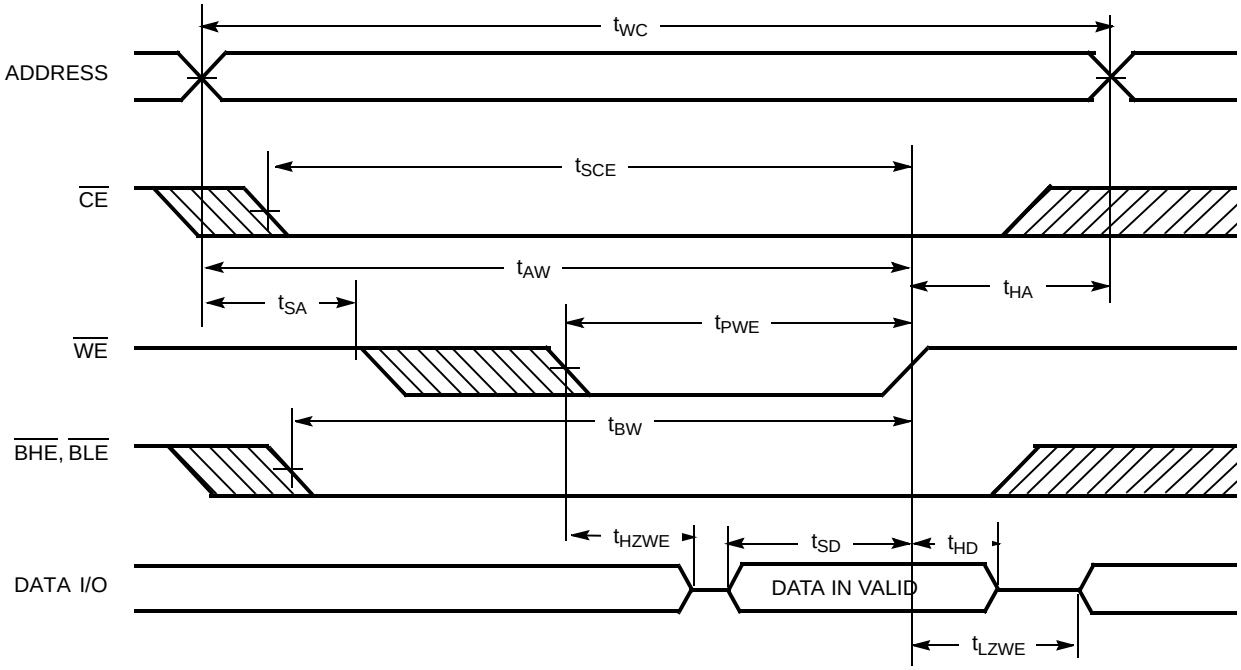
Figure 6. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
17. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [19]



Note
19. The minimum write pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

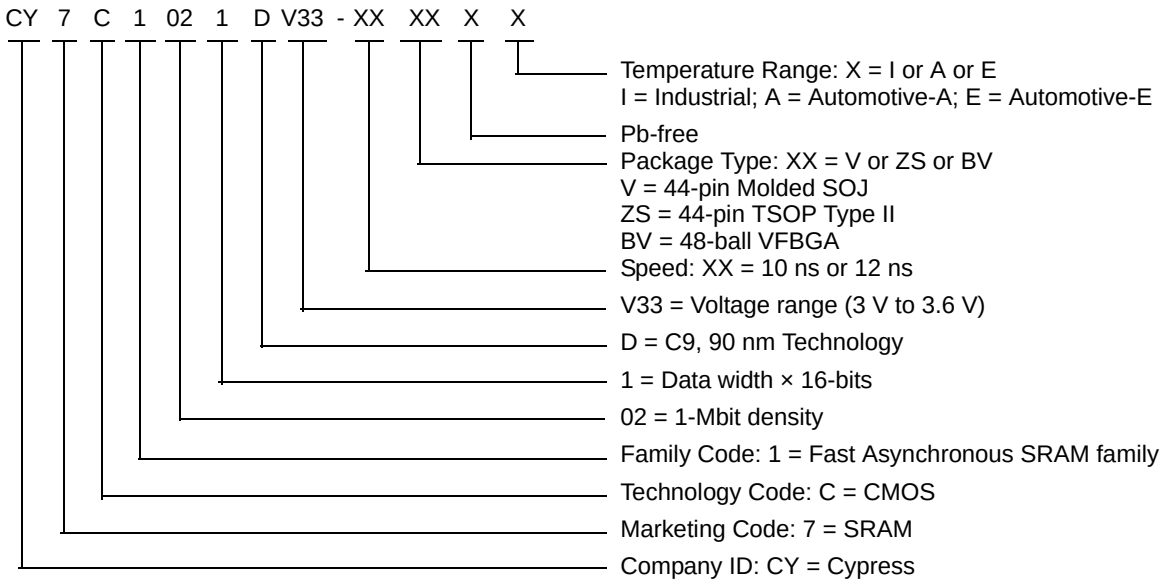
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021DV33-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1021DV33-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021DV33-10BVXI	51-85150	48-ball VFBGA (Pb-free)	
10	CY7C1021DV33-10ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A

Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 8. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082

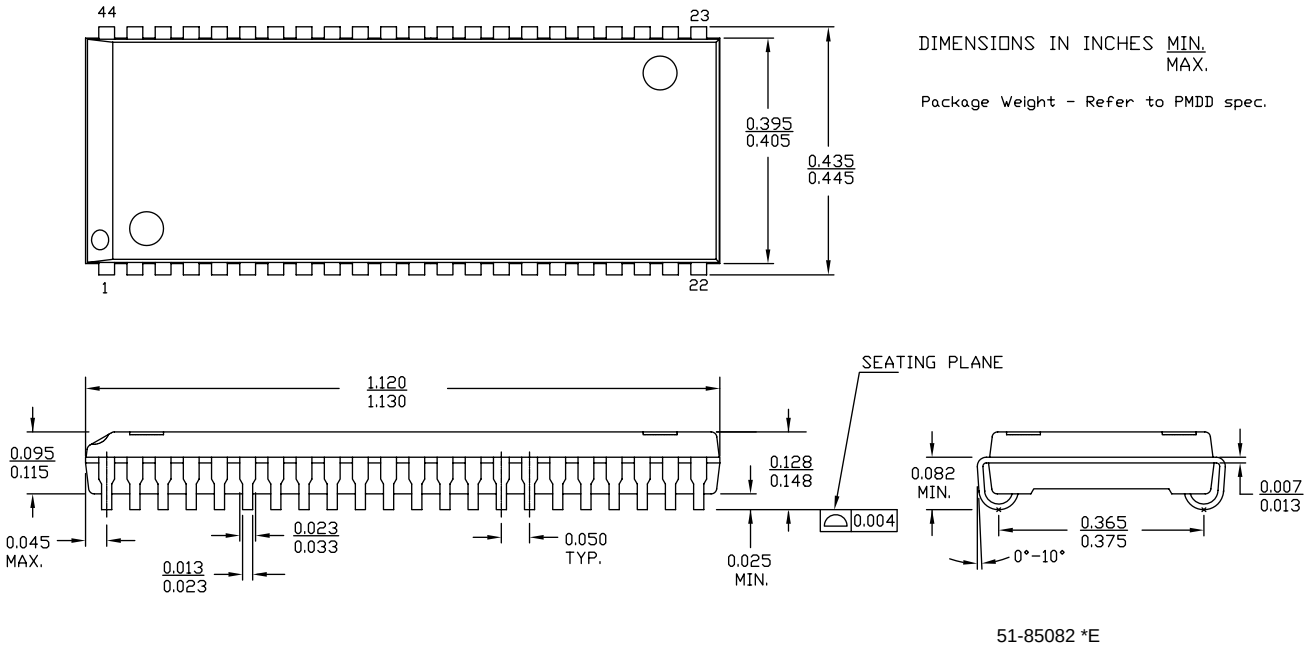
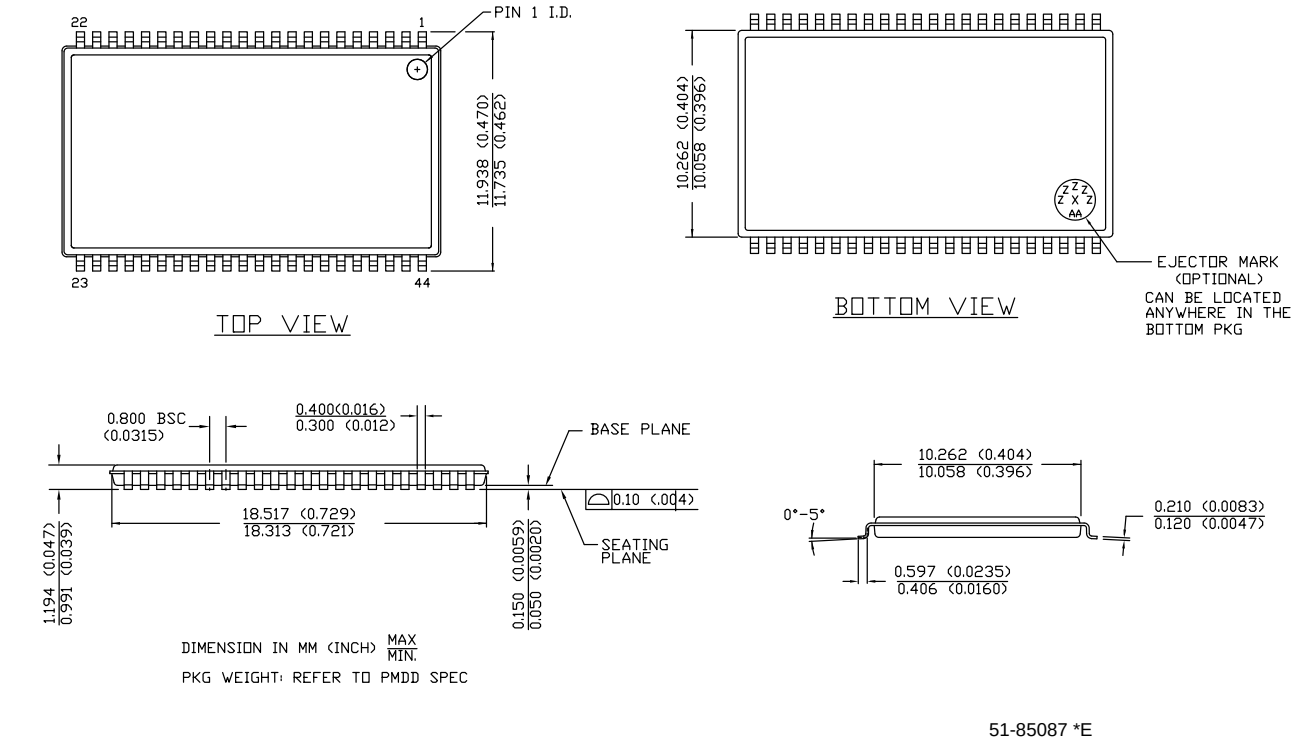
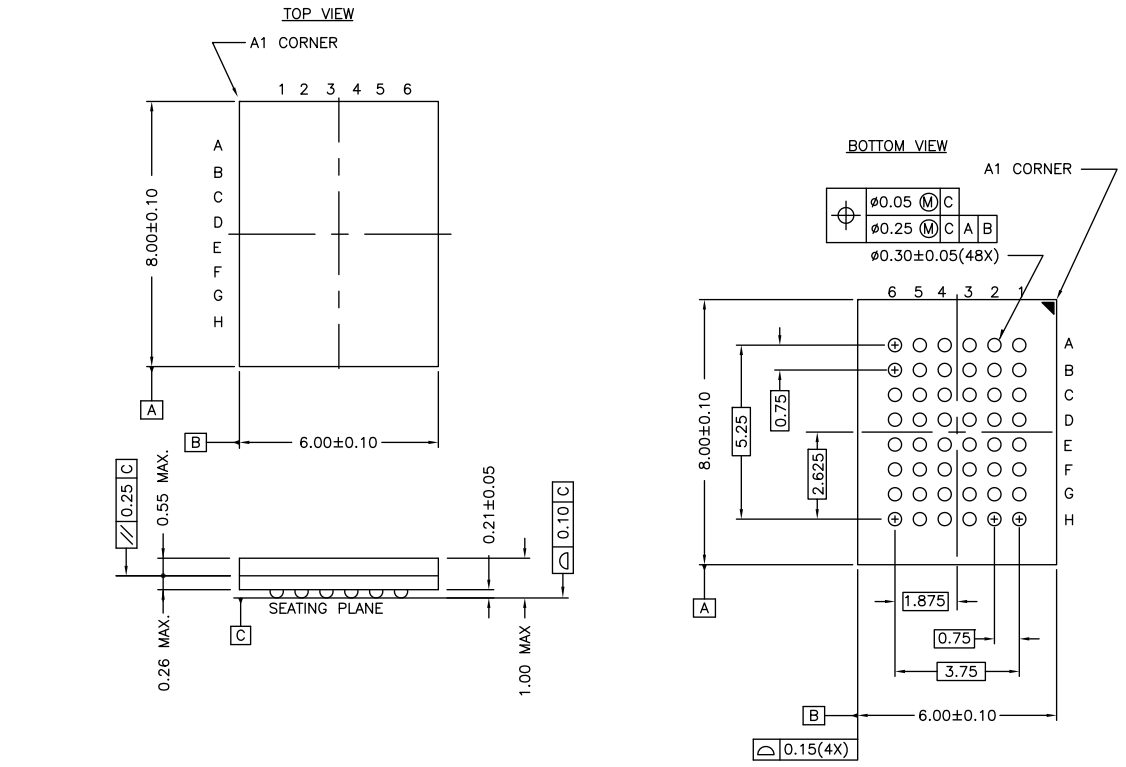


Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



Package Diagrams (continued)

Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SOJ	Small-Outline J-leaded
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021DV33, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05460				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP.
*A	233693	See ECN	RKF	Updated Electrical Characteristics (modified as per Eros (Spec # 01-02165)). Updated Ordering Information (included Pb-free offering).
*B	263769	See ECN	RKF	Updated Functional Description (Changed I/O_1–I/O_{16} to I/O_0–I/O_{15}). Updated Pin Configurations (Changed I/O_1–I/O_{16} to I/O_0–I/O_{15}). Added Data Retention Characteristics and Data Retention Waveform. Updated Switching Characteristics (Added T_{power} parameter and its details). Updated Ordering Information (Added shade, no change in part numbers).
*C	307601	See ECN	RKF	Updated Selection Guide (Reduced Speed bins to -8 and -10 ns (Removed -12 and -15 speed bins related information)). Updated Electrical Characteristics (Reduced Speed bins to -8 and -10 ns (Removed -12 and -15 speed bins related information)). Updated Switching Characteristics (Reduced Speed bins to -8 and -10 ns (Removed -12 and -15 speed bins related information)). Updated Ordering Information (Updated part numbers).
*D	520652	See ECN	VKN	Changed status from Preliminary to Final. Updated Features (Removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated Selection Guide (Removed -8 speed bin related information and incldued -12 speed bin related information). Updated Operating Range (Removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated Electrical Characteristics (Updated DC Electrical Characteristics (Removed -8 speed bin related information and included -12 speed bin related information, removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information), Updated Note 2 (Changed $V_{IH(max)}$ from V_{CC} + 2 V to V_{CC} + 1 V), added I_{CC} parameter values for the frequencies 83 MHz, 66 MHz and 40 MHz). Updated Thermal Resistance (Replaced TBD with values for all packages). Updated Switching Characteristics (Removed -8 speed bin related information and included -12 speed bin related information, removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated Data Retention Characteristics (Removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated Ordering Information (Updated part numbers).
*E	2898399	03/24/2010	AJU	Updated Package Diagrams.
*F	3109897	12/14/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.

Document History Page (continued)

Document Title: CY7C1021DV33, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05460				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*G	3421856	10/25/2011	TAVA	Updated Features (Removed Automotive-E Operating range related information). Updated Selection Guide (Removed Automotive-E Operating range related information, removed -12 speed bin related information). Updated Operating Range (Removed Automotive-E Operating range related information, removed -12 speed bin related information). Updated Electrical Characteristics (Updated DC Electrical Characteristics (Removed Automotive-E Operating range related information, removed -12 speed bin related information)). Updated Switching Characteristics (Removed Automotive-E Operating range related information, removed -12 speed bin related information). Updated Data Retention Characteristics (Removed Automotive-E Operating range related information). Updated Switching Waveforms. Updated Ordering Information (Updated part numbers). Updated Package Diagrams. Updated to new template.
*H	4578364	11/24/2014	MEMJ	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Switching Characteristics: Added Note 13 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 19 and referred the same note in Figure 7. Updated Ordering Information (Removed shade, no change in part numbers). Updated Package Diagrams: spec 51-85082 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *D to *E. spec 51-85150 – Changed revision from *G to *H. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com