

N-channel 850 V, 0.2 Ω typ., 19 A Zener-protected SuperMESH™ 5 Power MOSFET in a TO-247 package

Datasheet - production data

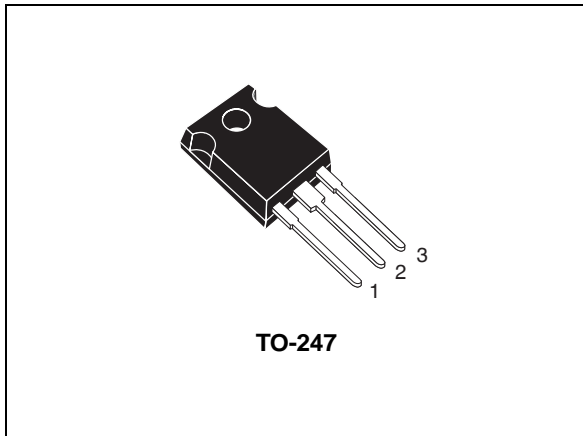
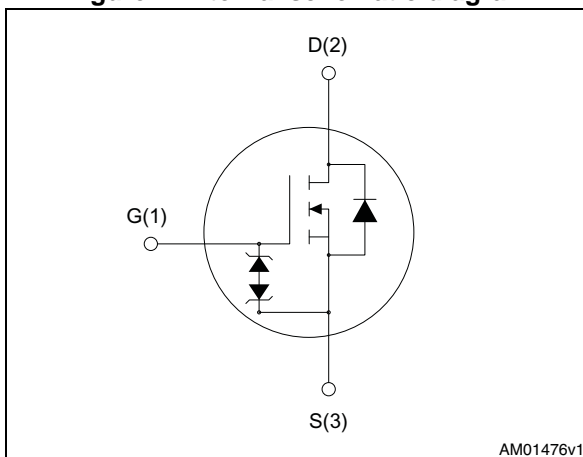


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)max}	I _D	P _W
STW23N85K5	850 V	< 0.275 Ω	19	250

- Worldwide best R_{DS(on)}* area
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STW23N85K5	23N85K5	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	19	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	76	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	6	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 19\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$, $V_{DD} = 680\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max.	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch², 2oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	850			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 850\text{ V}$, $V_{DS} = 850\text{ V}$, $T_c = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 9.5\text{ A}$		0.2	0.275	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			1650		pF
C_{oss}	Output capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	115	-	pF
C_{rss}	Reverse transfer capacitance			2		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }680\text{ V}$	-	185	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			72		
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 680\text{ V}$, $I_D = 19\text{ A}$		38		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$	-	11	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14)		20		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 9.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13 and Figure 18)		22		ns
t_r	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		55			ns
t_f	Fall time		8			ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19	A
I_{SDM}	Source-drain current (pulsed)		76	A		
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 19\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 19\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 15)	-	510		ns
Q_{rr}	Reverse recovery charge		11	μC		
I_{RRM}	Reverse recovery current		43	A		
t_{rr}	Reverse recovery time	$I_{SD} = 19\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15)	-	684		ns
Q_{rr}	Reverse recovery charge		14	μC		
I_{RRM}	Reverse recovery current		41	A		

1. Pulsed: pulse duration = $300\ \mu\text{s}$, duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} \pm 1\text{ mA}$, (open drain)	30	-	-	V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

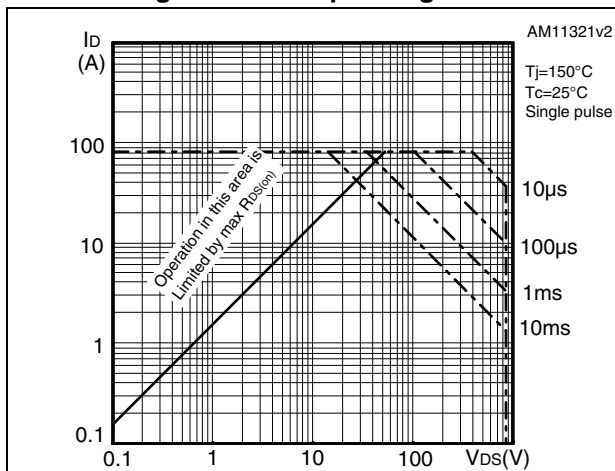


Figure 3. Thermal impedance

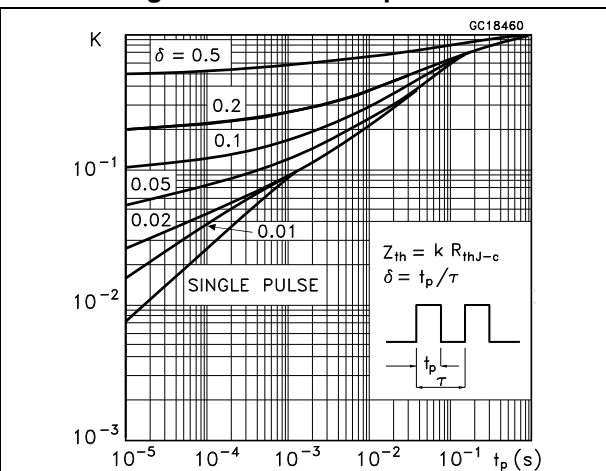


Figure 4. Output characteristics

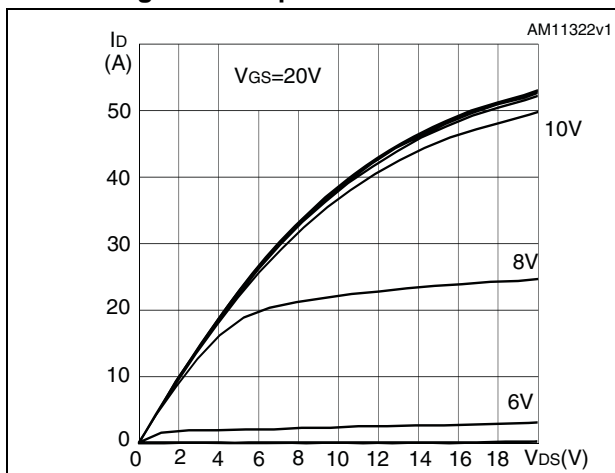


Figure 5. Transfer characteristics

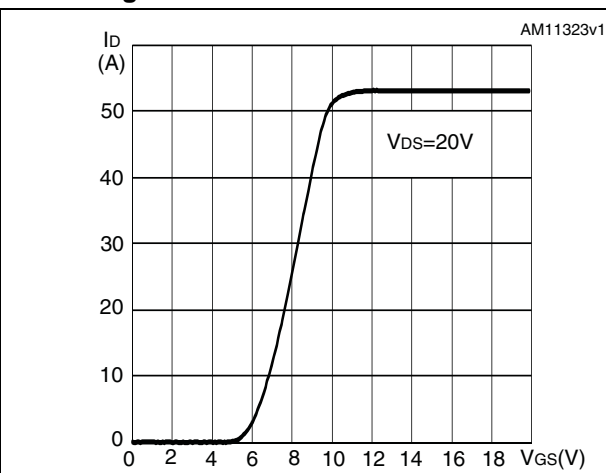


Figure 6. Normalized BV_{DSS} vs temperature

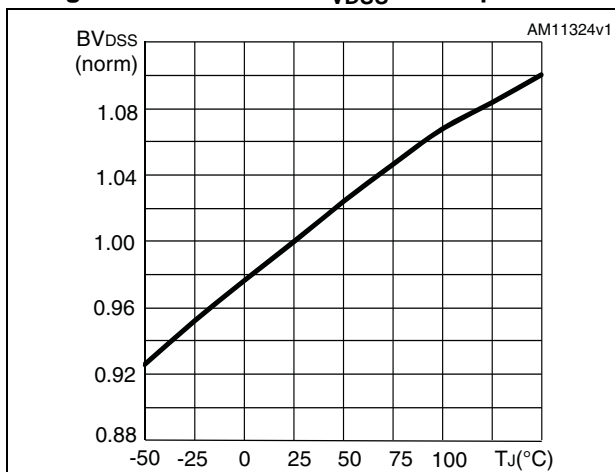


Figure 7. Static drain-source on-resistance

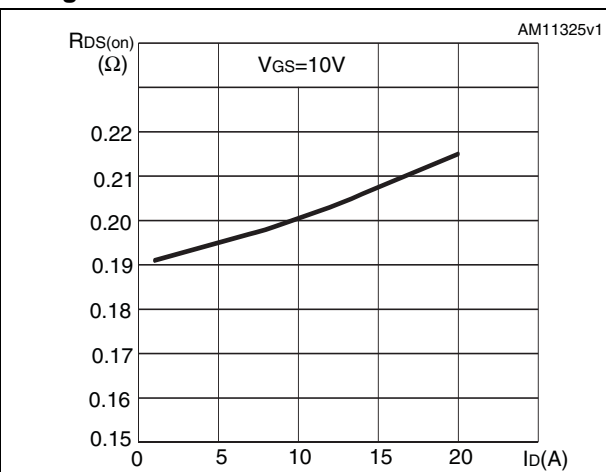


Figure 8. Gate charge vs gate-source voltage

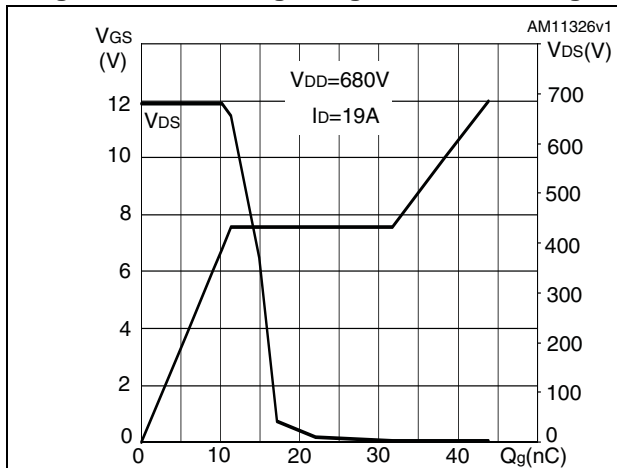


Figure 9. Capacitance variations

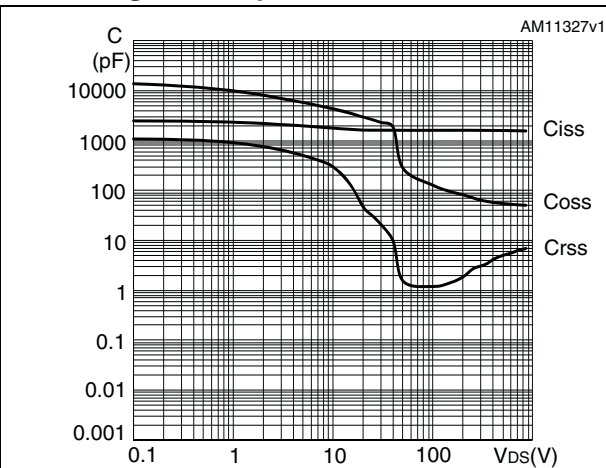


Figure 10. Normalized gate threshold voltage vs temperature

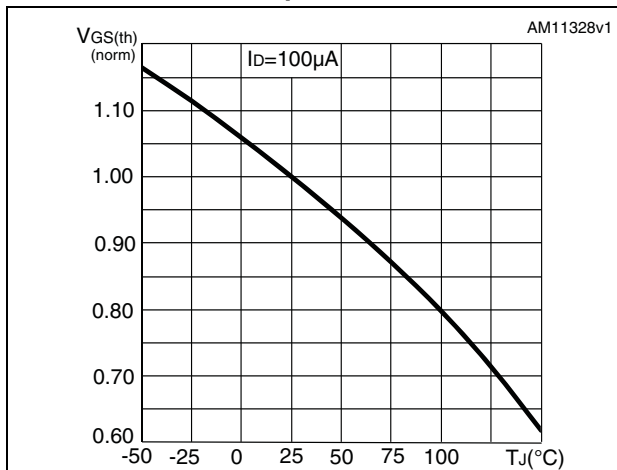


Figure 11. Normalized on-resistance vs temperature

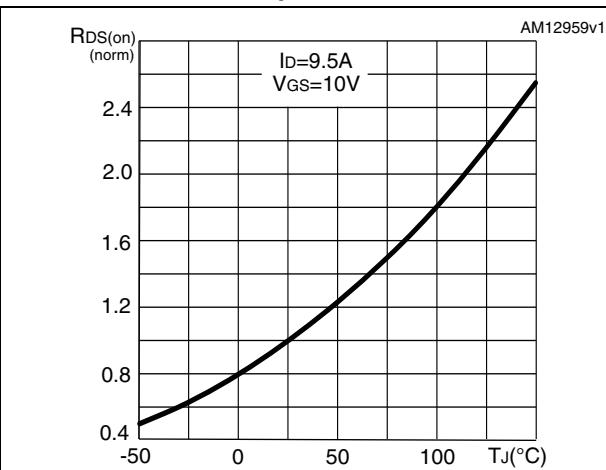
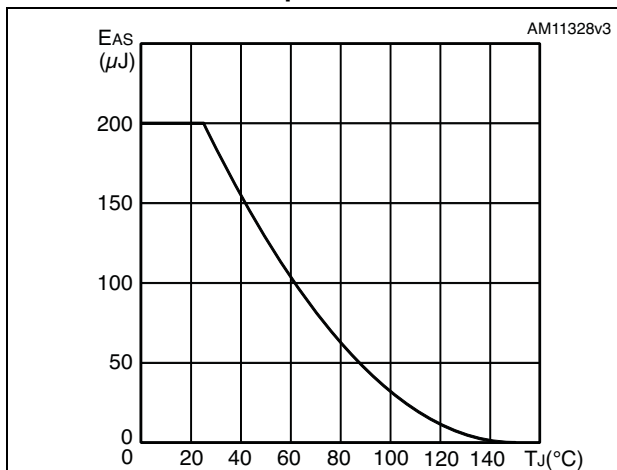
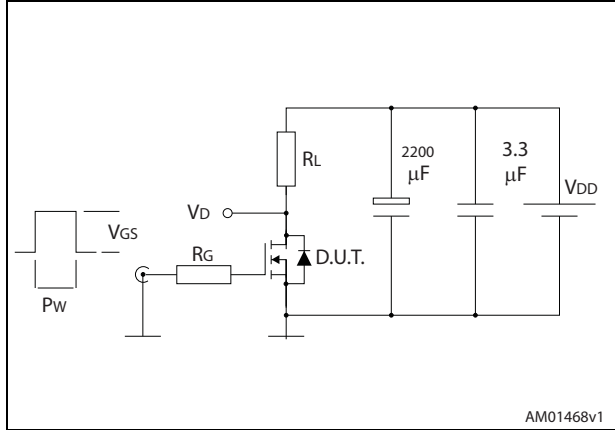


Figure 12. Maximum avalanche energy vs temperature



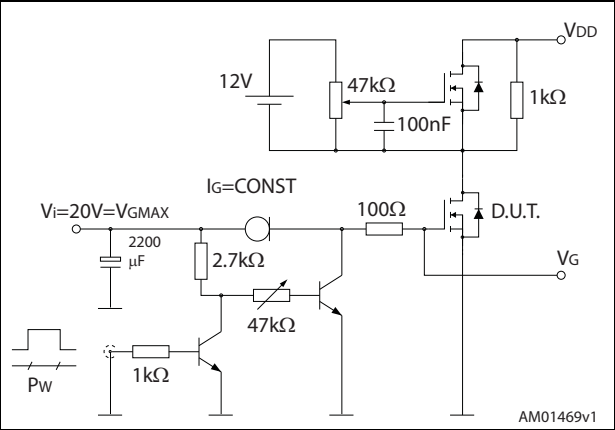
3 Test circuits

Figure 13. Switching times test circuit for resistive load



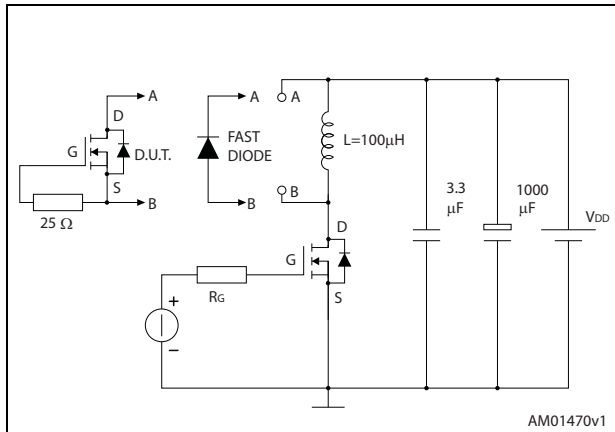
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Figure 14. Gate charge test circuit



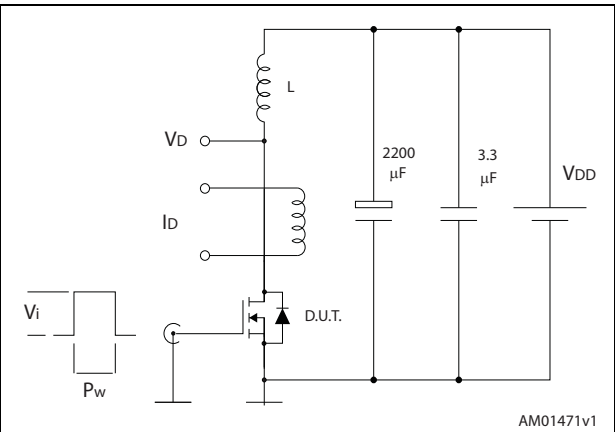
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Figure 15. Test circuit for inductive load switching and diode recovery times



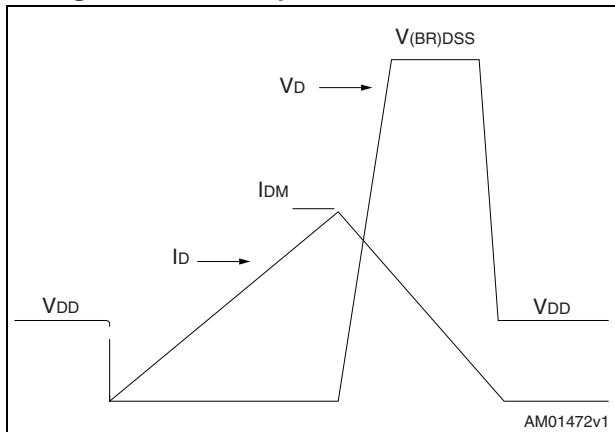
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Figure 16. Unclamped inductive load test circuit



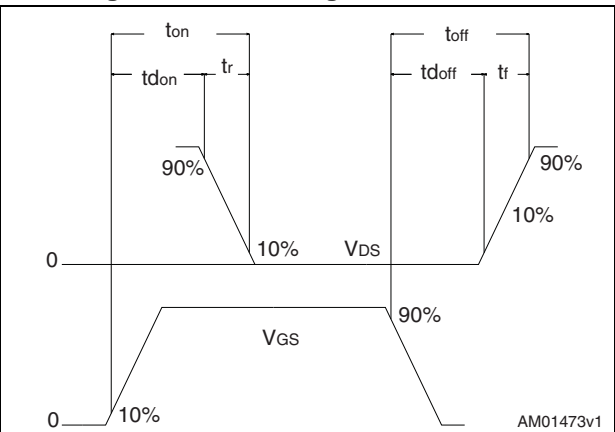
AM01471v1

Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 19. TO-247 drawing

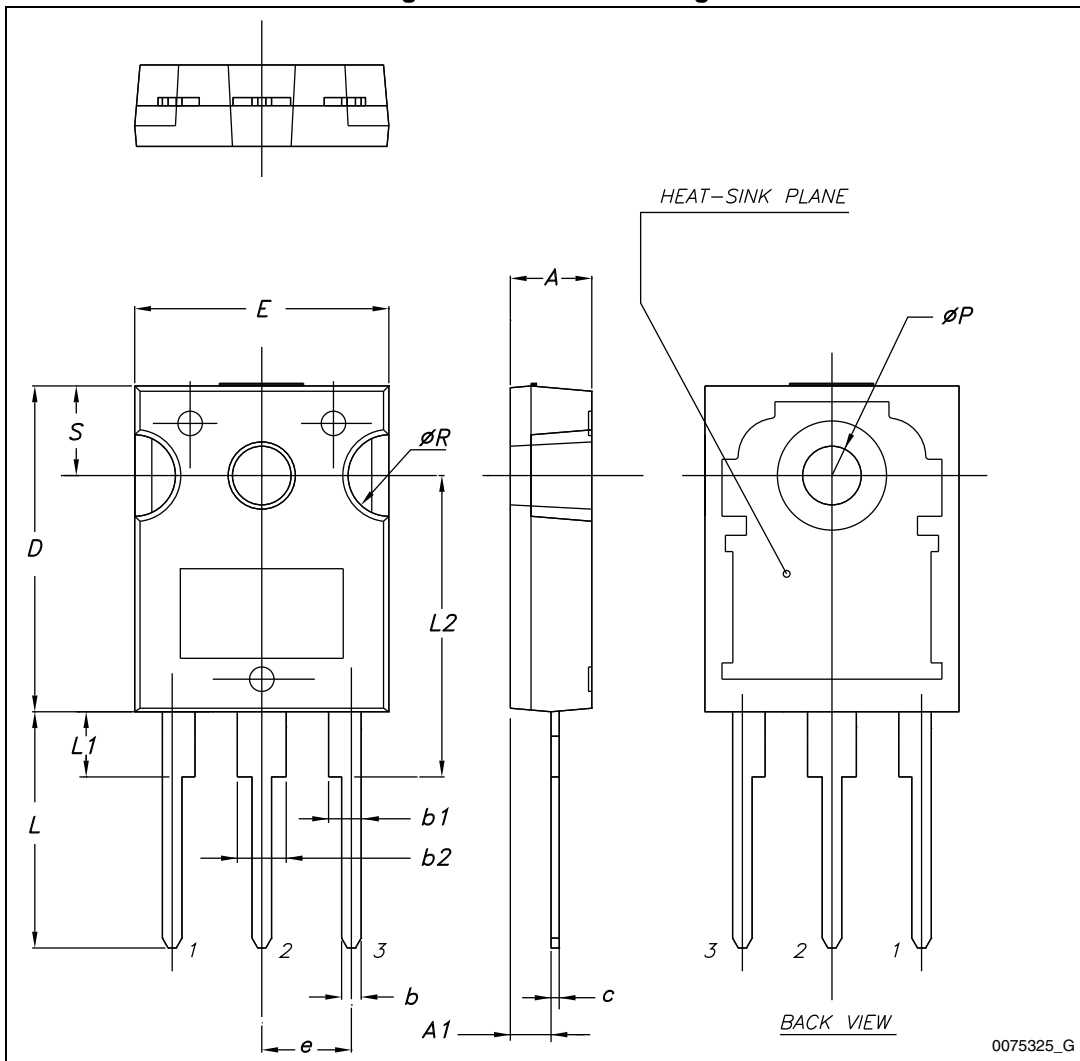


Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
06-Aug-2012	1	First release.
21-Jan-2014	2	Document status promoted from preliminary to production data. Added Figure 12: Maximum avalanche energy vs temperature .

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