



## FXLA0104

# Low-Voltage Dual-Supply 4-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

### Features

- Bi-Directional Interface between Two Levels: from 1.1 V to 3.6 V
- Fully Configurable: Inputs and Outputs Track  $V_{CC}$
- Non-Preferential Power-Up; Either  $V_{CC}$  May Be Powered Up First
- Outputs Switch to 3-State if Either  $V_{CC}$  is at GND
- Power-Off Protection
- Bus-Hold on Data Inputs Eliminates the Need for Pull-Up Resistors; Do Not Use Pull-Up Resistors on A or B Ports
- Control Input (OE) Referenced to  $V_{CCA}$  Voltage
- Available in the 12-Lead, 1.7 mm x 2.0 mm UMLP Package
- Direction Control Not Necessary
- 100 Mbps Throughput when Translating Between 1.8 V and 2.5 V
- ESD Protection Exceeds:
  - 6 kV HBM (per JESD22-A114 & Mil Std 883e 3015.7)
  - 2 kV CDM (per ESD STM 5.3)

### Description

The FXLA0104 is a configurable dual-voltage supply translator for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the  $V_{CCA}$  level and the B port tracks the  $V_{CCB}$  level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

The device remains in three-state as long as either  $V_{CC}=0V$ , allowing either  $V_{CC}$  to be powered up first. Internal power-down control circuits place the device in 3-state if either  $V_{CC}$  is removed.

The OE input, when LOW, disables both the A and B ports by placing them in a 3-state condition. The OE input is supplied by  $V_{CCA}$ .

The FXLA0104 supports bi-directional translation without the need for a direction control pin. The two ports of the device have auto-direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

### Applications

- Cell Phone, PDA, Digital Camera, Portable GPS

### Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FXLA0104QFX	-40 to 85°C	XU	12-Lead, 1.7 mm x 2.0 mm Ultrathin Molded Leadless Package (UMLP)	5000 Units Tape and Reel

## Pin Configuration

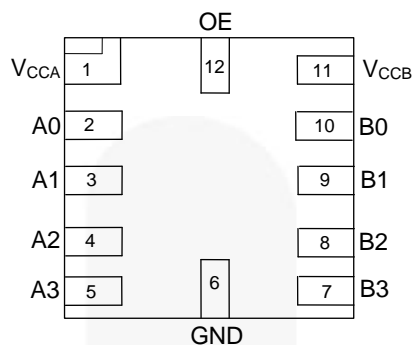


Figure 1. Top Through View

## Pin Definitions

Pin #	Name	Description
1	$V_{CCA}$	A-Side Power Supply
2	A0	A-Side Inputs or 3-State Outputs
3	A1	A-Side Inputs or 3-State Outputs
4	A2	A-Side Inputs or 3-State Outputs
5	A3	A-Side Inputs or 3-State Outputs
6	GND	Ground
7	B3	B-Side Inputs or 3-State Outputs
8	B2	B-Side Inputs or 3-State Outputs
9	B1	B-Side Inputs or 3-State Outputs
10	B0	B-Side Inputs or 3-State Outputs
11	$V_{CCB}$	B-Side Power Supply
12	OE	Output Enable Input

Functional Diagram

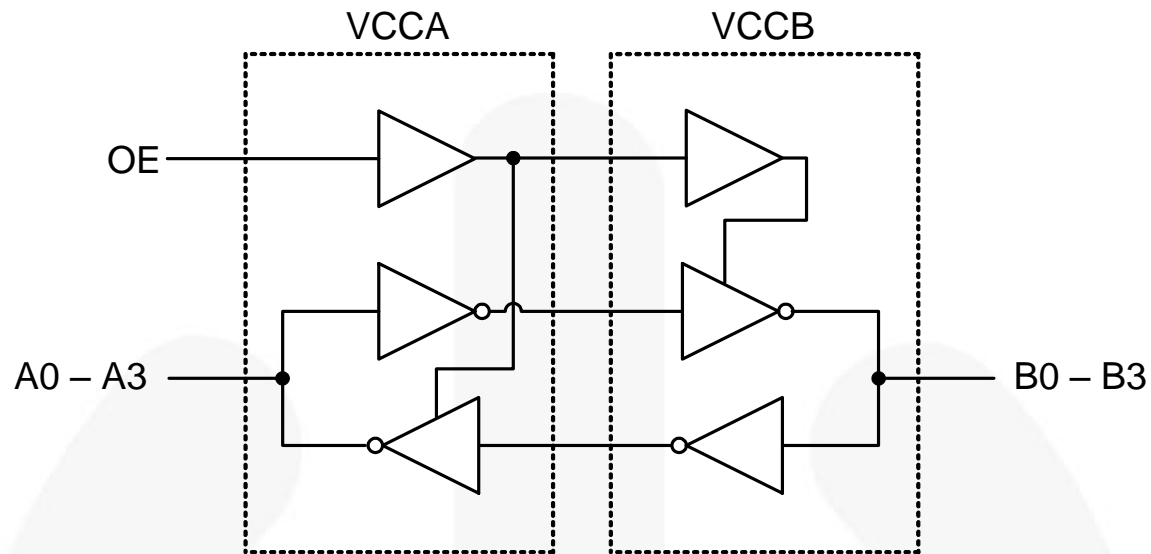


Figure 2. Functional Diagram

Function Table

Control	Outputs
OE	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	$V_{CCA}$	-0.5	4.6	V
		$V_{CCB}$	-0.5	4.6	
$V_I$	DC Input Voltage	I/O Ports A and B	-0.5	4.6	V
		Control Input (OE)	-0.5	4.6	
$V_O$	Output Voltage <sup>(2)</sup>	Output 3-State	-0.5	4.6	V
		Output Active ( $A_n$ )	-0.5	$V_{CCA} + 0.5$	
		Output Active ( $B_n$ )	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
$I_{OK}$	DC Output Diode Current	$V_O < 0V$		-50	mA
		$V_O > V_{CC}$		+50	
$I_{OH}/I_{OL}$	DC Output Source/Sink Current		-50	+50	mA
$I_{CC}$	DC $V_{CC}$ or Ground Current (per Supply Pin)			$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
$P_D$	Power Dissipation			17	mW
ESD	Electrostatic Discharge Capability	Human Body Model (per JESD22-A114 & Mil Std 883e 3015.7)		6	kV
		Charged Device Model (per ESD STM 5.3)		2	

### Notes:

- $I_O$  absolute maximum ratings must be observed.
- All unused inputs and input/outputs must be held at  $V_{CCi}$  or GND.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
$V_{CC}$	Power Supply	Operating $V_{CCA}$ or $V_{CCB}$	1.1	3.6	V
$V_{IN}$	Input Voltage	Ports A and B	0	3.6	V
		Control Input (OE)	0	$V_{CCA}$	V
$T_A$	Operating Temperature, Free Air		-40	+85	°C
dt/dV	Minimum Input Edge Rate	$V_{CCA/B} = 1.1$ to 3.6 V		10	ns/V
$\theta_{JA}$	Thermal Resistance: Junction-to-Ambient			300	°C/W
$\theta_{JC}$	Thermal Resistance: Junction-to-Case			165	°C/W

## Power-Up/Power-Down Sequence

FXL translators offer an advantage in that either  $V_{CC}$  may be powered up first. This benefit derives from the chip design. When either  $V_{CC}$  is at 0V, outputs are in a high-impedance state. The control input (OE) is designed to track the  $V_{CCA}$  supply.

The recommended power-up sequence is:

1. Apply power to the first  $V_{CC}$ .
2. Apply power to the second  $V_{CC}$ .
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either  $V_{CC}$ .
3. Remove power from other  $V_{CC}$ .

## Pull-Up/Pull-Down Resistors

Do not use pull-up or pull-down resistors. This device has bus-hold circuits; pull-up or pull-down resistors are not recommended because they interfere with the output state. The current through these resistors may exceed the hold drive,  $I_{I(HOLD)}$  and/or  $I_{I(OD)}$  bus-hold currents, resulting in data transition and/or auto-direction sensing failures. The bus-hold feature eliminates the need for extra resistors.

## DC Electrical Characteristics

$T_A = -40$  to  $85^\circ\text{C}$

Symbol	Parameter	Condition	$V_{CCA}$ (V)	$V_{CCB}$ (V)	Min.	Typ.	Max.	Unit
$V_{IHA}$	High-Level Input Voltage	Data Inputs $A_n$ Control Pin OE	2.70 to 3.60	1.10 to 3.60	2.00			V
			2.30 to 2.70		1.60			
			1.65 to 2.30		$.65 \times V_{CCA}$			
			1.40 to 1.65		$.65 \times V_{CCA}$			
			1.10 to 1.40		$.90 \times V_{CCA}$			
$V_{IHB}$	High-Level Input Voltage	Data Inputs $B_n$	1.10 to 3.60	2.70 to 3.60	2.00			V
				2.30 to 2.70	1.60			
				1.65 to 2.30	$.65 \times V_{CCB}$			
				1.40 to 1.65	$.65 \times V_{CCB}$			
				1.10 to 1.40	$.90 \times V_{CCB}$			
$V_{ILA}$	Low-Level Input Voltage	Data Inputs $A_n$ Control Pin OE	2.70 to 3.60	1.10 to 3.60			.80	V
			2.30 to 2.70				.70	
			1.65 to 2.30				$.35 \times V_{CCA}$	
			1.40 to 1.65				$.35 \times V_{CCA}$	
			1.10 to 1.40				$.10 \times V_{CCA}$	
$V_{ILB}$	Low-Level Input Voltage	Data Inputs $B_n$	1.10 to 3.60	2.70 to 3.60			.80	V
				2.30 to 2.70			.70	
				1.65 to 2.30			$.35 \times V_{CCB}$	
				1.40 to 1.65			$.35 \times V_{CCB}$	
				1.10 to 1.40			$.10 \times V_{CCB}$	
$V_{OHA}$	High-Level Output Voltage <sup>(3)</sup>	$I_{OH} = -4 \mu\text{A}$	1.10 to 3.60	1.10 to 3.60	$V_{CCA} - .4$			V
$V_{OHB}$		$I_{OH} = -4 \mu\text{A}$	1.10 to 3.60	1.10 to 3.60	$V_{CCB} - .4$			
$V_{OLA}$	Low-Level Output Voltage <sup>(3)</sup>	$I_{OL} = 4 \mu\text{A}$	1.10 to 3.60	1.10 to 3.60			.4	V
$V_{OLB}$		$I_{OL} = 4 \mu\text{A}$	1.10 to 3.60	1.10 to 3.60			.4	
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive Current	$V_{IN} = 0.8 \text{ V}$	3.00	3.00	75.0			$\mu\text{A}$
		$V_{IN} = 2.0 \text{ V}$	3.00	3.00	-75.0			
		$V_{IN} = 0.7 \text{ V}$	2.30	2.30	45.0			
		$V_{IN} = 1.6 \text{ V}$	2.30	2.30	-45.0			
		$V_{IN} = 0.57 \text{ V}$	1.65	1.65	25.0			
		$V_{IN} = 1.07 \text{ V}$	1.65	1.65	-25.0			
		$V_{IN} = 0.49 \text{ V}$	1.40	1.40	11.0			
		$V_{IN} = 0.91 \text{ V}$	1.40	1.40	-11.0			
		$V_{IN} = 0.11 \text{ V}$	1.10	1.10		4.0		
		$V_{IN} = 0.99 \text{ V}$	1.10	1.10		-4.0		

### Note:

3. This is the output voltage for static conditions. Dynamic drive specifications are given in the Dynamic Output Electrical Characteristics table.

*Continued on following page...*

**DC Electrical Characteristics** (Continued) $T_A = -40$  to  $85^\circ\text{C}$ .

Symbol	Parameter	Condition	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min.	Max.	Unit
I <sub>I(ODH)</sub>	Bus-Hold Input Overdrive High Current <sup>(4)</sup>	Data Inputs A <sub>n</sub> , B <sub>n</sub>	3.60	3.60	450.0		μA
			2.70	2.70	300.0		
			1.95	1.95	200.0		
			1.60	1.60	120.0		
			1.40	1.40	80.0		
I <sub>I(ODL)</sub>	Bus-Hold Input Overdrive Low Current <sup>(5)</sup>	Data Inputs A <sub>n</sub> , B <sub>n</sub>	3.60	3.60	-450.0		μA
			2.70	2.70	-300.0		
			1.95	1.95	-200.0		
			1.60	1.60	-120.0		
			1.40	1.40	-80.0		
I <sub>I</sub>	Input Leakage Current	Control Inputs OE, V <sub>I</sub> =V <sub>CCA</sub> or GND	1.10 to 3.60	3.60		±1.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	A <sub>n</sub> V <sub>O</sub> =0 V to 3.6 V	0	3.60		±2.0	μA
		B <sub>n</sub> V <sub>O</sub> =0 V to 3.6 V	3.60	0		±2.0	
I <sub>OZ</sub>	3-State Output Leakage	A <sub>n</sub> , B <sub>n</sub> V <sub>O</sub> =0 V or 3.6 V, OE=V <sub>IL</sub>	3.60	3.60		±5.0	μA
		A <sub>n</sub> V <sub>O</sub> =0 V or 3.6 V, OE=V <sub>CCA</sub>	3.60	0		±5.0	
		B <sub>n</sub> V <sub>O</sub> =0 V or 3.6 V, OE=3.6V	0	3.60		±5.0	
I <sub>CCA/B</sub>	Quiescent Supply Current <sup>(6, 7)</sup>	V <sub>I</sub> =V <sub>CCI</sub> or GND; I <sub>O</sub> =0, OE=V <sub>IH</sub>	1.10 to 3.60	1.10 to 3.60		10.0	μA
I <sub>CCZ</sub>		V <sub>I</sub> =V <sub>CCI</sub> or GND; I <sub>O</sub> =0, OE=GND	1.10 to 3.60	1.10 to 3.60		10.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>I</sub> =V <sub>CCB</sub> or GND; I <sub>O</sub> =0 B-to-A Direction; OE=V <sub>IH</sub>	0	1.10 to 3.60		-10.0	μA
		V <sub>I</sub> =V <sub>CCA</sub> or GND; I <sub>O</sub> =0 A-to-B Direction	1.10 to 3.60	0		10.0	
I <sub>CCB</sub>		V <sub>I</sub> =V <sub>CCA</sub> or GND; I <sub>O</sub> =0, A-to-B Direction, OE=V <sub>IH</sub>	1.10 to 3.60	0		-10.0	μA
		V <sub>I</sub> =V <sub>CCB</sub> or GND; I <sub>O</sub> =0 B-to-A Direction	0	1.10 to 3.60		10.0	

**Notes:**

4. An external drive must source at least the specified current to switch LOW-to-HIGH.
5. An external drive must source at least the specified current to switch HIGH-to-LOW.
6.  $V_{CCI}$  is the  $V_{CC}$  associated with the input side.
7. Reflects current per supply,  $V_{CCA}$  or  $V_{CCB}$ .

## Dynamic Output Electrical Characteristic

### A Port ( $A_n$ )

Output Load:  $C_L=15$  pF,  $R_L \geq M\Omega$  ( $C_{I/O}=4$  pF),  $T_A=-40$  to  $85^\circ\text{C}$

Symbol	Parameter	$V_{CCA}=3.0$ V to 3.6 V		$V_{CCA}=2.3$ V to 2.7 V		$V_{CCA}=1.65$ V to 1.95 V		$V_{CCA}=1.4$ V to 1.6 V		$V_{CCA}=1.1$ V to 1.3 V	Unit
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	
$t_{rise}$	Output Rise Time A Port <sup>(9)</sup>		3.0		3.5		4.0		5.0	7.5	ns
$t_{fall}$	Output Fall Time A Port <sup>(10)</sup>		3.0		3.5		4.0		5.0	7.5	ns
$I_{OHD}$	Dynamic Output Current High <sup>(9)</sup>	-11.4		-7.5		-4.7		-3.2		-1.7	mA
$I_{OLD}$	Dynamic Output Current Low <sup>(10)</sup>	+11.4		+7.5		+4.7		+3.2		+1.7	mA

### B Port ( $B_n$ )

Output Load:  $C_L=15$  pF,  $R_L \geq M\Omega$  ( $C_{I/O}=5$  pF),  $T_A=-40$  to  $85^\circ\text{C}$

Symbol	Parameter	$V_{CCB}=3.0$ V to 3.6 V		$V_{CCB}=2.3$ V to 2.7 V		$V_{CCB}=1.65$ V to 1.95 V		$V_{CCB}=1.4$ V to 1.6 V		$V_{CCB}=1.1$ V to 1.3 V	Unit
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	
$t_{rise}$	Output Rise Time B Port <sup>(9)</sup>		3.0		3.5		4.0		5.0	7.5	ns
$t_{fall}$	Output Fall Time B Port <sup>(10)</sup>		3.0		3.5		4.0		5.0	7.5	ns
$I_{OHD}$	Dynamic Output Current High <sup>(9)</sup>	-12.0		-7.9		-5.0		-3.4		-1.8	mA
$I_{OLD}$	Dynamic Output Current Low <sup>(10)</sup>	+12.0		+7.9		+5.0		+3.4		+1.8	mA

#### Notes:

8. Dynamic output characteristics are guaranteed, but not tested.
9. See Figure 7.
10. See Figure 8.



**AC Characteristics** **$V_{CCA} = 3.0\text{ V to }3.6\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$** 

Symbol	Parameter	$V_{CCB}=3.0\text{ V to }3.6\text{ V}$		$V_{CCB}=2.3\text{ V to }2.7\text{ V}$		$V_{CCB}=1.65\text{ V to }1.95\text{ V}$		$V_{CCB}=1.4\text{ V to }1.6\text{ V}$		$V_{CCB}=1.1\text{ V to }1.3\text{ V}$	Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.2	4.0	0.3	4.2	0.5	5.4	0.6	6.8	6.9	ns
	B to A	0.2	4.0	0.2	4.1	0.3	5.0	0.5	6.0	4.5	ns
$t_{PZL}, t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu\text{s}$
$t_{SKEW}$	A Port, B Port <sup>(11)</sup>		0.5		0.5		0.5		1.0	1.0	ns

 **$V_{CCA} = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$** 

Symbol	Parameter	$V_{CCB}=3.0\text{ V to }3.6\text{ V}$		$V_{CCB}=2.3\text{ V to }2.7\text{ V}$		$V_{CCB}=1.65\text{ V to }1.95\text{ V}$		$V_{CCB}=1.4\text{ V to }1.6\text{ V}$		$V_{CCB}=1.1\text{ V to }1.3\text{ V}$	Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.2	4.1	0.4	4.5	0.5	5.6	0.8	6.9	7.0	ns
	B to A	0.3	4.2	0.4	4.5	0.5	5.5	0.5	6.5	4.8	ns
$t_{PZL}, t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu\text{s}$
$t_{SKEW}$	A Port, B Port <sup>(11)</sup>		0.5		0.5		0.5		1.0	1.0	ns

 **$V_{CCA} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40\text{ to }85^\circ\text{C}$** 

Symbol	Parameter	$V_{CCB}=3.0\text{ V to }3.6\text{ V}$		$V_{CCB}=2.3\text{ V to }2.7\text{ V}$		$V_{CCB}=1.65\text{ V to }1.95\text{ V}$		$V_{CCB}=1.4\text{ V to }1.6\text{ V}$		$V_{CCB}=1.1\text{ V to }1.3\text{ V}$	Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	7.5	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	5.4	ns
$t_{PZL}, t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu\text{s}$
$t_{SKEW}$	A Port, B Port <sup>(11)</sup>		0.5		0.5		0.5		1.0	1.0	ns

Note:

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port ( $A_n$  or  $B_n$ ) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 10). Skew is guaranteed, but not tested.

**AC Characteristics** (Continued) $V_{CCA} = 1.4 \text{ V to } 1.6 \text{ V}$ ,  $T_A = -40 \text{ to } 85^\circ\text{C}$ 

Symbol	Parameter	$V_{CCB}=3.0 \text{ V}$ to $3.6 \text{ V}$		$V_{CCB}=2.3 \text{ V}$ to $2.7 \text{ V}$		$V_{CCB}=1.65 \text{ V}$ to $1.95 \text{ V}$		$V_{CCB}=1.4 \text{ V}$ to $1.6 \text{ V}$		$V_{CCB}=1.1 \text{ V}$ to $1.3 \text{ V}$	Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	7.9	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	6.1	ns
$t_{PZL}, t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu\text{s}$
$t_{SKEW}$	A Port, B Port <sup>(12)</sup>		1.0		1.0		1.0		1.0	1.0	ns

 $V_{CCA} = 1.1 \text{ V to } 1.3 \text{ V}$ ,  $T_A = -40 \text{ to } 85^\circ\text{C}$ 

Symbol	Parameter	$V_{CCB}=3.0 \text{ V}$ to $3.6 \text{ V}$	$V_{CCB}=2.3 \text{ V}$ to $2.7 \text{ V}$	$V_{CCB}=1.65 \text{ V}$ to $1.95 \text{ V}$	$V_{CCB}=1.4 \text{ V}$ to $1.6 \text{ V}$	$V_{CCB}=1.1 \text{ V}$ to $1.3 \text{ V}$	Unit
		Typ.	Typ.	Typ.	Typ.	Typ.	
$t_{PLH}, t_{PHL}$	A to B	4.6	4.8	5.4	6.2	9.2	ns
	B to A	6.8	7.0	7.4	7.8	9.1	ns
$t_{PZL}, t_{PZH}$	OE to A, OE to B	1.7	1.7	1.7	1.7	1.7	$\mu\text{s}$
$t_{SKEW}$	A Port, B Port <sup>(12)</sup>	1.0	1.0	1.0	1.0	1.0	ns

Note:

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port ( $A_n$  or  $B_n$ ) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 10). Skew is guaranteed, but not tested.

**Maximum Data Rate<sup>(13, 14)</sup>****T<sub>A</sub> = -40 to 85°C**

<b>V<sub>CCA</sub></b>	<b>V<sub>CCB</sub>=3.0 V to 3.6 V</b>	<b>V<sub>CCB</sub>=2.3V to 2.7V</b>	<b>V<sub>CCB</sub>=1.65V to 1.95V</b>	<b>V<sub>CCB</sub>=1.4V to 1.6V</b>	<b>V<sub>CCB</sub>=1.1V to 1.3V</b>	<b>Unit</b>
	<b>Min.</b>	<b>Min.</b>	<b>Min.</b>	<b>Min.</b>	<b>Typ.</b>	
V <sub>CCA</sub> =3.00 to 3.60 V	140	120	100	80	40	Mbps
V <sub>CCA</sub> =2.30 to 2.70 V	120	120	100	80	40	Mbps
V <sub>CCA</sub> =1.65 to 1.95 V	100	100	80	60	40	Mbps
V <sub>CCA</sub> =1.40 to 1.60 V	80	80	60	60	40	Mbps
V <sub>CCA</sub> =1.10 to 1.30 V	<b>Typ.</b>	<b>Typ.</b>	<b>Typ.</b>	<b>Typ.</b>	<b>Typ.</b>	
	40	40	40	40	40	Mbps

**Notes:**

13. Maximum data rate is guaranteed, but not tested.

14. Maximum data rate is specified in megabits per second (see Figure 9). It is equivalent to two times the F-toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50MHz.

**Capacitance**

<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>	<b>T<sub>A</sub>=+25°C Typical</b>	<b>Unit</b>
C <sub>IN</sub>	Input Capacitance Control Pin (OE)	V <sub>CCA</sub> =V <sub>CCB</sub> =GND	3	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CCA</sub> =V <sub>CCB</sub> =3.3 V, OE=GND	4	pF
			5	
C <sub>pd</sub>	Power Dissipation Capacitance	V <sub>CCA</sub> =V <sub>CCB</sub> =3.3 V, V <sub>I</sub> =0V or V <sub>CC</sub> , f=10 MHz	25	pF

## I/O Architecture Benefit

The FXLA0104 I/O architecture benefits the end user, beyond level translation, in the following three ways:

**Auto Direction** without an external direction pin.

**Drive Capacitive Loads.** Automatically shifts to a higher current drive mode only during “Dynamic Mode” or HL / LH transitions.

**Lower Power Consumption.** Automatically shifts to low-power mode during “Static Mode” (no transitions), lowering power consumption.

The FXLA0104 does not require a direction pin. Instead, the I/O architecture detects input transitions on both side and automatically transfers the data to the corresponding output. For example, for a given channel, if both A and B side are at a static LOW, the direction has been established as  $A \rightarrow B$ , and a LH transition occurs on the B port; the FXLA0104 internal I/O architecture automatically changes direction from  $A \rightarrow B$  to  $B \rightarrow A$ .

During HL / LH transitions, or “Dynamic Mode,” a strong output driver drives the output channel in parallel with a weak output driver. After a typical delay of approximately 10 ns – 50 ns, the strong driver is turned off, leaving the weak driver enabled for holding the logic state of the channel. This weak driver is called the “bus

hold.” “Static Mode” is when only the bus hold drives the channel. The bus hold can be over ridden in the event of a direction change. The strong driver allows the FXLA0104 to quickly charge and discharge capacitive transmission lines during dynamic mode. Static mode conserves power, where  $I_{CC}$  is typically  $< 5 \mu A$ .

### Bus Hold Minimum Drive Current

Specifies the minimum amount of current the bus hold driver can source/sink. The bus hold minimum drive current ( $I_{HOLD}$ ) is  $V_{CC}$  dependent and guaranteed in the DC Electrical tables. The intent is to maintain a valid output state in a static mode, but that can be overridden when an input data transition occurs.

### Bus Hold Input Overdrive Drive Current

Specifies the minimum amount of current required (by an external device) to overdrive the bus hold in the event of a direction change. The bus hold overdrive ( $I_{ODH}$ ,  $I_{OLD}$ ) is  $V_{CC}$  dependent and guaranteed in the DC Electrical tables.

### Dynamic Output Current

The strength of the output driver during LH / HL transitions is *referenced on page 8, Dynamic Output Electrical Characteristics,  $I_{OHD}$ , and  $I_{OLD}$ .*

# Test Diagrams

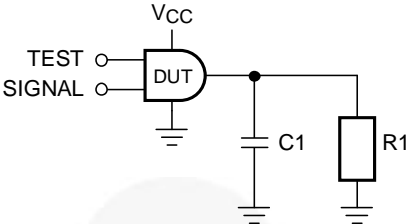


Figure 3. Test Circuit

Table 1. AC Test Conditions

Test	Input Signal	Output Enable Control
$t_{PLH}$ , $t_{PHL}$	Data Pulses	VCCA
$t_{PZL}$	0V	LOW to HIGH Switch
$t_{PZH}$	VCCI	LOW to HIGH Switch

Table 2. AC Load

V <sub>CCO</sub>	C1	R1
1.2 V ± 0.1 V	15 pF	1 MΩ
1.5 V ± 0.1 V	15 pF	1 MΩ
1.8 V ± 0.15 V	15 pF	1 MΩ
2.5 V ± 0.2 V	15 pF	1 MΩ
3.3 V ± 0.3 V	15 pF	1 MΩ

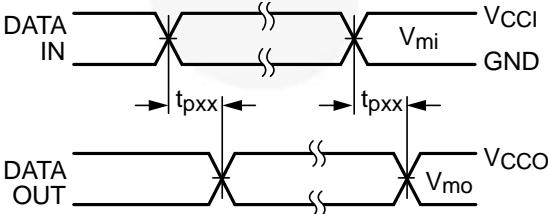


Figure 4. Waveform for Inverting and Non-Inverting Functions

## Notes:

15. Input  $t_R = t_F = 2.0$  ns, 10% to 90%.
16. Input  $t_R = t_F = 2.5$  ns, 10% to 90%, at  $V_I = 3.0$  V to 3.6 V only.

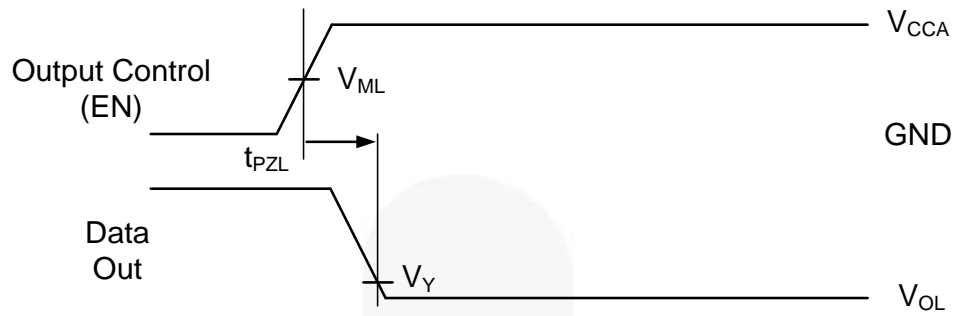


Figure 5. 3-State Output Low Enable

**Notes:**

- 17. Input  $t_R = t_F = 2.0$  ns, 10% to 90%.
- 18. Input  $t_R = t_F = 2.5$  ns, 10% to 90%, at  $V_I = 3.0$  V to 3.6 V only.

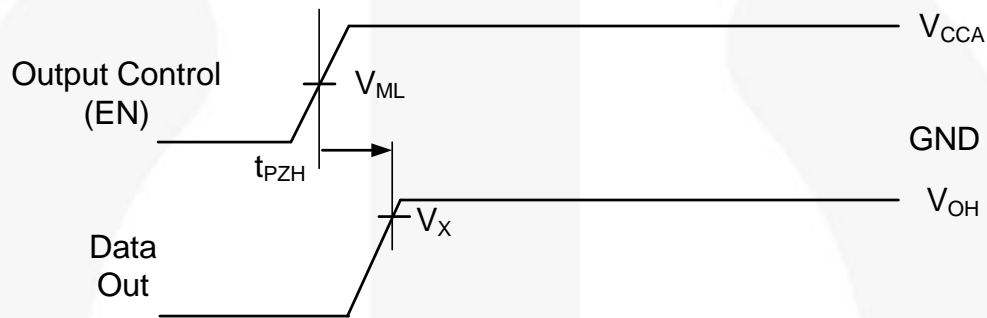


Figure 6. 3-State Output High Enable

**Notes:**

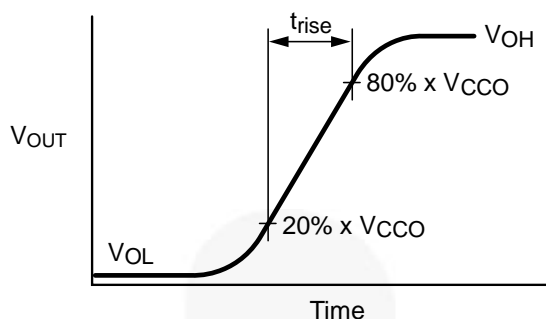
- 19. Input  $t_R = t_F = 2.0$  ns, 10% to 90%.
- 20. Input  $t_R = t_F = 2.5$  ns, 10% to 90%, at  $V_I = 3.0$  V to 3.6 V only.

Table 3. Test Measure Points

Symbol	$V_{DD}$
$V_{MI}^{(21)}$	$V_{CCI} / 2$
$V_{MO}$	$V_{CCO} / 2$
$V_X$	$0.9 \times V_{CCO}$
$V_Y$	$0.1 \times V_{CCO}$

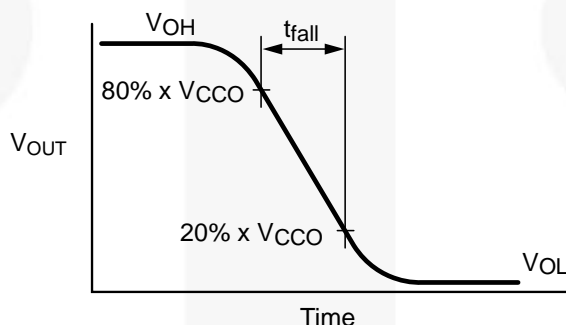
**Note:**

- 21.  $V_{CCI} = V_{CCA}$  for control pin OE or  $V_{MI}(V_{CCA}/2)$ .



$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \cdot V_{CC0}}{t_{RISE}}$$

Figure 7. Active Output Rise Time and Dynamic Output Current High



$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \cdot V_{CC0}}{t_{FALL}}$$

Figure 8. Active Output Fall Time and Dynamic Output Current Low

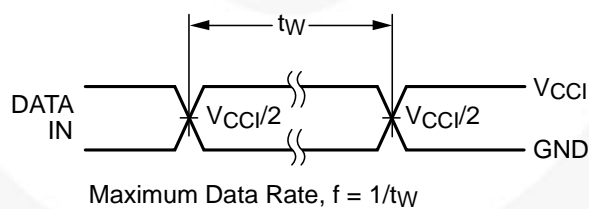


Figure 9. Maximum Data Rate

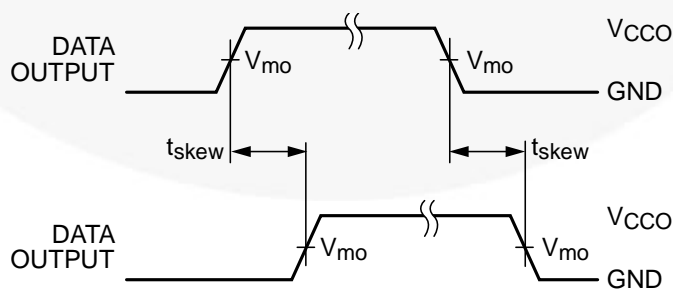
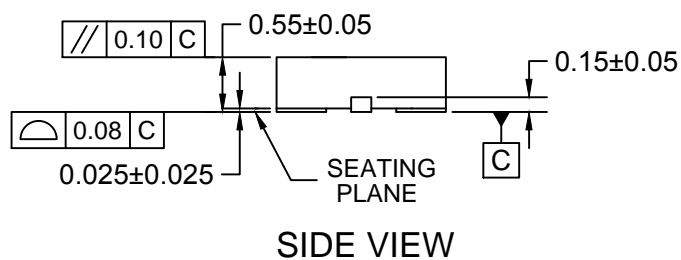
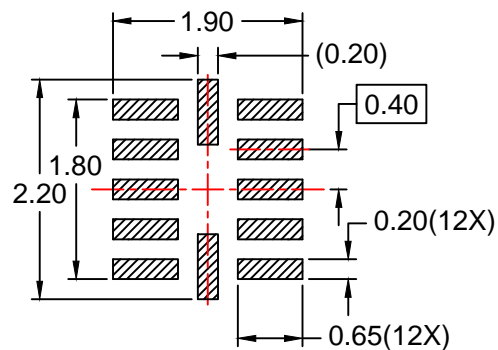
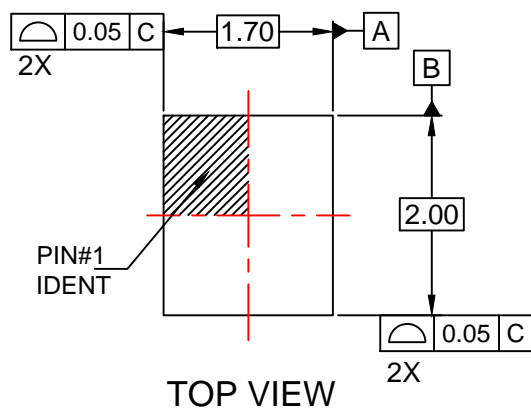


Figure 10. Output Skew Time

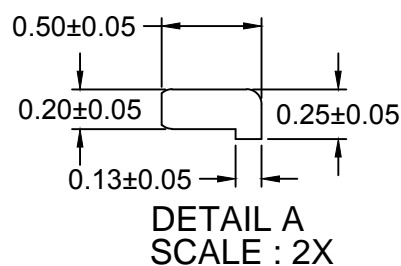
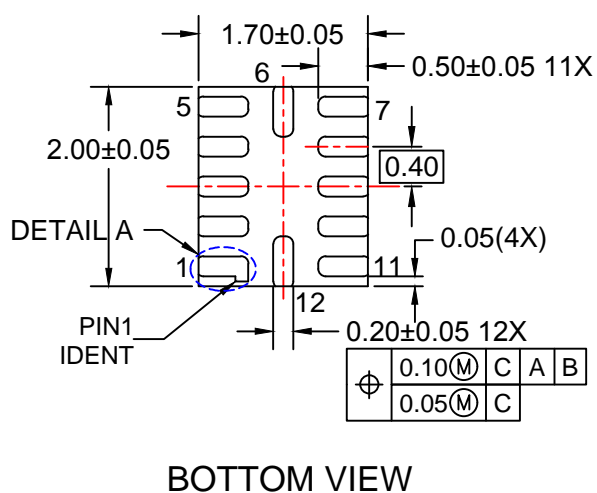
**Note:**

22.  $t_{SKEW} = (t_{pHLmax} - t_{pHLmin})$  OR  $(t_{pLHmax} - t_{pLHmin})$



#### NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-220 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-UMLP12Crev3.












## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™	F-PFS™		
Awinda®	FRFET®		
AX-CAP®*	Global Power Resource™	PowerTrench®	TinyBoost®
BitSiC™	GreenBridge™	PowerXS™	TinyBuck®
Build it Now™	Green FPS™	Programmable Active Droop™	TinyCalc™
CorePLUS™	Green FPS™ e-Series™	QFET®	TinyLogic®
CorePOWER™	Gmax™	QS™	TINYOPTO™
CROSSVOL™	GTO™	Quiet Series™	TinyPower™
CTL™	IntelliMAX™	RapidConfigure™	TinyPWM™
Current Transfer Logic™	ISOPLANAR™		TinyWire™
DEUXPEED®	Making Small Speakers Sound Louder and Better™	Saving our world, 1mW/W/kW at a time™	TranSiC™
Dual Cool™	MegaBuck™	SignalWise™	TriFault Detect™
EcoSPARK®	MICROCOUPLER™	SmartMax™	TRUECURRENT®*
EfficientMax™	MicroFET™	SMART START™	μSerDes™
ESBC™	MicroPak™	Solutions for Your Success™	
	MicroPak2™	SPM®	UHC®
Fairchild®	MillerDrive™	STEALTH™	Ultra FRFET™
Fairchild Semiconductor®	MotionMax™	SuperFET®	UniFET™
FACT Quiet Series™	MotionGrid®	SuperSOT™-3	VCX™
FACT®	MTi®	SuperSOT™-6	VisualMax™
FAST®	MTx®	SuperSOT™-8	VoltagePlus™
FastvCore™	MVN®	SupreMOS®	XS™
FETBench™	mWSaver®	SyncFET™	Xsens™
FPS™	OptoHiT™	Sync-Lock™	仙童™

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I71

# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit [www.ameya360.com](http://www.ameya360.com)

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct    +86 (21) 6401-6692  
Email     amall@ameya360.com  
QQ        800077892  
Skype     ameyasales1 ameyasales2

➤ Customer Service :

Email     service@ameya360.com

➤ Partnership :

Tel        +86 (21) 64016692-8333  
Email     mkt@ameya360.com