

N-Channel UltraFET Power MOSFET **55 V, 35 A, 34 mΩ**

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75321.

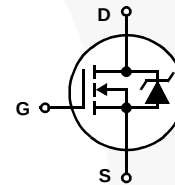
Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75321P3	TO-220AB	75321P

Features

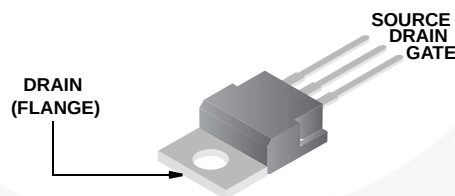
- 35A, 55V
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Models
 - Thermal Impedance SPICE and SABER Models Available on the WEB at: www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF75321P3

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55 V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	55 V
Gate to Source Voltage	V_{GS}	± 20 V
Drain Current		
Continuous (Figure 2)	I_D	35 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15
Power Dissipation	P_D	93 W
Derate Above 25°C		0.625 $\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175 $^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 50V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 45V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 35A, V _{GS} = 10V (Figure 9)	-	0.028	0.034	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	1.6	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220	-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D ≅ 35A, R _L = 0.86Ω, V _{GS} = 10V, R _{GS} = 25Ω	-	-	100	ns	
Turn-On Delay Time	t _{d(ON)}		-	11	-	ns	
Rise Time	t _r		-	55	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	47	-	ns	
Fall Time	t _f		-	66	-	ns	
Turn-Off Time	t _{OFF}		-	-	170	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 30V, I _D ≅ 35A, R _L = 0.86Ω I _{g(REF)} = 1.0mA (Figure 13)	-	36	44	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	21	26	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	1.3	1.6	nC
Gate to Source Gate Charge	Q _{gs}			-	3	-	nC
Reverse Transfer Capacitance	Q _{gd}			-	9	-	nC

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Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12)	-	680	-	pF
Output Capacitance	C_{OSS}		-	270	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	60	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 35\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 35\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	59	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 35\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	82	nC

Typical Performance Curves

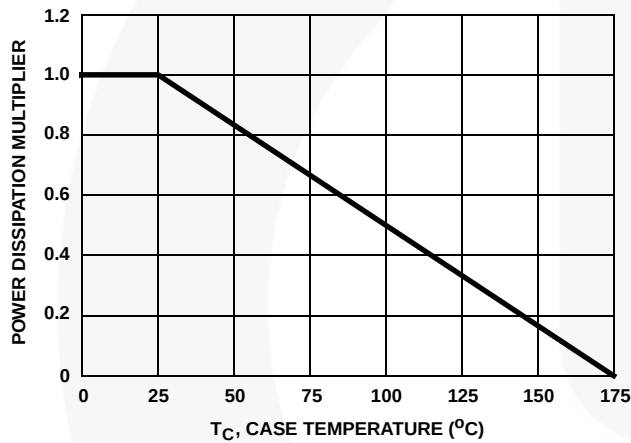


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

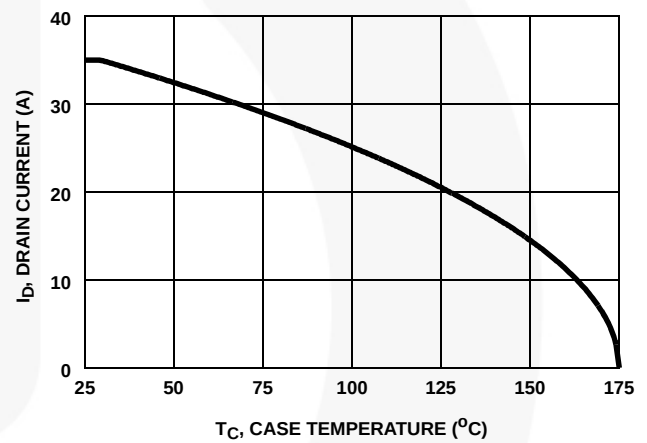


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

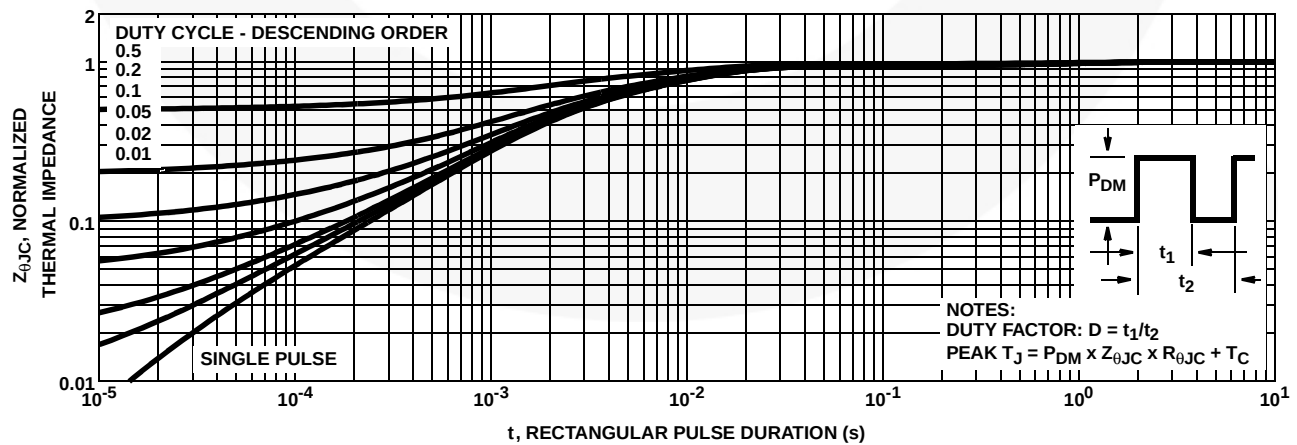


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

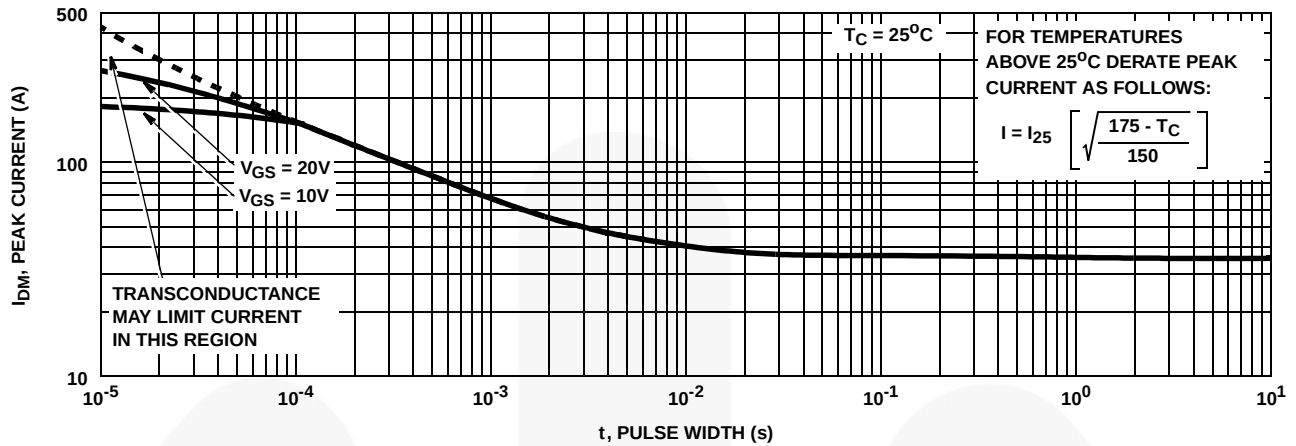


FIGURE 4. PEAK CURRENT CAPABILITY

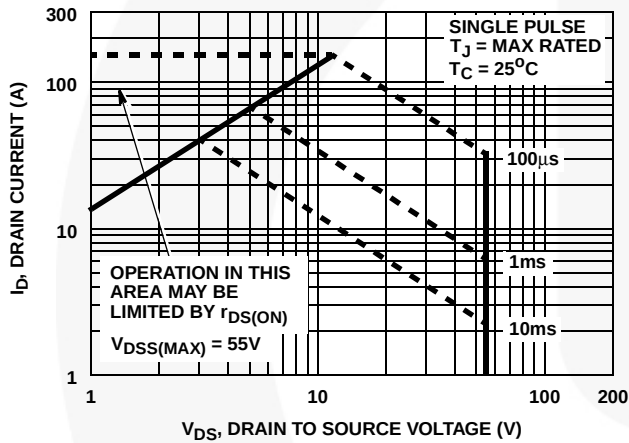
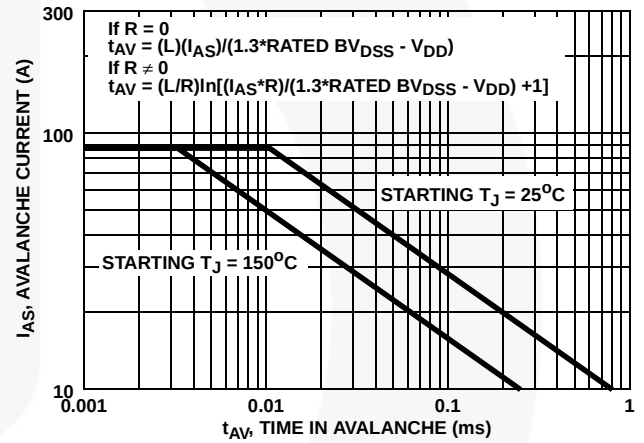


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

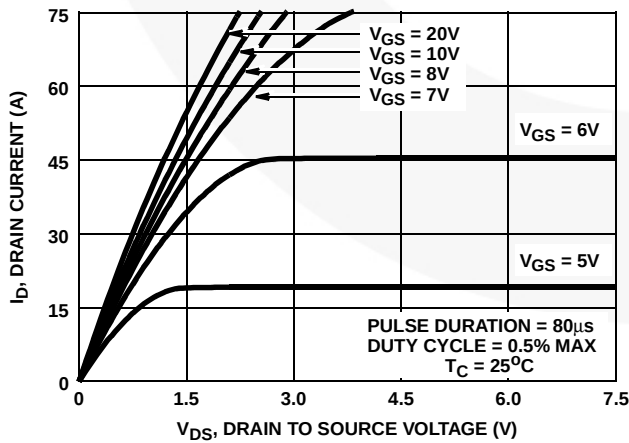


FIGURE 7. SATURATION CHARACTERISTICS

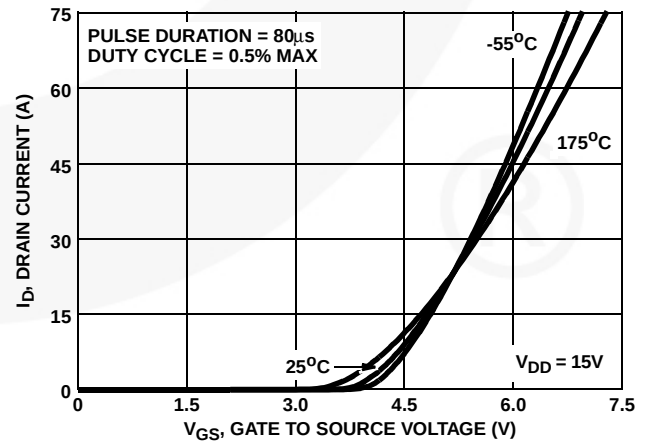


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

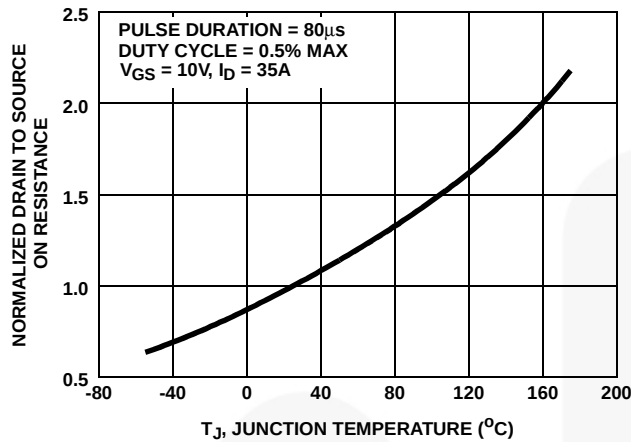


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

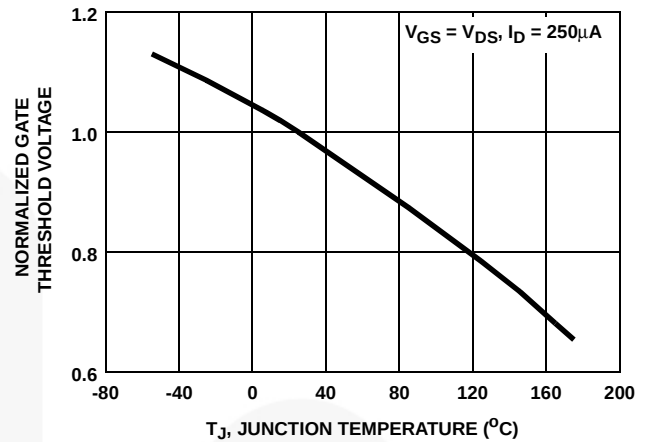


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

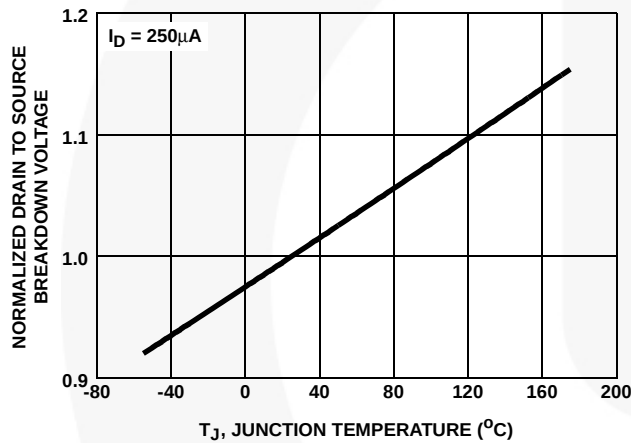


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

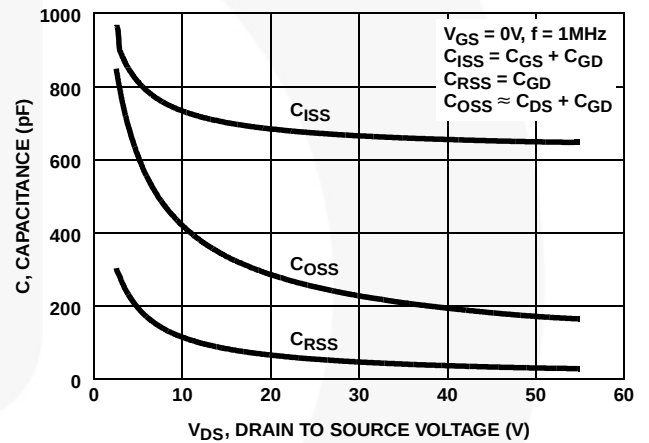
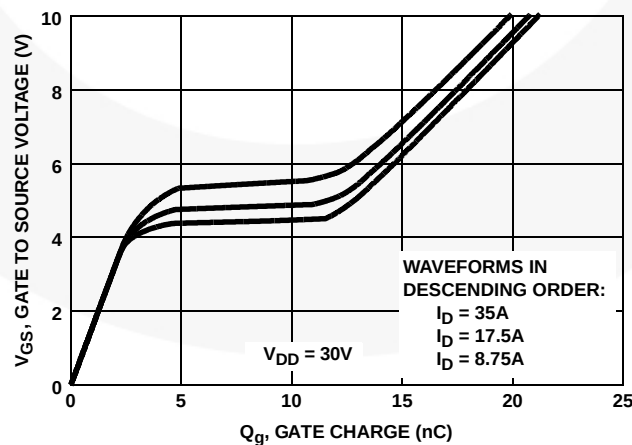


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

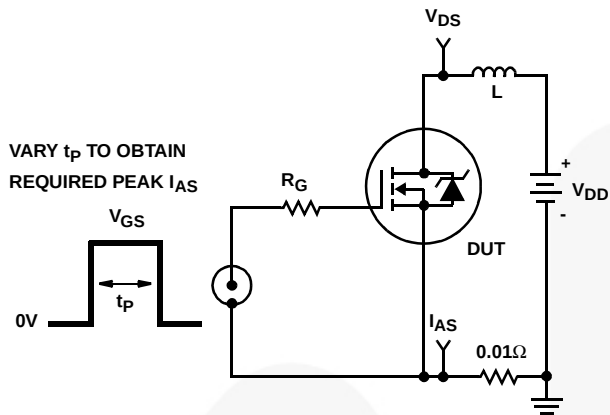


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

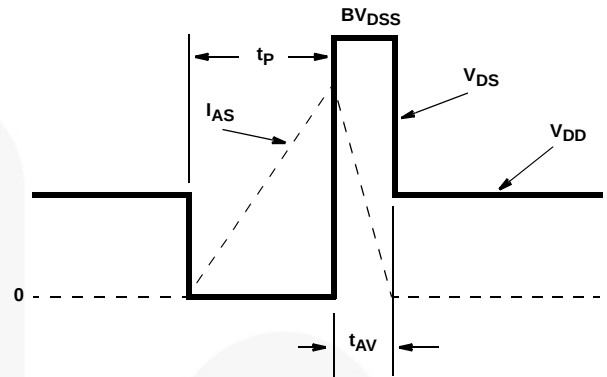


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

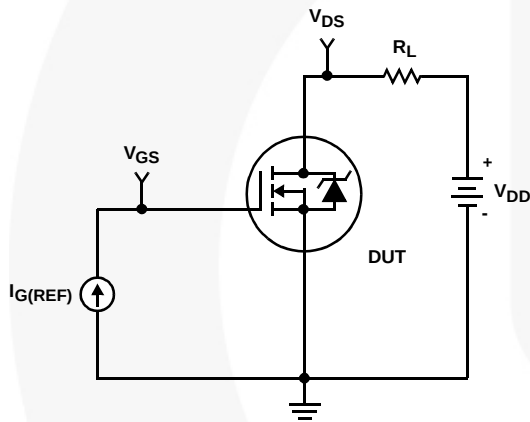


FIGURE 16. GATE CHARGE TEST CIRCUIT

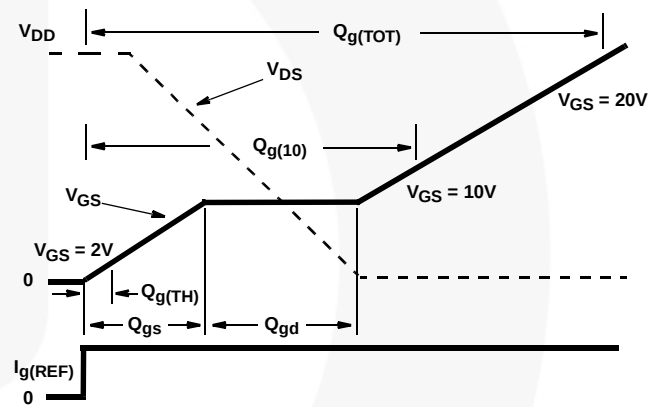


FIGURE 17. GATE CHARGE WAVEFORM

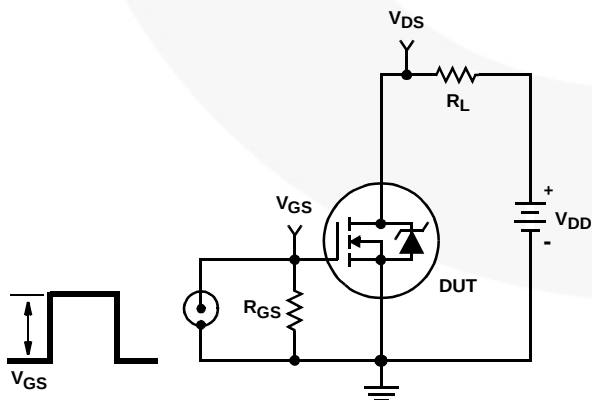


FIGURE 18. SWITCHING TIME TEST CIRCUIT

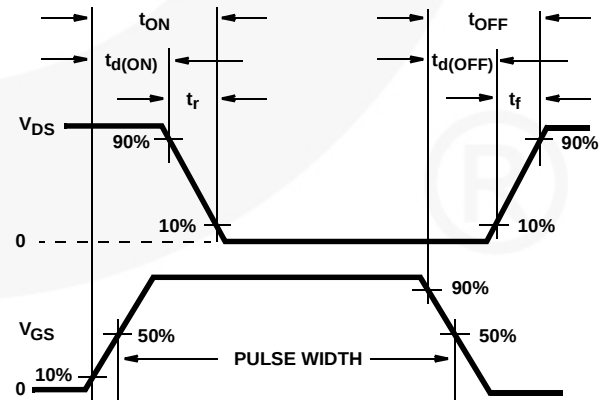


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

SPICE Thermal Model

REV 24 February 1999

HUF75321P

CTHERM1 th 6 2.7e-3
 CTHERM2 6 5 3.7e-3
 CTHERM3 5 4 1.2e-2
 CTHERM4 4 3 3.8e-3
 CTHERM5 3 2 1.4e-2
 CTHERM6 2 tl 10.55

R THERM1 th 6 1.10e-2
 R THERM2 6 5 2.72e-2
 R THERM3 5 4 7.67e-2
 R THERM4 4 3 4.30e-1
 R THERM5 3 2 6.49e-1
 R THERM6 2 tl 8.61e-2

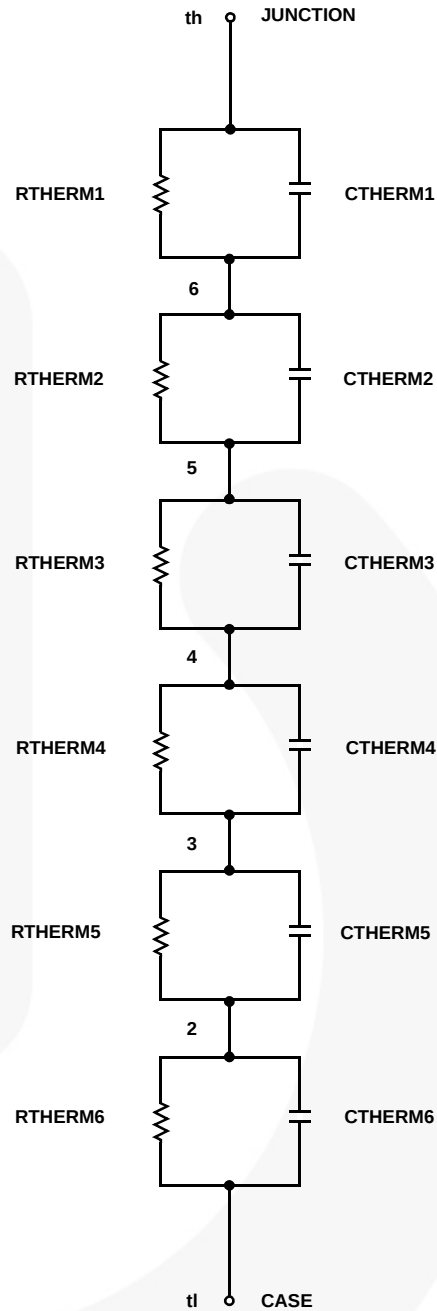
SABER Thermal Model

SABER thermal model HUF75321P

```
template thermal_model th tl
thermal_c th, tl
```

```
{
  ctherm.ctherm1 th 6 = 2.7e-3
  ctherm.ctherm2 6 5 = 3.7e-3
  ctherm.ctherm3 5 4 = 1.2e-2
  ctherm.ctherm4 4 3 = 3.8e-3
  ctherm.ctherm5 3 2 = 1.4e-2
  ctherm.ctherm6 2 tl = 10.55
```

```
  rtherm.rtherm1 th 6 = 1.10e-2
  rtherm.rtherm2 6 5 = 2.72e-2
  rtherm.rtherm3 5 4 = 7.67e-2
  rtherm.rtherm4 4 3 = 4.30e-1
  rtherm.rtherm5 3 2 = 6.49e-1
  rtherm.rtherm6 2 tl = 8.61e-2
}
```





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Website :

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Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com