13 Channel ESD Protection Solution with Current-Limit Load Switch for HDMI Port

Check for Samples: TPD13S523

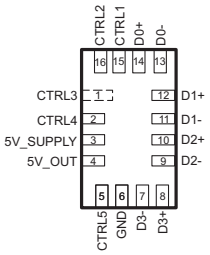
FEATURES

- **Single Chip ESD Solution for HDMI 1.4 and HDMI 1.3 Interface**
- **On-chip 5V Load Switch with Current Limit and Reverse Current Protection**
- **Supports UTILITY Line Protection for HDMI 1.4 Audio Return Line**
- **<0.05-pF Differential Capacitance Between the TMDS Signal Pair**
- **Industry Standard 16-TSSOP and Space Saving 16-RSV Package**
- **Supports Data Rates in Excess of 3.3Gbps**
- **R_{DYN} 0.5Ω**
- **IEC 61000-4-2 (Level 4) ESD Compliance**
- **Commercial Temperature Range: –40°C to 85°C**

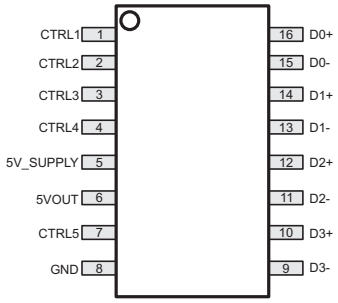
APPLICATIONS

- **Set-top Box**
- **Smart Phone**
- **Digital Camcorder**
- **Portable Game Console**

16-RSV: 2.6mm x 1.8mm (TOP VIEW)



16-TSSOP: 6.4mm x 5.0mm (TOP VIEW)



All the CTRLx pins have the same ESD circuit and are interchangeable.

DESCRIPTION

The TPD13S523 is a single-chip integrated ESD protection solution for HDMI 1.4 or HDMI 1.3 interface. This device offers 13 channels of ESD clamp circuits with flow-through pin mapping that matches HDMI connector high-speed lines. While providing ESD protection, the TPD13S523 adds little to no additional distortion to the high-speed differential signals. The monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line (<0.05pF differential matching between TMDS lines). This is a advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality.

The TPD13S523 incorporates an on-chip current limited load switch that is compliant with HDMI 5V out electrical specifications. The short circuit protection at 5V_OUT ensures that the device is not damaged in case there is accidental short to GND. The load switch also incorporates reverse current blocking feature which ensures that the HDMI driver side is not erroneously turned on when two HDMI drivers are connected together.

Connecting a 0.1µF to 1µF capacitor at 5V_OUT, TPD13S523 protects the system against ±12kV contact and ±14kV air-gap ESD discharge.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	3000	Tape and reel	TPD13S523PWR	RA523
	3000	Tape and reel	TPD13S523RSVR	ZTT

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CIRCUIT BLOCK DIAGRAMS

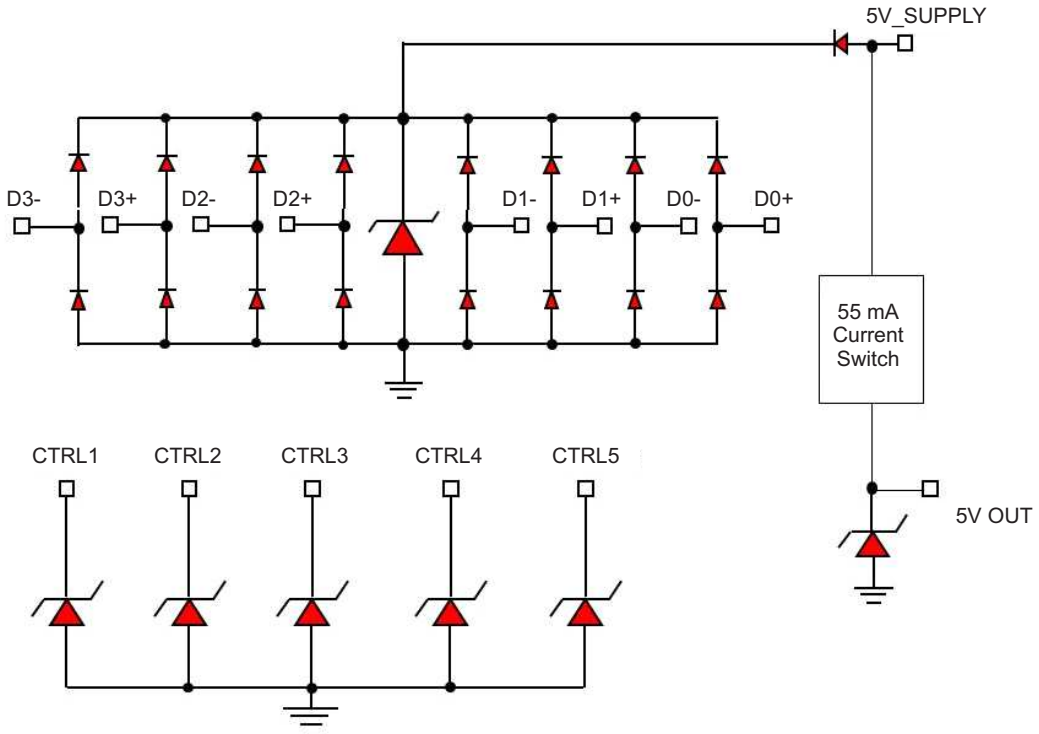


Figure 1. Electrical Equivalent Circuit Diagrams

ESD TERMINAL DESCRIPTIONS

SIGNAL	TSSOP PIN NO.	RSV PIN NO.	TYPE	DESCRIPTION
Dx+, Dx-	9, 10, 11, 12, 13, 14, 15, 16	7, 8, 9, 10, 11, 12, 13, 14	connector pins(1)	High-speed ESD Clamp: provides ESD protection for TMDS lines.
CTRLx	1, 2, 3, 4, 7	1, 2, 5, 15, 16	connector pins(1)	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.

(1) Connector pins are Dx+, Dx–, CTRLx, and 5V_OUT

SUPPLY TERMINAL DESCRIPTIONS

SIGNAL	TSSOP PIN NO.	RSV PIN NO.	TYPE	DESCRIPTION
5V_SUPPLY	5	3	Supply pin	**Supply Pin for HDMI 5V_OUT** 5.0 Volts, connects to internal VCC plane on the PCB board; connect a 0.1 to 1µF capacitor shunt to ground.
5V_OUT	6	4	HDMI 5VOUT pin	**Current Limited HDMI 5V_OUT:** connect to HDMI 5V_OUT; offers IEC61000-4-2 ESD protection; connect a 0.1 to 1µF capacitor shunt to ground.

LAYOUT SCHEME USING TPD13S523

The TPD13S523 device offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. In the event of an ESD stress, this device ensures that the core circuitry is protected and the system is functioning properly. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD13S523 as close to the connector as possible. This allows the TPD13S523 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place two 0.1-µF capacitors very close to the 5V_SUPPLY and 5VOUT pins. These capacitors will help limit the noise at the 5VOUT power line, and also help with system level ESD protection.
3. Ensure that there is enough metallization for the GND pad. During normal operation, the TPD13S523 ESD pins consume ultra low leakage current. During the ESD event, GND pin will see multiple amps current. Sufficient current paths enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. If there is no UTILITY pin protection required, it is recommended to leave CTRL5 open (Figure 2). Connect the CEC, SCL, SDA, and HPD lines to CTRL1-CTRL4 pins.
5. The critical routing paths for HMDI interface are the high-speed TMDS lines. With the PW package, all the TMDS lines (pin Dxx) can be routed in a single signal plane and still maintain the differential coupling & trace symmetry. This helps reduce the overall board manufacturing cost. The slow speed control lines can be routed in another signal layer through VIAs.

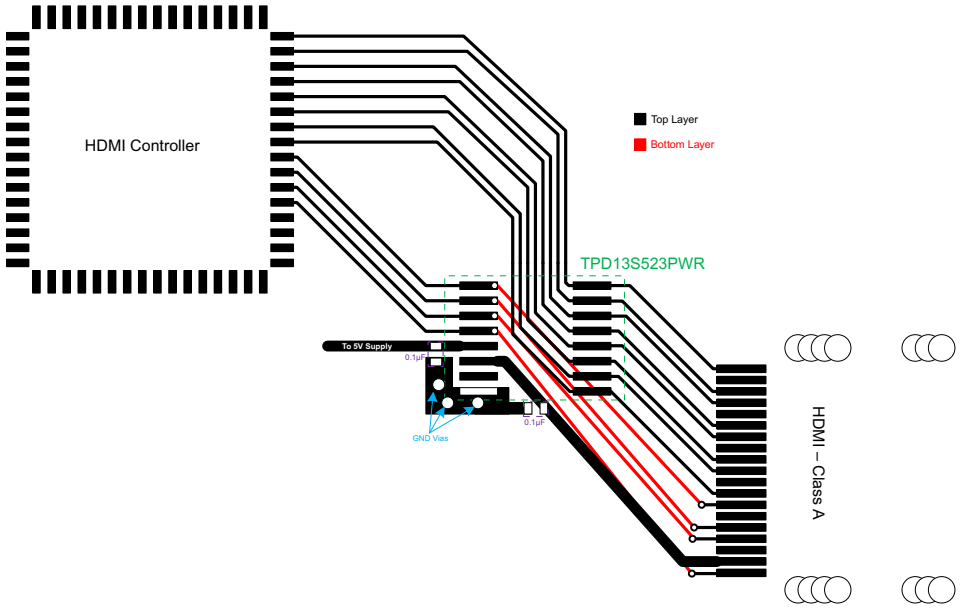


Figure 2. TPD13S523PWR Layout Example 12-Line HDMI Protection (Leave CTRL5 Open)

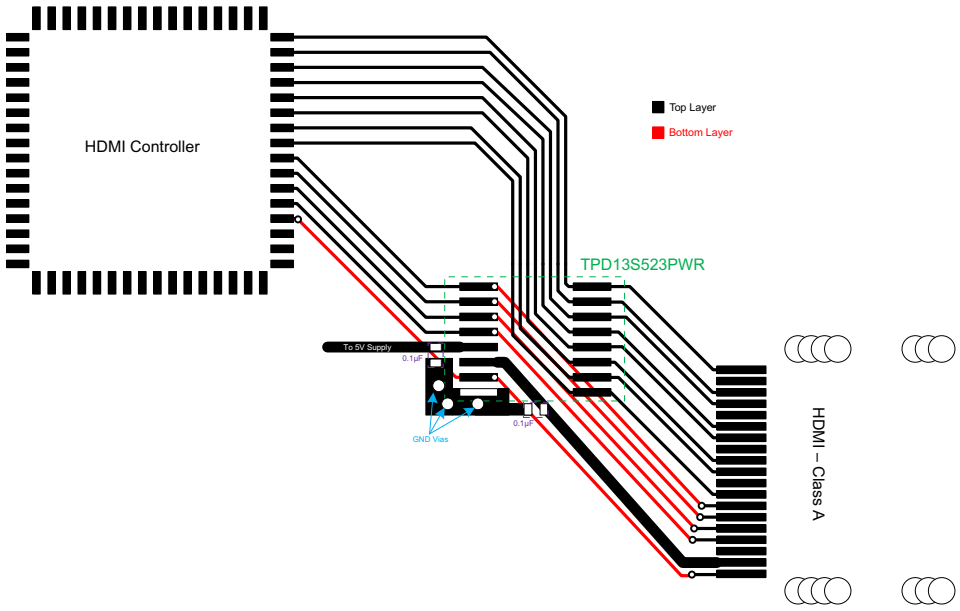


Figure 3. TPD13S523PWR Layout Example 13-Line HDMI Protection (Additional UTILITY Line Protection)

ABSOLUTE MAXIMUM RATINGS

T_A = –40°C to 85°C

DESCRIPTION		MIN	MAX	UNIT
V_{CC} Voltage Tolerance	5V_SUPPLY	–0.3	6	V
IO Voltage Tolerance	Connector Pins(1)	–0.3	6	V
Storage Temperature		–65	125	°C
IEC 61000-4-2 Contact Discharge	Connector Pins(1)		±12	kV
IEC 61000-4-2 Air-gap Discharge	Connector Pins(1)		±14	kV
IEC 61000-4-5 Peak current (8/20 µs)	Connector Pins(1)		3	A
IEC 61000-4-5 Peak Power (8/20 µs)	Connector Pins(1)		30	W

(1) Connector pins are Dx+, Dx–, CTRLx, and 5V_OUT

THERMAL INFORMATION

THERMAL METRIC(1)		TPD13S523PW TSSOP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	119.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	54.5	
θ_{JB}	Junction-to-board thermal resistance	65.0	
ψ_{JT}	Junction-to-top characterization parameter	9.7	
ψ_{JB}	Junction-to-board characterization parameter	n/a	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

T_A = –40°C to 85°C

DESCRIPTION		MIN	MAX	UNIT
VCC Voltage	5V_SUPPLY		5.5	V
IO voltage at external signal pins	Signal Pins(1)	–0.3	5.5	V
Operating free-air temperature range		–40	85	°C

(1) External Signal pins are Dx+, Dx–, CTRLx, and 5V_OUT

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
LOAD SWITCH						
I_{CC}	Supply current at 5V_SUPPLY	5V_SUPPLY =5V, 5V OUT = Open	6.5	7	10	µA
I_{SC}	Short circuit current at 5V_OUT	5V_SUPPLY =5V, 5V_OUT = GND	100	116	147	mA
$I_{BACKDRIVE}$	Reverse leakage current at 5VOUT	5V_SUPPLY =0V, 5V_OUT = 5V		0.01	0.69	µA
V_{DROP}	5V_OUT output voltage drop	5V_SUPPLY =5V, I_{5V_OUT} = 55 mA		170	205	mV
CONNECTOR PINS						
V_{RWM}	Reverse stand-off voltage				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	Ipp = 1A, 8/20 µs(1)			13	V
		Ipp = 3A, 8/20 µs(1)			15	
I_{IO}	Leakage current through external signal pins(2)	5V_SUPPLY =5V, V_{IO} = 5 V	2	7	65	nA
I_{OFF}	Current from IO Port to supply pins when powered down through signal pins(3)	5V_SUPPLY = 0 V, V_{IO} = 2.5 V	1	5	44	nA
V_D	Diode forward voltage through external signal pins(2); lower clamp diode	I_D = 8 mA	0.7	0.85	0.95	V
R_{DYN}	Dynamic resistance of ESD clamps external pins(3)	Pin to ground(2)		0.5		Ω
C_{IO_TMDS}	IO capacitance Dx+, Dx– pins to GND	5V_SUPPLY = 5 V, V_{IO} = 2.5 V		1		pF
ΔC_{IO_TMDS}	Differential capacitance for the Dx+, Dx– lines	5V_SUPPLY = 5 V, V_{IO} = 2.5 V		0.05		pF
$C_{IO\_CONTROL}$	CTRLx pin capacitance	5V_SUPPLY = 5 V, V_{IO} = 2.5 V		1		pF
V_{BR}	Break-down voltage through signal pins(3)	I_{IO} = 1 mA	6			V

(1) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC61000-4-5
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I=1A AND I=10A
(3) Signal pins are Dx+, Dx–, and CTRLx

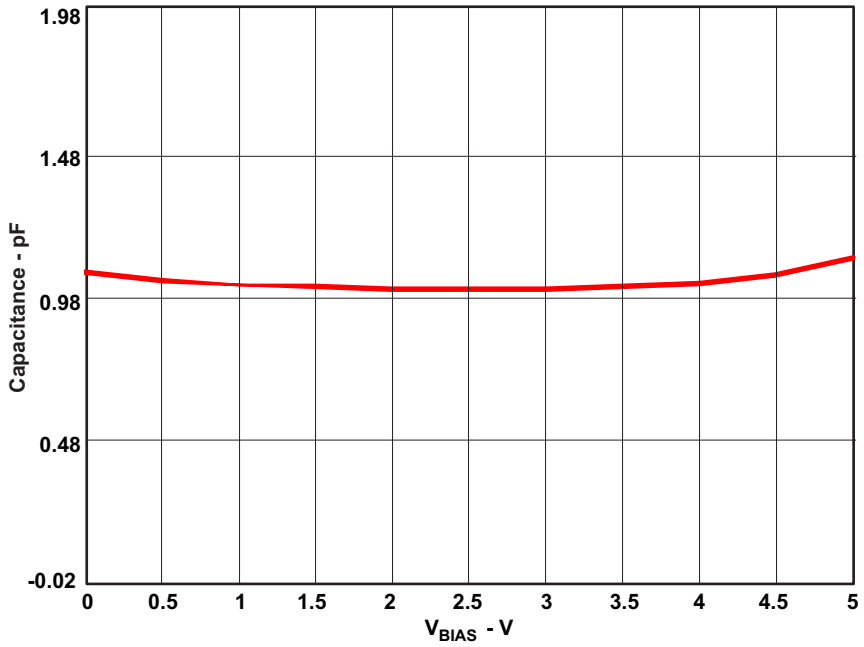


Figure 4. Pin Capacitance

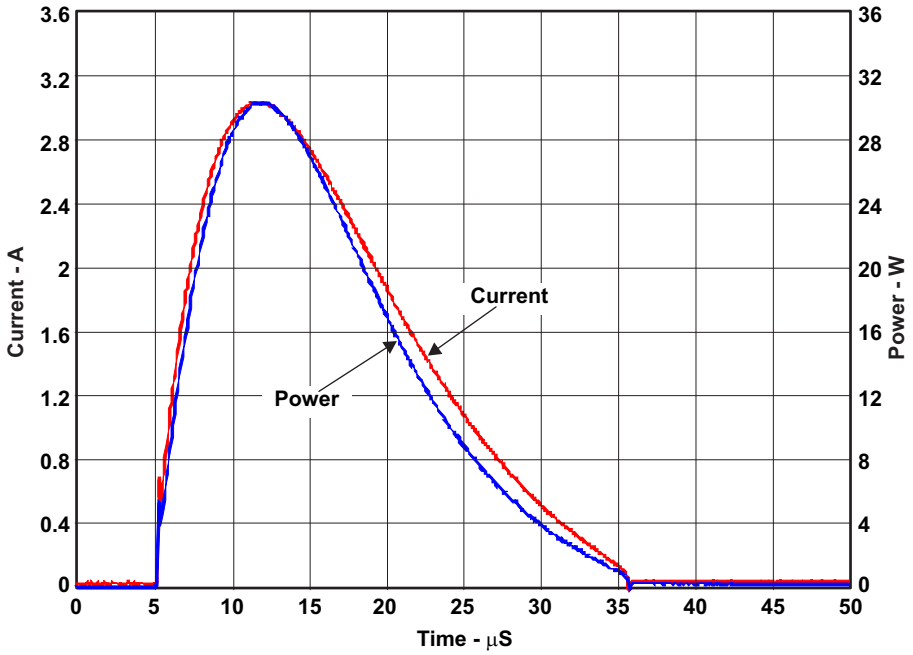


Figure 5. IEC61000-4-5 (Surge) I_{PP} and P_{PP} Waveform

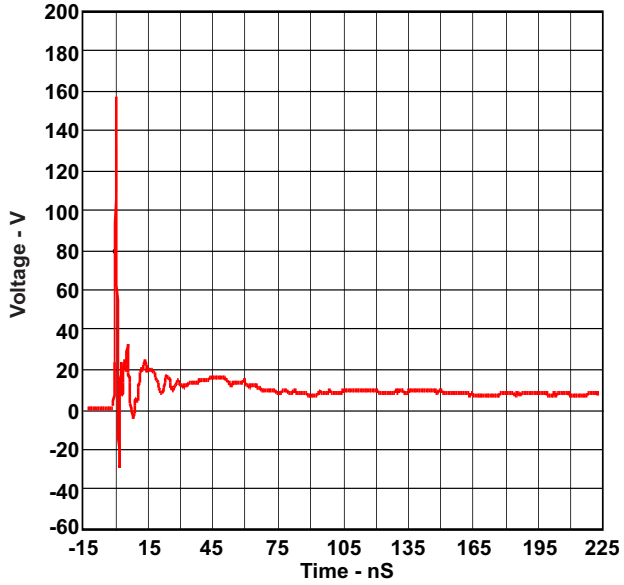


Figure 6. IEC Positive Clamping Waveform using +8kV Contact

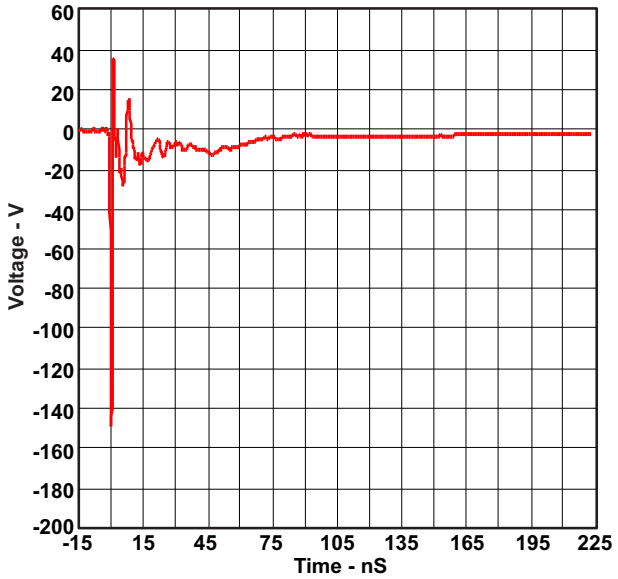


Figure 7. IEC Negative Clamping Waveform using -8kV Contact

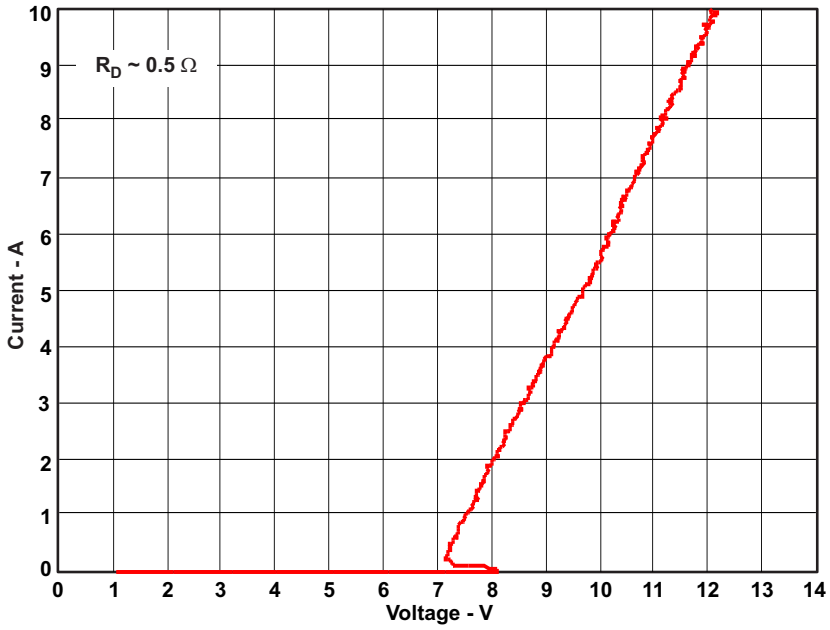


Figure 8. TLP Plot on Connector Pins

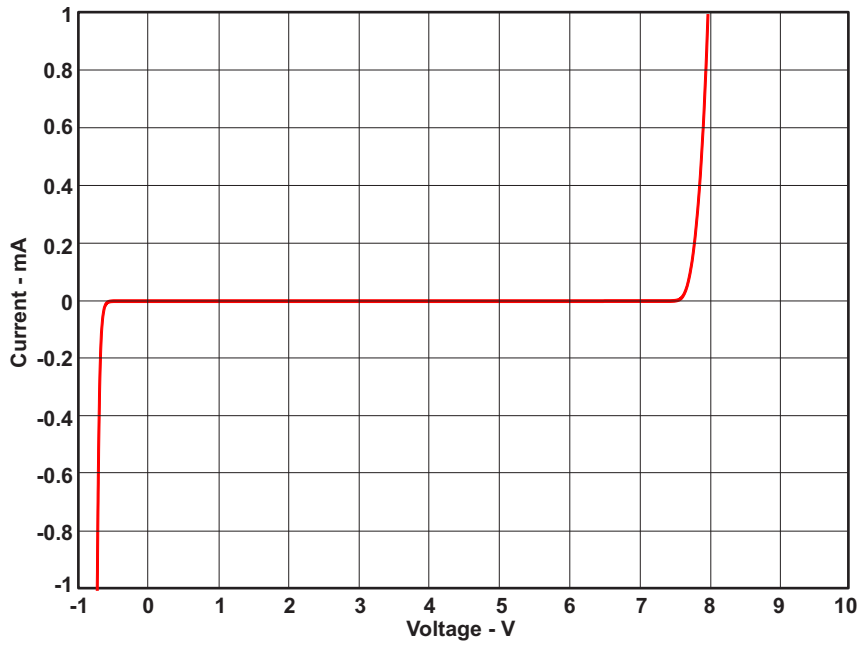


Figure 9. IV Curve on Signal Pins

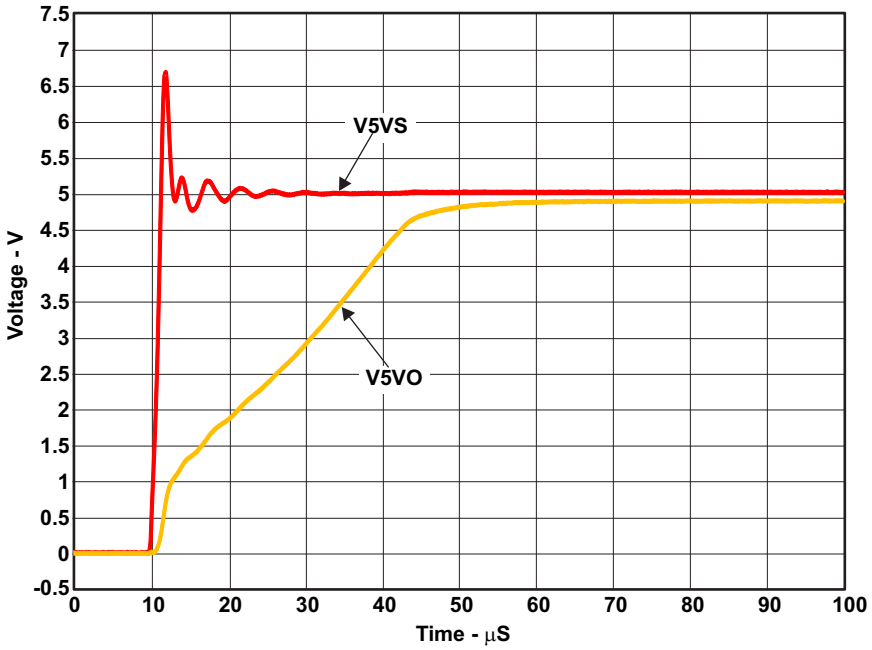


Figure 10. Load Switch Start-up Transient Waveform. Cin=1µF, Cout=1µF, I_{SWITCH}=55mA, T_A=25°C

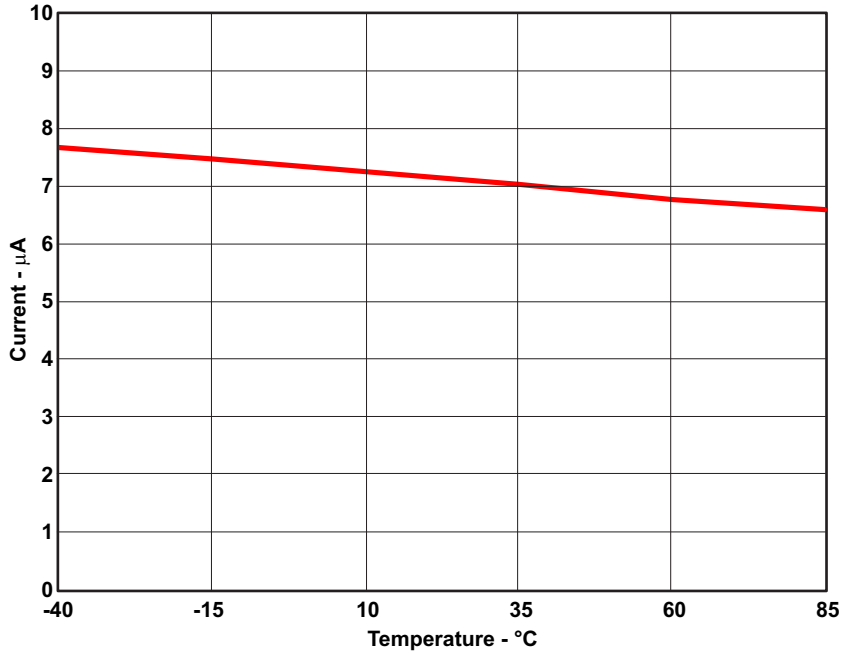


Figure 11. Load Switch Supply Current; 5V_SUPPLY=5V, 5VOUT=open

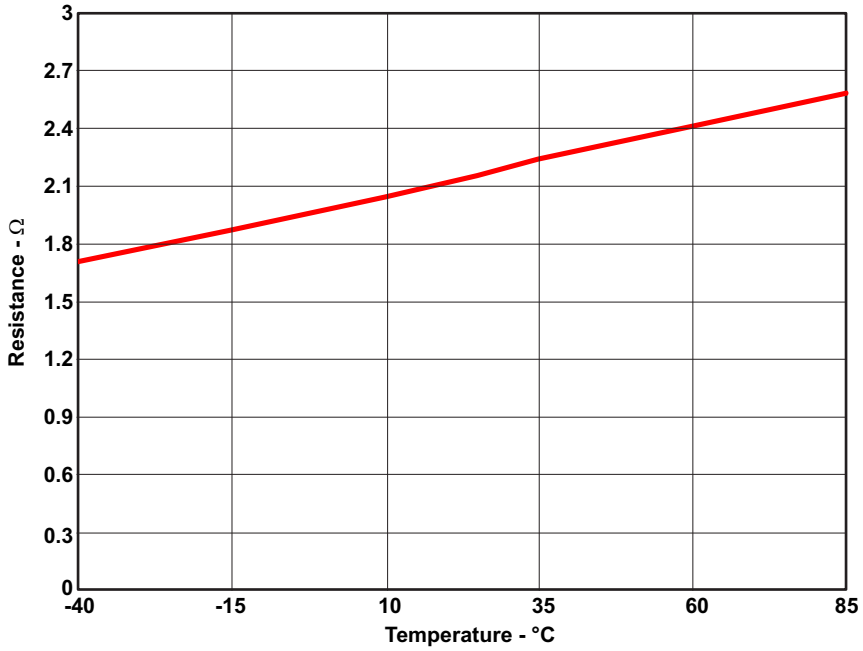


Figure 12. Load Switch Resistance vs. Temperature

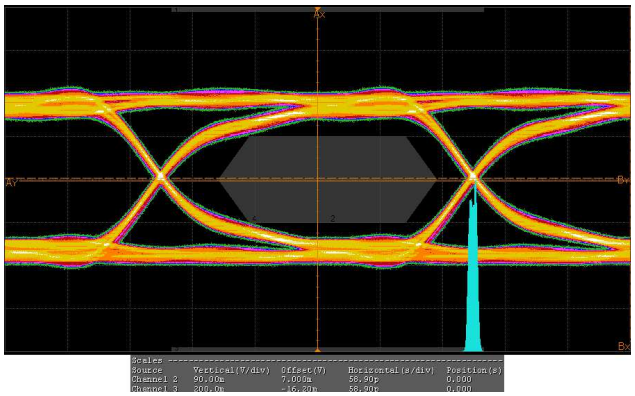


Figure 13. Eye diagram using EVM without TPD13S523 for the TMDS Lines at 1080p, 340MHz pixel clock, 3.4Gbps

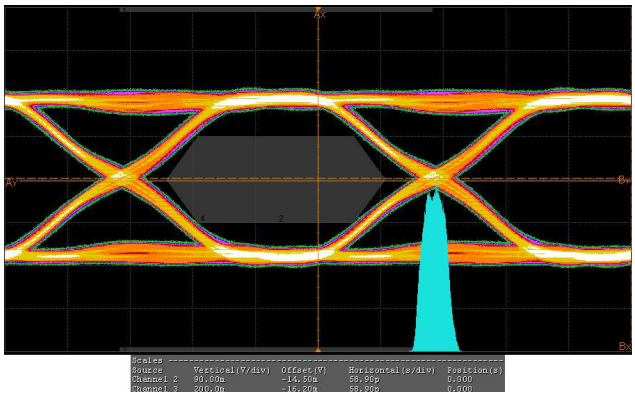


Figure 14. Eye diagram using EVM with TPD13S523 for the TMDS Lines at 1080p, 340MHz pixel clock, 3.4Gbps

REVISION HISTORY

Changes from Revision A (May 2012) to Revision B	Page
• Removed PREVIEW status from RSV package.	1
• Added RSV package to ORDERING INFORMATION table.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD13S523PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RA523	Samples
TPD13S523RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		ZTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

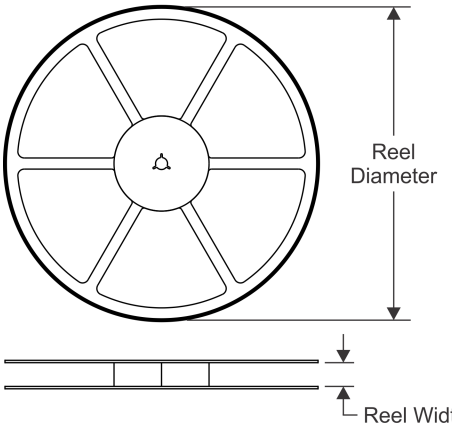
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

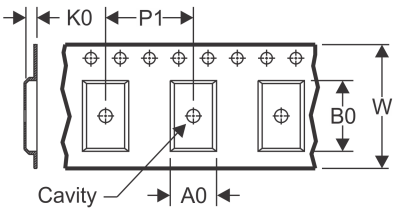
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

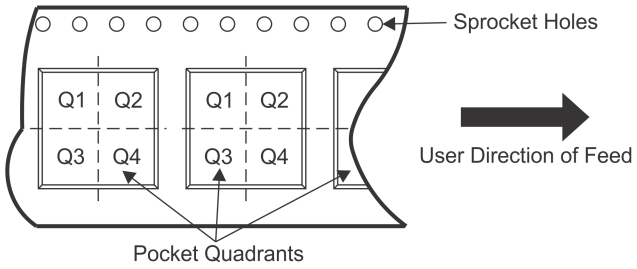


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

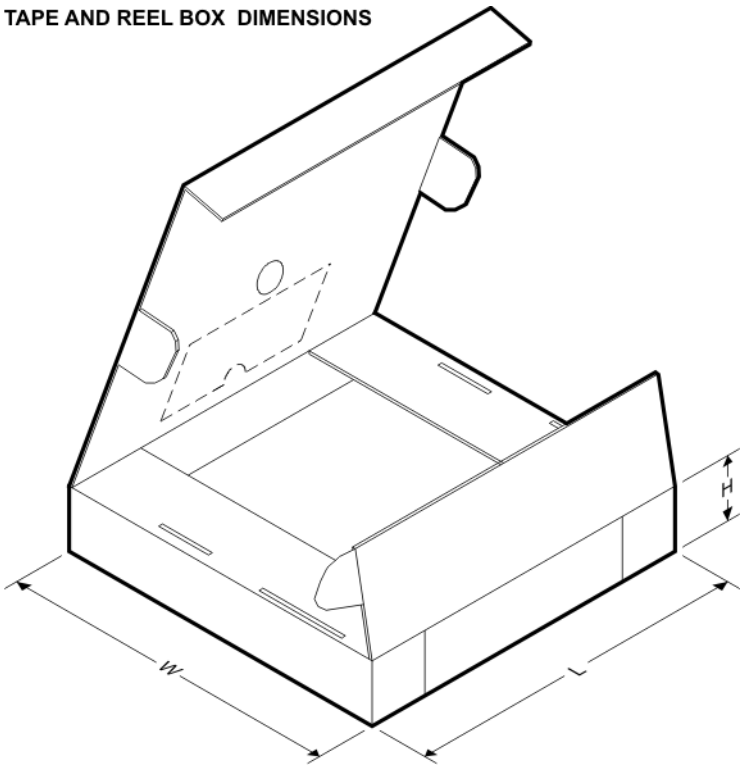
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD13S523PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPD13S523RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

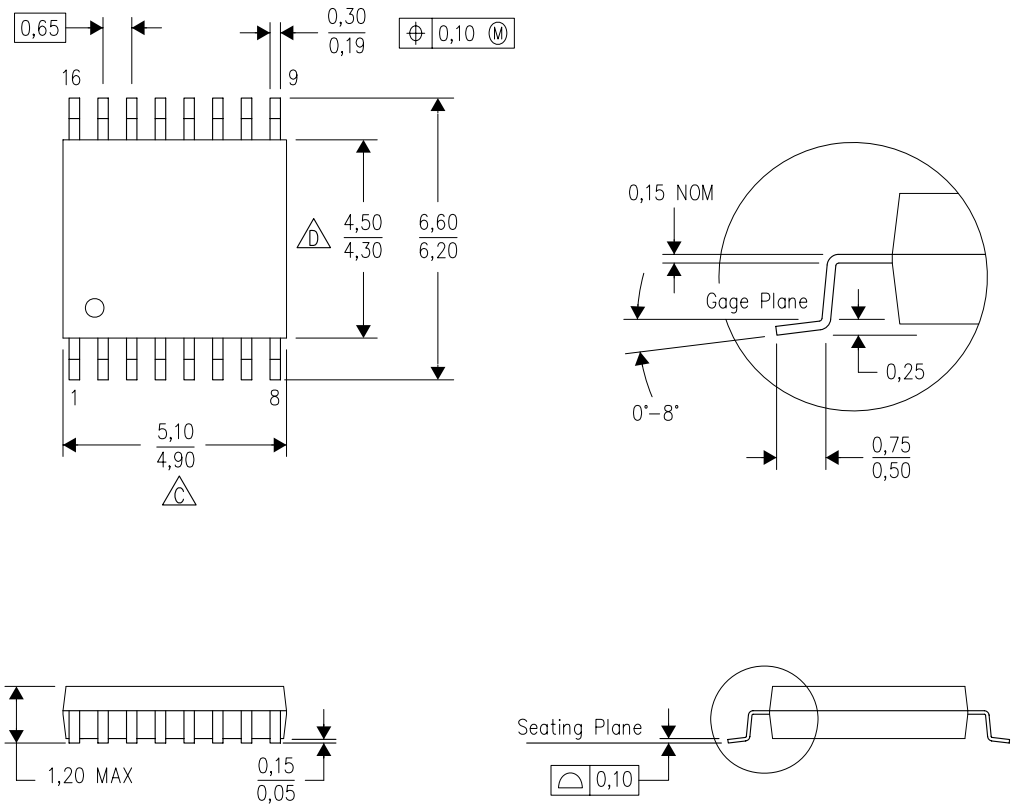
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD13S523PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TPD13S523RSVR	UQFN	RSV	16	3000	180.0	180.0	30.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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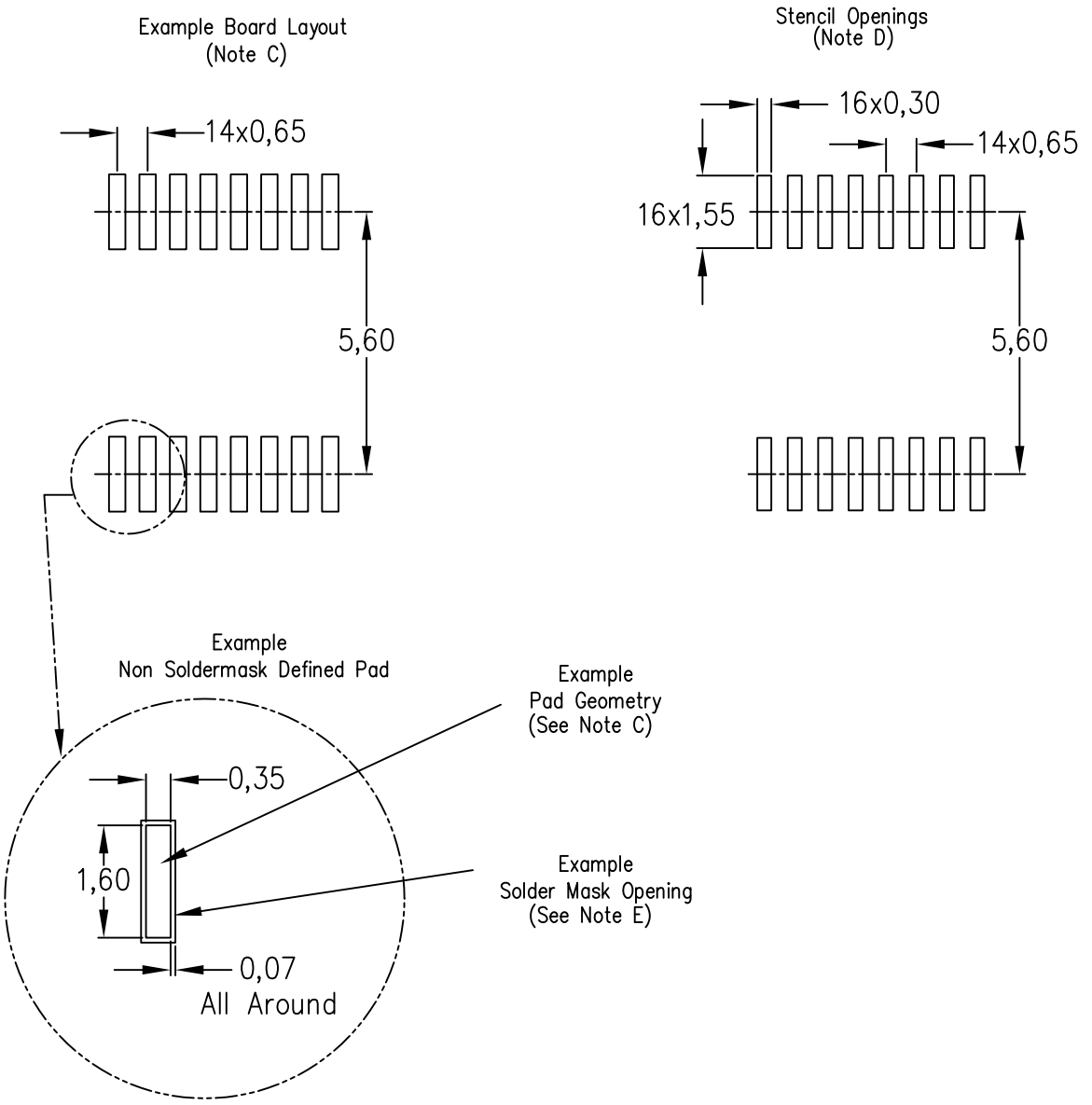
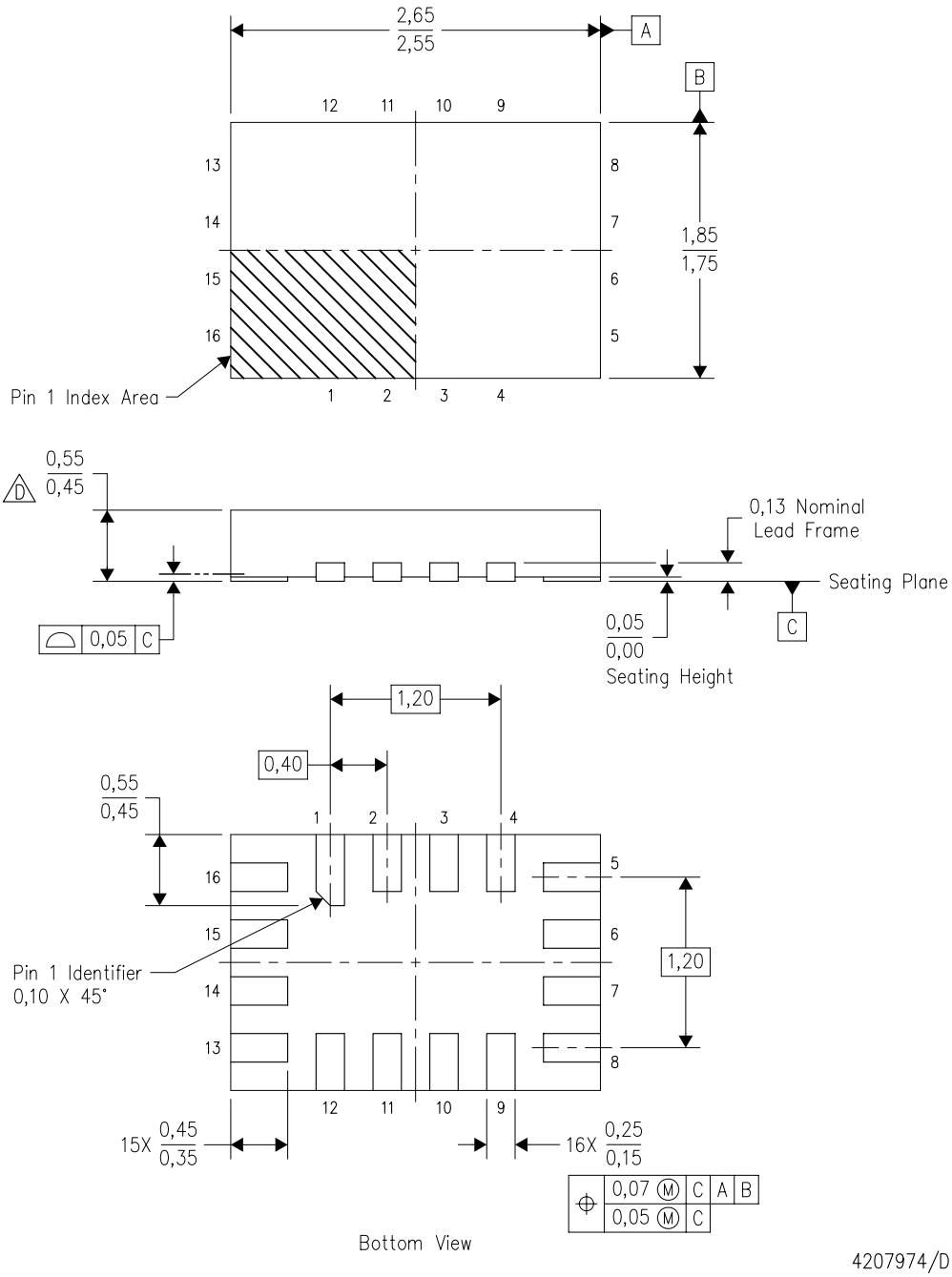
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



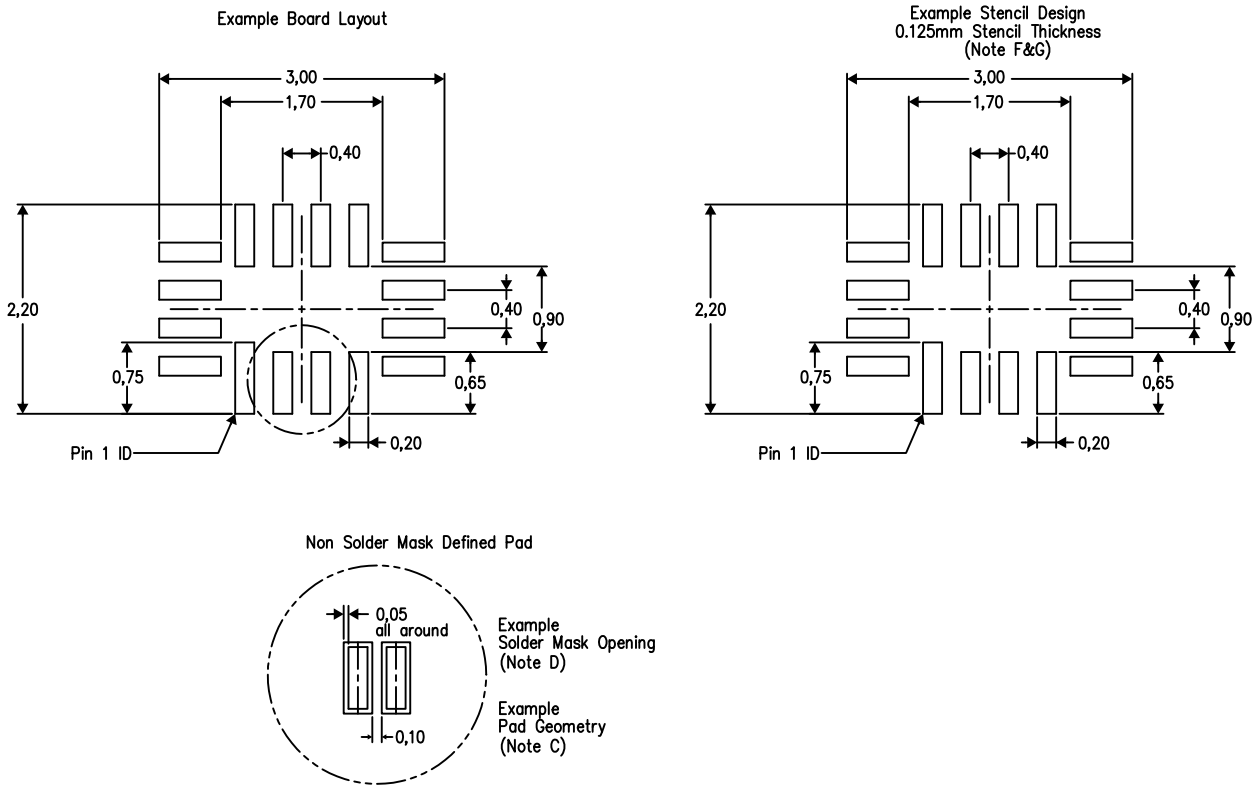
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

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