3.3-V AND/OR 5-V HIGH-SPEED DIGITAL ISOLATORS

Check for Samples: ISO721-Q1, ISO722-Q1

FEATURES

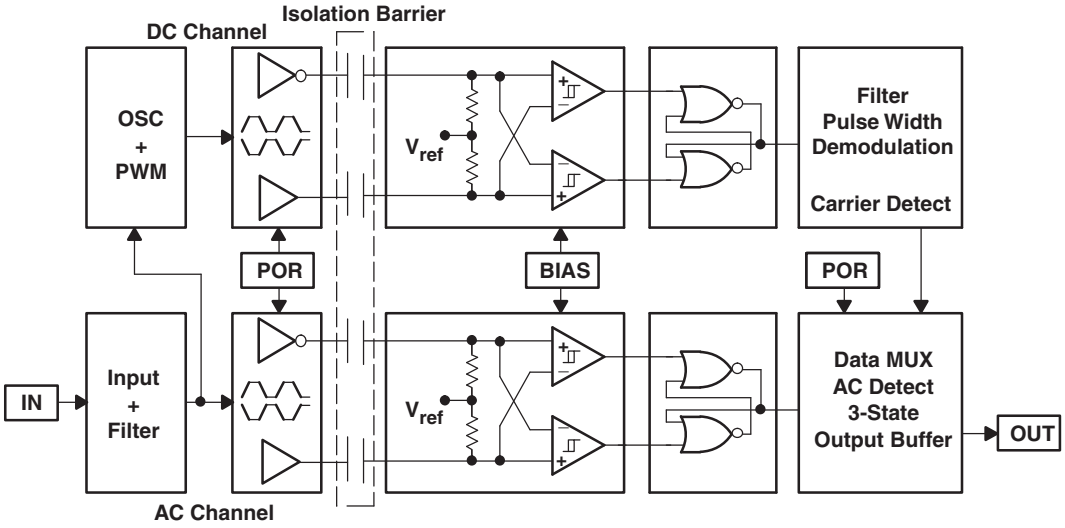
- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40ºC to 125ºC Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C5**
- **4000-$V_{(peak)}$ Isolation**
  - **UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1**
  - **50-kV/s Transient Immunity (Typ)**
- **Signaling Rate 0 Mbps to 100 Mbps**
  - **Low Propagation Delay**
  - **Low Pulse Skew (Pulse-Width Distortion)**
- **Low-Power Sleep Mode**
- **High Electromagnetic Immunity**
- **Low Input Current Requirement**
- **Failsafe Output**
- **Drop-In Replacement for Most Optical and Magnetic Isolators**

DESCRIPTION

The ISO72x-Q1 is a digital isolator with a logic input and output buffer separated by a silicon oxide (SiO_2) insulation barrier. This barrier provides galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

The capacitive isolation barrier conditions, translates to a balanced signal, then differentiates a binary input signal. Across the isolation barrier, a differential comparator receives the logic-transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse sent across the barrier ensures the proper dc level of the output. On failure to receive this dc refresh pulse for more than 4 µs, the response of the device is as if the input is or not actively driven, and the failsafe circuit drives the output to a logic-high state.

FUNCTION DIAGRAM



DESCRIPTION (CONTINUED)

The symmetry of the dielectric and capacitor within the integrated circuitry provides for close capacitive matching and allows fast transient voltage changes between the input and output grounds without corrupting the output. The small capacitance and resulting time constant provide for fast operation with signaling rates(1) from 0 Mbps (dc) to 100 Mbps.

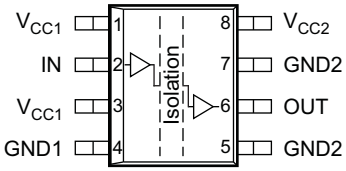
The device requires two supply voltages of 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply, and all outputs are 4-mA CMOS. The device has a TTL input threshold and a noise filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device.

The ISO722-Q1 device includes an active-low output enable that, when driven to a high logic level, places the output in a high-impedance state and turns off internal bias circuitry to conserve power.

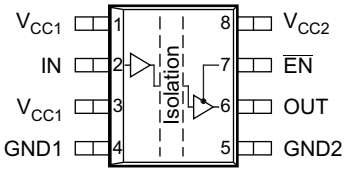
The ISO72x-Q1 is characterized for operation over the ambient temperature range of –40°C to 125°C.

(1) The signaling rate of a line is the number of voltage transitions that occur per second, expressed in the units bps (bits per second).

ISO721-Q1
D PACKAGE
(TOP VIEW)



ISO722-Q1
D PACKAGE
(TOP VIEW)



ORDERING AND PACKAGING INFORMATION

For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice: CA-5A	Recognized under 1577 Component Recognition Program(1)
File Number: 40016131	File Number: 1698195	File Number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}		–0.5 V to 6 V
V_I	Voltage at IN or OUT terminal		–0.5 V to 6 V
I_O	Output current		±15 mA
T_J	Maximum virtual-junction temperature		170°C
ESD	Electrostatic discharge rating	Human-Body Model(3)	±2 kV
		Charged-Device Model(4)	±1 kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values. Vrms values are not listed in this publication.
(3) JEDEC Standard 22, Test Method A114-C.01
(4) JEDEC Standard 22, Test Method C101

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}		3	5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current		–4		mA
t_{ui}	Input pulse duration		10		ns
V_{IH}	High-level input voltage (IN)		2	V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0	0.8	V
T_A	Operating free-air temperature		–40	125	°C
T_J	Operating virtual-junction temperature	See the Thermal Characteristics table		150	°C
H	External magnetic field intensity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input-to-output test voltage	After Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	672	V
		Method a, $V_{PR} = V_{IORM} \times 1.6$, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	V
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100 % Production test with t = 1 s, Partial discharge < 5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722-Q1 Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			10	14	
V_{OH}	High-level output voltage		I_{OH} = -4 mA, See Figure 1		V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	µA
I_{IL}	Low-level input current		IN at 0.8 V		–10			
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		15	50		kV/µs

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output		See Figure 1		17	24	ns
t_{PHL}	Propagation delay , high-to-low-level output		See Figure 1		17	24	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 1		0.5	2	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	3	ns
t_r	Output-signal rise time		See Figure 1		1		ns
t_f	Output-signal fall time		See Figure 1		1		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See Figure 2	6	8	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			3.5	4	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	5.5	8	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			4	5	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722-Q1	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		4	6.5	mA
		25 Mbps				5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1		V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	µA
I_{IL}	Low-level input current		IN at 0.8 V		–10			µA
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		15	40		kV/µs

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output		See Figure 1		19	30	ns
t_{PHL}	Propagation delay , high-to-low-level output		See Figure 1		19	30	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 1		0.5	3	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See Figure 2	7	13	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			5	6	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			5	6	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.3	0.5	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722-Q1 Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			10	14	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1		V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	µA
I_{IL}	Low-level input current		IN at 0.8 V		–10			µA
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		15	40		kV/µs

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output		See Figure 1		17	30	ns
t_{PHL}	Propagation delay , high-to-low-level output		See Figure 1		17	30	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 1		0.5	3	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See Figure 2	7	9	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			4.5	5	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	7	9	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			4.5	5	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V[(1)] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.3	0.5	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722-Q1 Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1		V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	µA
I_{IL}	Low-level input current		IN at 0.8 V		–10			µA
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5		15	40		kV/µs

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

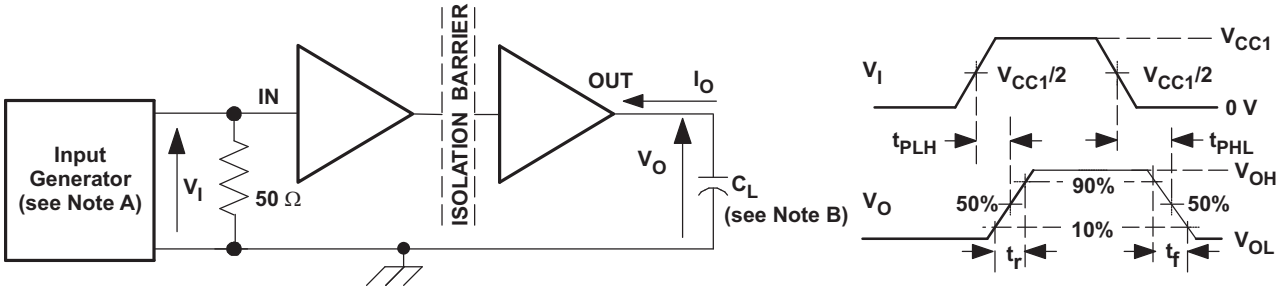
SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output		See Figure 1		20	34	ns
t_{PHL}	Propagation delay , high-to-low-level output		See Figure 1		20	34	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 1		0.5	3	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See Figure 2	7	13	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			5	6	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			5	6	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		100-Mbps NRZ data input, See Figure 6		2		ns
			100-Mbps unrestricted bit run length data input, See Figure 6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION



A. A generator having the following characteristics supplies the input pulse: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

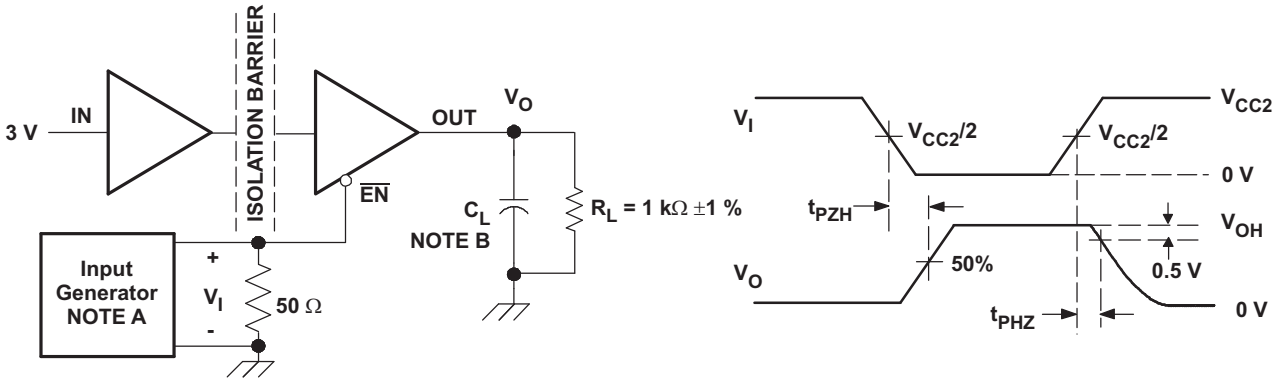


Figure 2. ISO722-Q1 Sleep-Mode High-Level Output Test Circuit and Voltage Waveforms

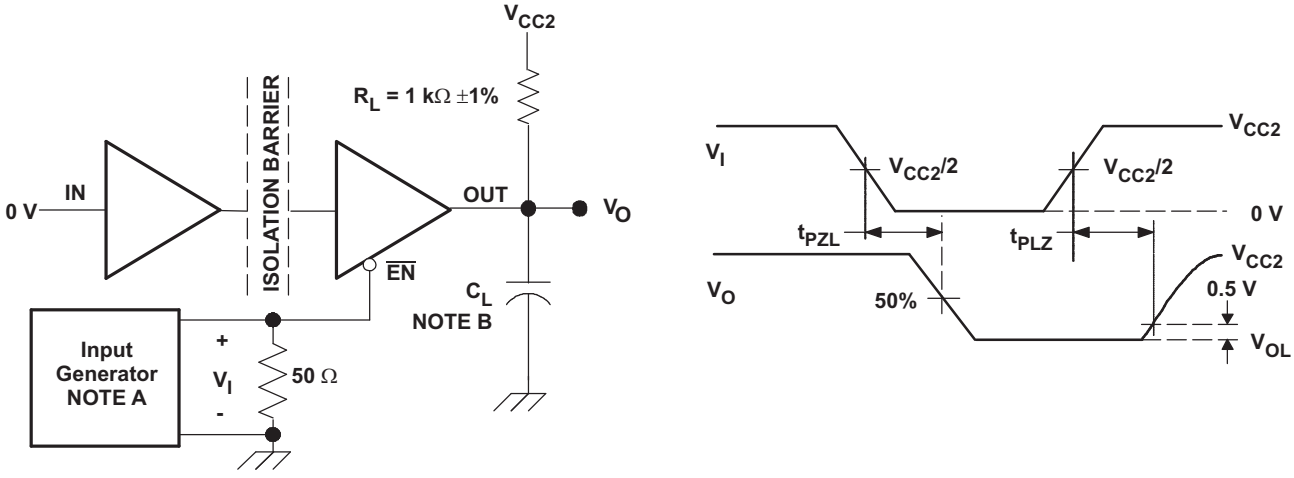


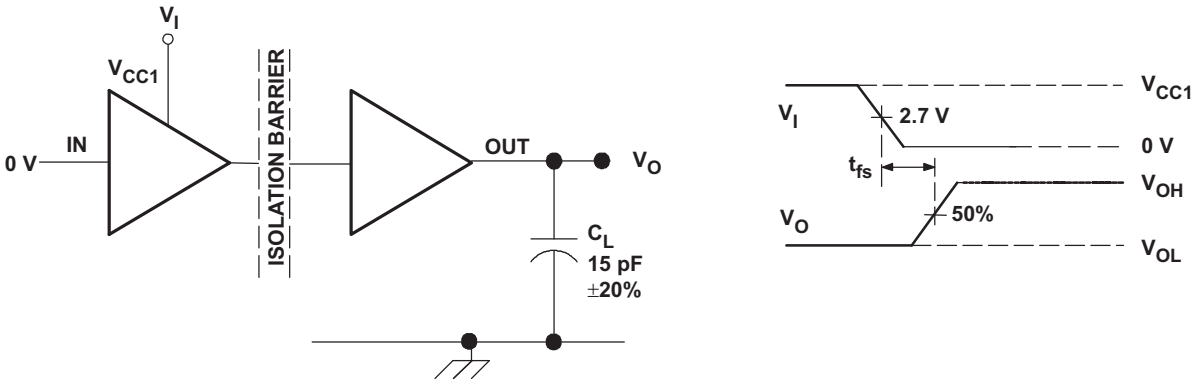
Figure 3. ISO722-Q1 Sleep-Mode Low-Level Output Test Circuit and Voltage Waveforms

NOTE

A: A generator having the following characteristics Supplies the input pulse: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

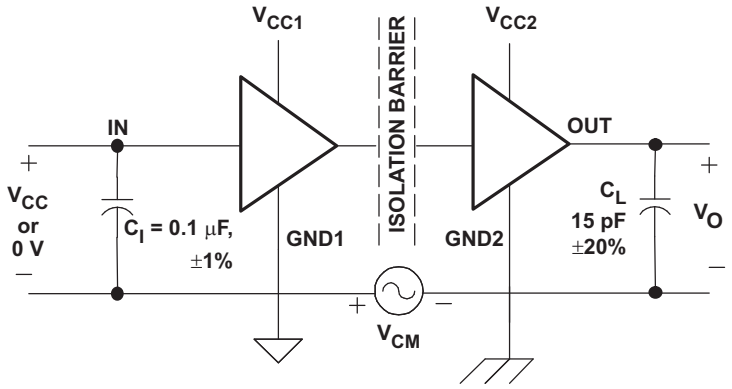
B: C_L = 15 pF ± 20% and includes instrumentation and fixture capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: V_I transition time is 100 ns.

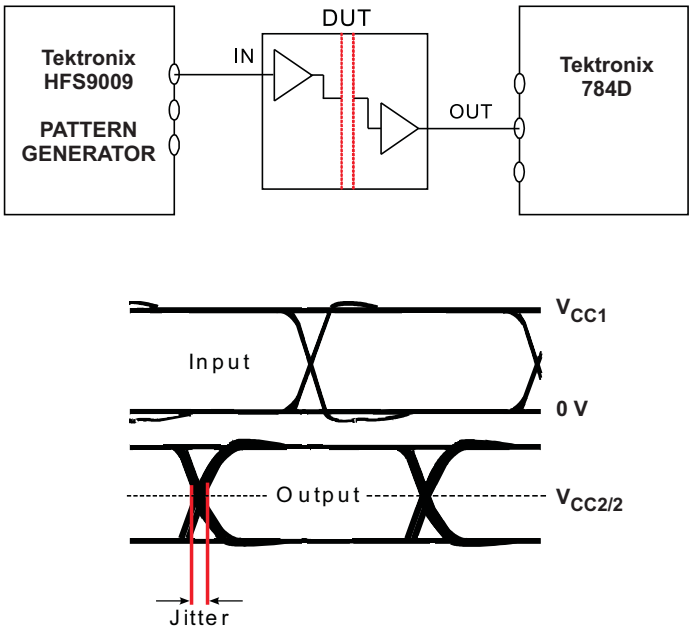
Figure 4. Failsafe Delay-Time Test Circuit and Voltage Waveforms



NOTE: Pass or fail criterion is no change in V_O.

Figure 5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: Bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(101)	Minimum air gap (clearance) (1)	Shortest terminal-to-terminal distance through air	4.8			mm
L(102)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
C_{TI}	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 Part 1	≥ 175			V
	Minimum internal gap (internal clearance)	Distance through insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		$>10^{12}$		Ω
		Input-to-output, V_{IO} = 500 V, 100°C ≤ T_A< T_A max.		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output	V_I = 0.4 sin (4E6πt)		1		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		1		pF

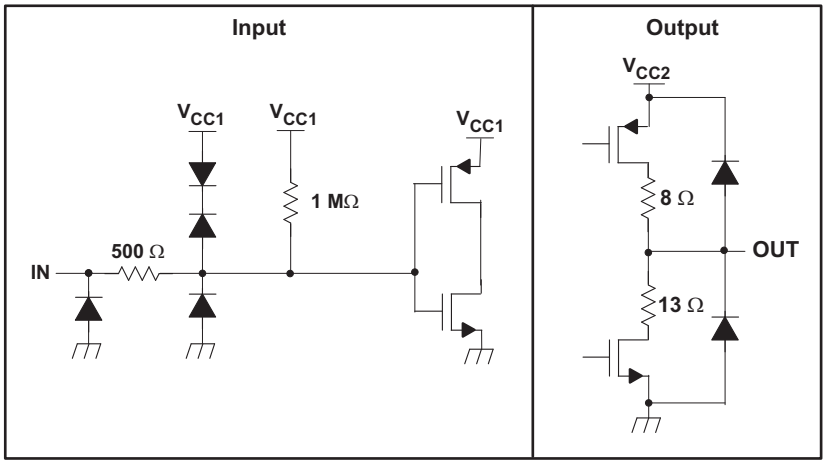
(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Take care to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Use techniques such as inserting grooves and/or ribs on a printed circuit board to help increase these specifications.

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III

DEVICE I/O SCHEMATIC

Figure 7. Equivalent Input and Output Schematic Diagrams



IEC SAFETY LIMITING VALUES

Safety limiting is designed to prevent potential damage to the isolation barrier on failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply, and without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 263°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C		100	mA
		θ_{JA} = 263°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C		153	
T_S	Maximum case temperature			150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

Table 2. THERMAL CHARACTERISTICS
(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K(1)		263		°C/W
		High-K(1)		125		
θ_{JB}	Junction-to-board thermal resistance			44		°C/W
θ_{JC}	Junction-to-case thermal resistance			75		°C/W
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 100-Mbps 50% duty cycle square wave			159	mW

(1) Tested in accordance with the low-K or high-K thermal metric definition of EIA/JESD51-3 for leaded surface-mount packages.

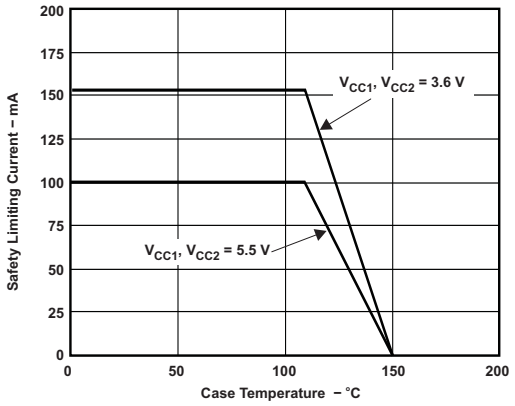


Figure 8. θ_{JC} Thermal Derating Curve Per IEC 60747-5-2

Table 3. FUNCTION TABLE(1)

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = powered up (V_{CC} ≥ 3 V), PD = powered down (V_{CC} ≤ 2.5 V), X = irrelevant, H = high level, L = low level

TYPICAL CHARACTERISTICS

RMS SUPPLY CURRENT versus SIGNALING RATE

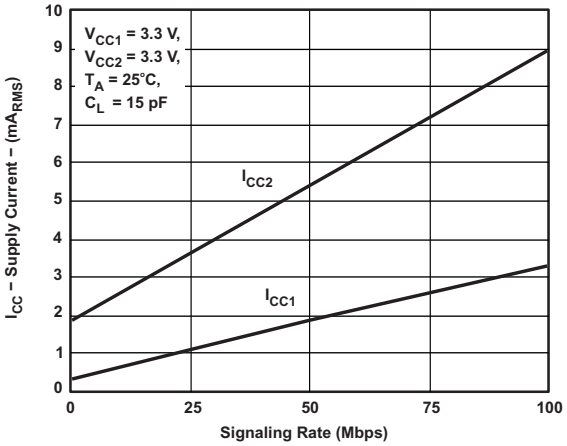


Figure 9.

RMS SUPPLY CURRENT versus SIGNALING RATE

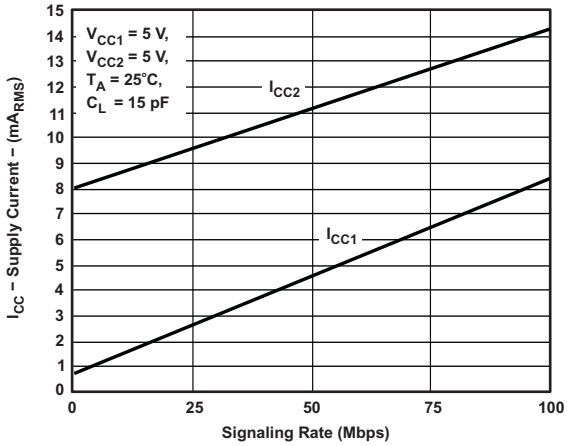


Figure 10.

PROPAGATION DELAY versus FREE-AIR TEMPERATURE

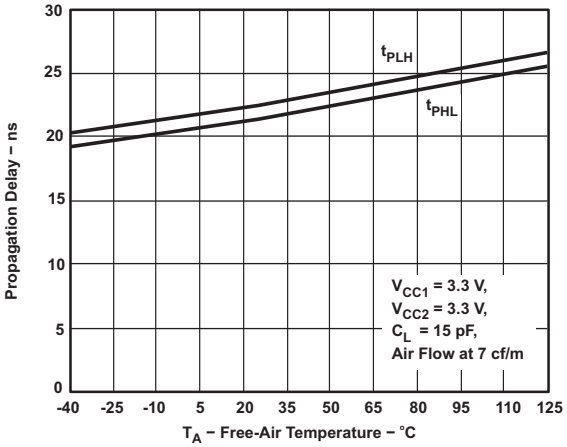


Figure 11.

PROPAGATION DELAY versus FREE-AIR TEMPERATURE

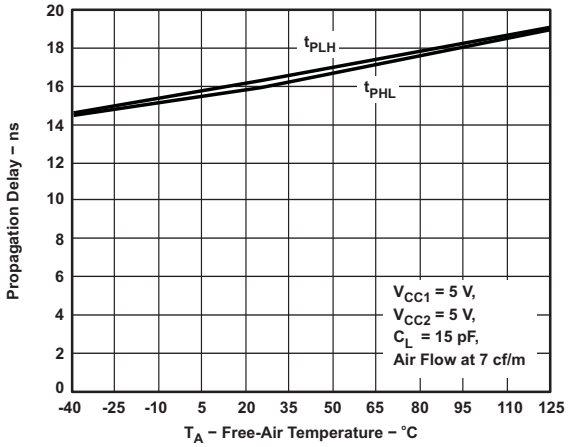


Figure 12.

INPUT THRESHOLD VOLTAGE versus FREE-AIR TEMPERATURE

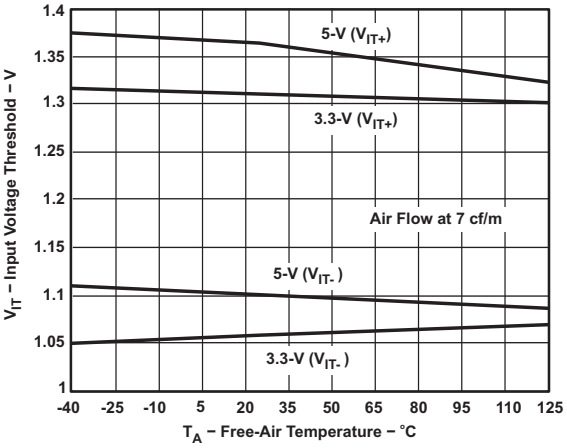


Figure 13.

V_{CC1} FAILSAFE THRESHOLD VOLTAGE versus FREE-AIR TEMPERATURE

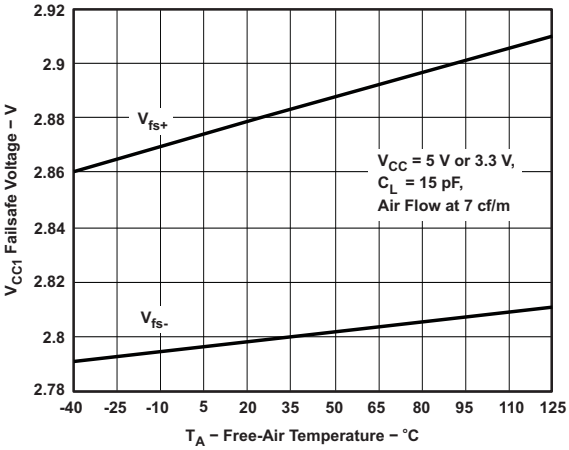


Figure 14.

TYPICAL CHARACTERISTICS (continued)

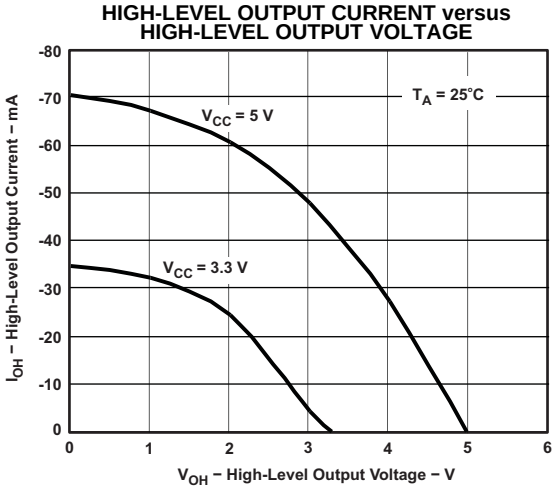


Figure 15.

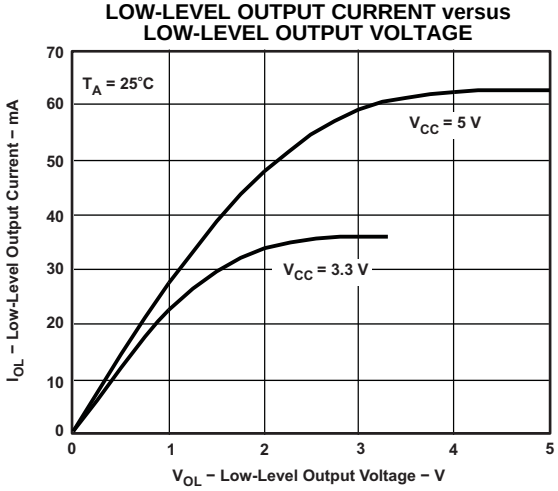


Figure 16.

APPLICATION INFORMATION

MANUFACTURER CROSS-REFERENCE DATA

The ISO72x-Q1 isolator has the same functional pinout as most other vendors, and it is often a pin-for-pin drop-in replacement. The notable differences in the product are propagation delay, signaling rate, power consumption, and transient protection rating. Use(1) as a guide for replacing other isolators with the ISO72x-Q1 single-channel isolators.

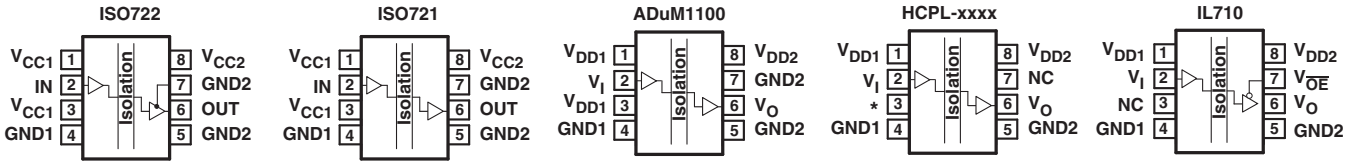


Figure 17. Pinout Cross-Reference

Table 4. Competitive Cross-Reference

ISOLATOR	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7		PIN 8
							ISO721	ISO722	
ISO721(1) (2)	V_{CC1}	IN	V_{CC1}	GND1	GND2	OUT	GND2	$\overline{EN}$	V_{CC2}
ADuM1100(1) (2)	V_{DD1}	V_I	V_{DD1}	GND1	GND2	V_O	GND2		V_{DD2}
HCPL-xxxx	V_{DD1}	V_I	Leave open(3)	GND1	GND2	V_O	NC(4)		V_{DD2}
IL710	V_{DD1}	V_I	NC(5)	GND1	GND2	V_O	$V_{\overline{OE}}$		V_{DD2}

(1) An HCPL device pin 7 must be floating (open) or grounded to use an ISO722 device as a drop-in replacement. Placing pin 7 of the ISO722 device in a high logic state disables the output of the device.
(1) The ISO721 pin 1 and pin 3 connect together internally. One may use either or both as V_{CC1}.
(2) The ISO721 pin 5 and pin 7 connect together internally. One may use either or both as GND2.
(3) Pin 3 of the HCPL devices must be open. This is not a problem when substituting an ISO721, because the extra V_{CC1} on pin 3 may be open-circuit as well.
(4) An HCPL device pin 7 must be floating (open) or grounded to use an ISO722 device as a drop-in replacement. Placing pin 7 of the ISO722 device in a high logic state disables the output of the device.
(5) Pin 3 of the IL710 must not tie to ground on the circuit board, because this shorts the ISO721 V_{CC1} to ground. The IL710 pin 3 may only tie to V_{CC} or be open to drop in an ISO721.

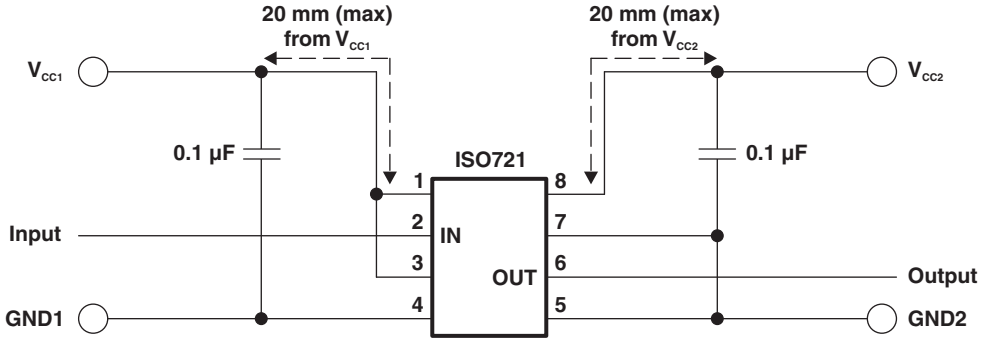
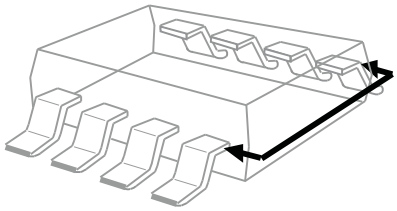


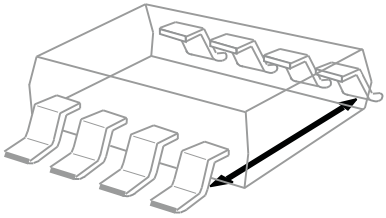
Figure 18. Basic Application Circuit

ISOLATION GLOSSARY

Creepage Distance—The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest-distance path is around the end of the package body.



Clearance—The shortest distance between two conductive input to output leads measured through air (line of sight)



Input-to-Output Barrier Capacitance—The total capacitance between all input terminals connected together, and all output terminals connected together

Input-to-Output Barrier Resistance—The total resistance between all input terminals connected together, and all output terminals connected together

Primary Circuit—An internal circuit directly connected to an external supply main or other equivalent source which supplies the primary-circuit electric power

Secondary Circuit—A circuit with no direct connection to primary power, and deriving its power from a separate isolated source

Comparative Tracking Index (CTI)—CTI is an index used for electrical insulating materials and defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, generating an electric spark. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. The name of this process is *tracking*.

Insulation

Operational insulation—Insulation needed for the correct operation of the equipment

Basic insulation—Insulation to provide basic protection against electric shock

Supplementary insulation-—Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation

Double insulation—Insulation comprising both basic and supplementary insulation

Reinforced insulation—A single insulation system that provides a degree of protection against electric shock equivalent to double insulation

Pollution Degree

Pollution Degree 1—No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2—Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3—Conductive pollution occurs or dry nonconductive pollution occurs that becomes conductive due to condensation, which is to be expected.

Pollution Degree 4–Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category

Overvoltage Category—This section addresses insulation coordination by identifying the transient overvoltages that may occur and by assigning four different levels as indicated in IEC 60664.

I: Signal Level-—Special equipment or parts of equipment

II: Local Level—Portable equipment, etc.

III: Distribution Level-—Fixed installation

IV: Primary Supply Level-—Overhead lines, cable systems

Each successive category should be subject to smaller transients than any higher-numbered category following it.

REVISION HISTORY

Changes from Revision B (June 2013) to Revision C	Page
• Changed temperature grade from 3 to 1	1

Changes from Revision A (September 2011) to Revision B	Page
• Added AEC-Q100 qualifications	1
• Changed signaling-rate limit to 100 Mbps	1
• Deleted Ordering Information table	3
• Changed last sentence in the Installation Category section	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO721QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	IS721Q	Samples
ISO722QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	IS722Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

OTHER QUALIFIED VERSIONS OF ISO721-Q1, ISO722-Q1 :

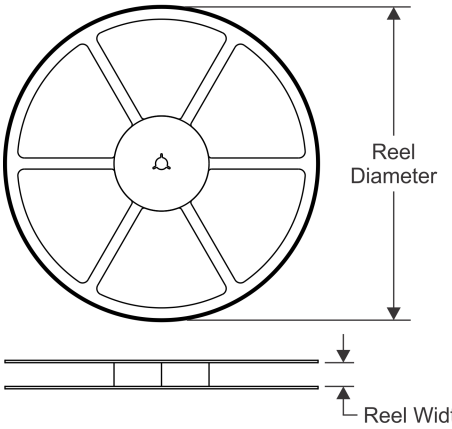
- Catalog: ISO721, ISO722

NOTE: Qualified Version Definitions:

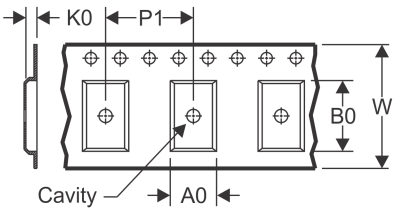
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

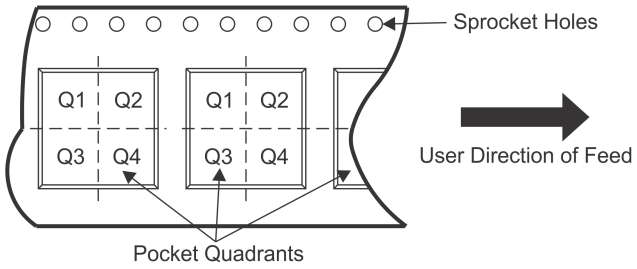


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

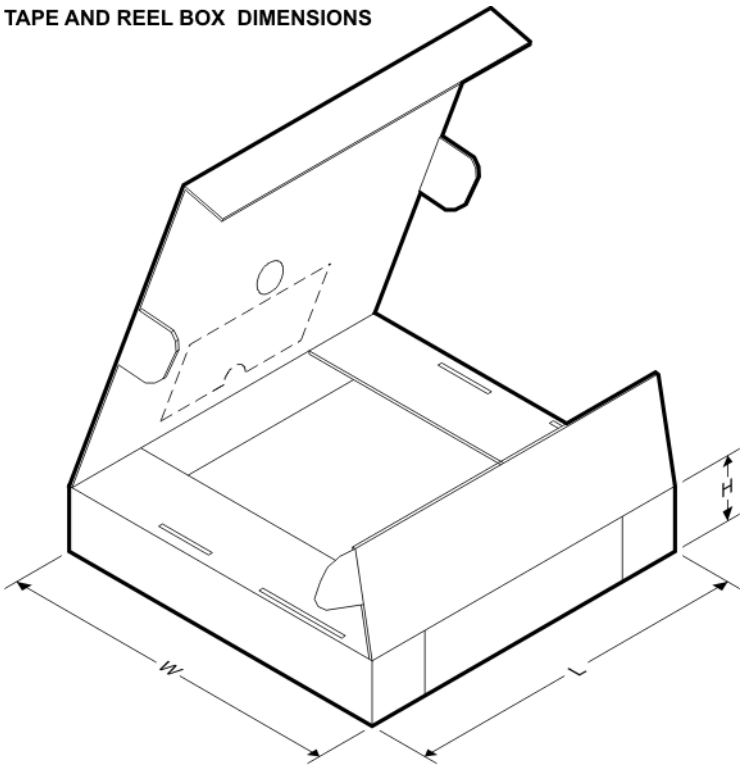
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO721QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

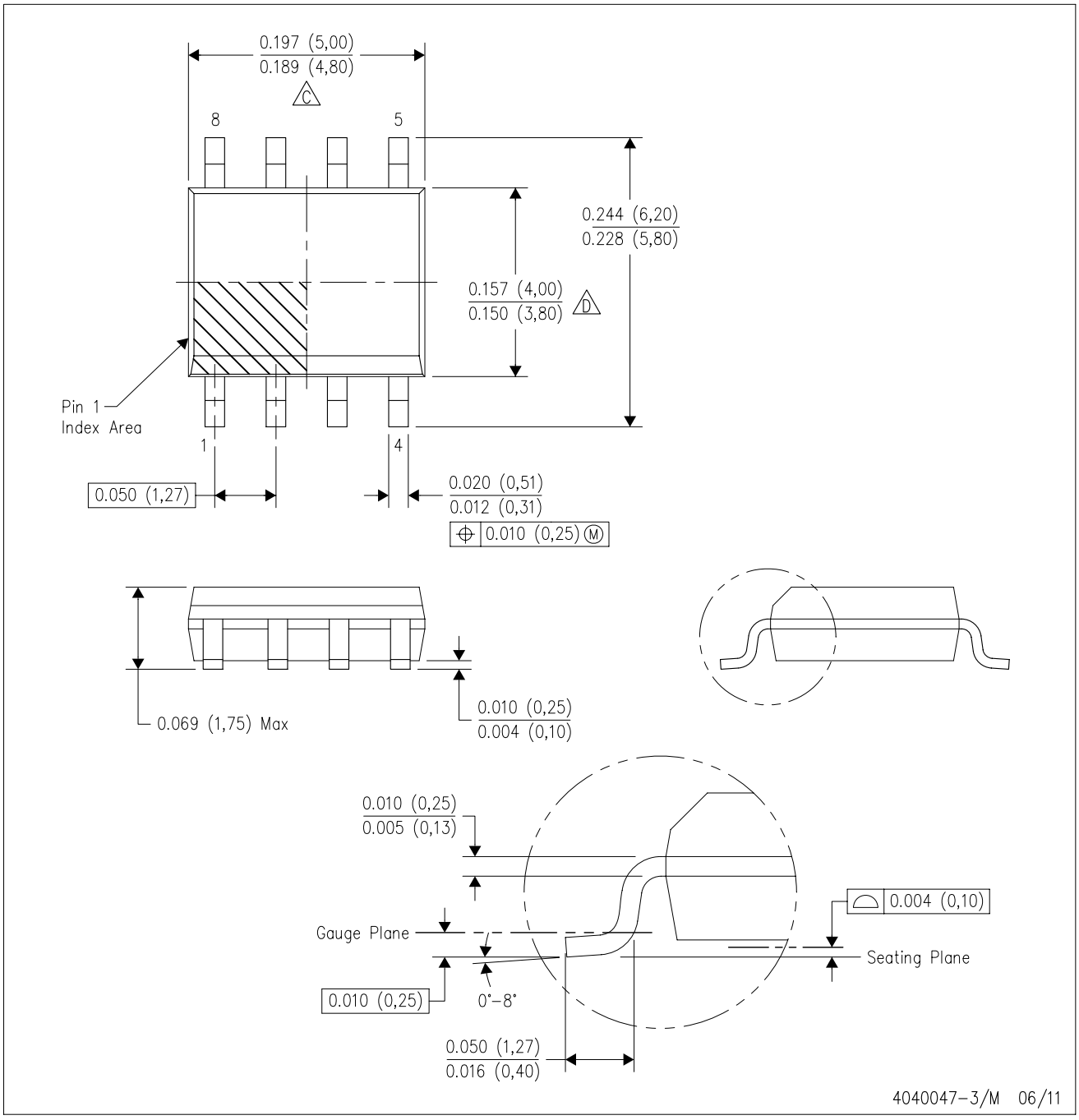
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

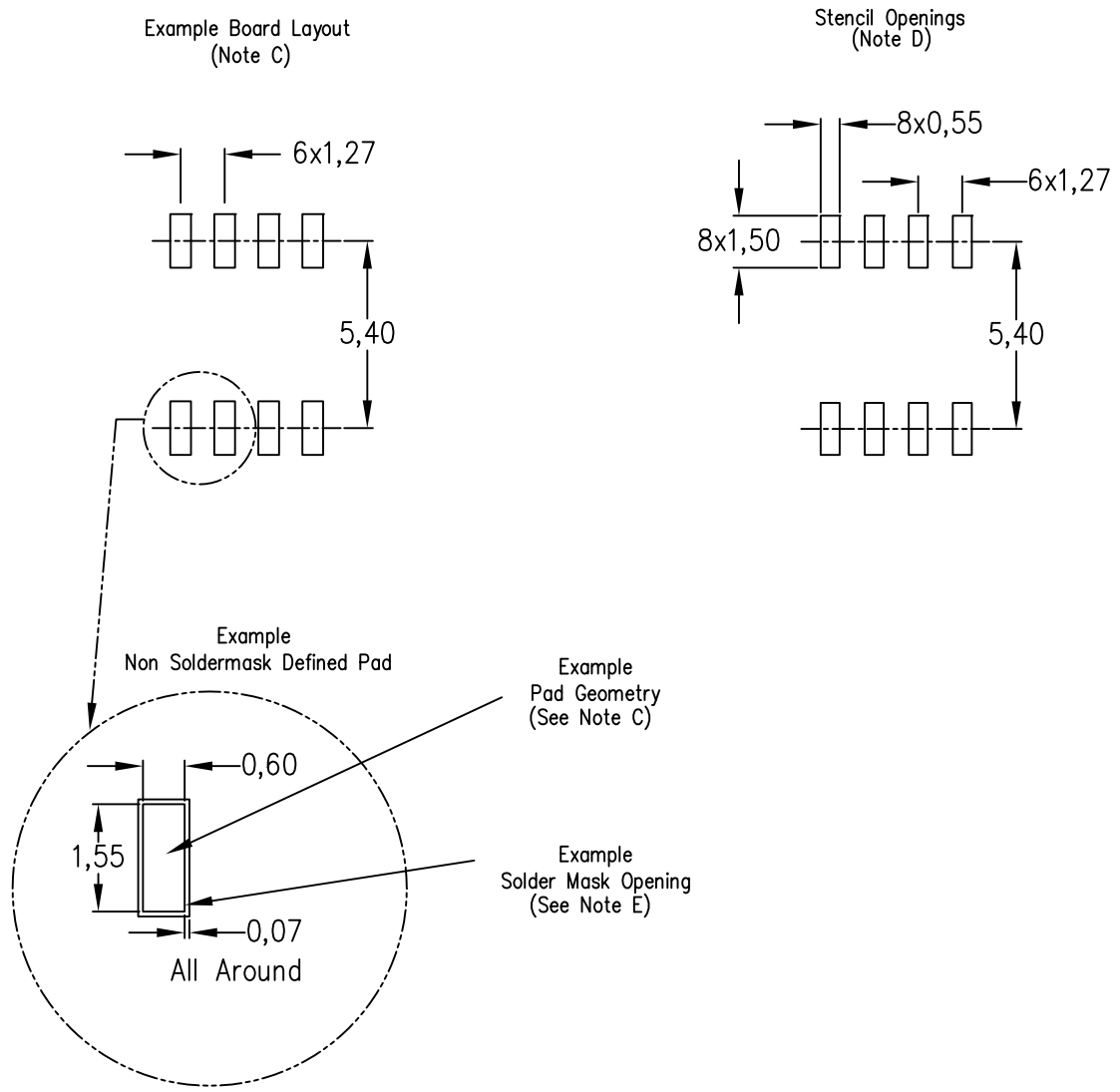
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO721QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
ISO722QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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