BLL6H1214-500; BLL6H1214LS-500

LDMOS L-band radar power transistor

Rev. 3 — 5 August 2013 Product data sheet

1. Product profile

1.1 General description

500 W LDMOS power transistor intended for L-band radar applications in the 1.2 GHz to 1.4 GHz range.

Table 1. Test information

Typical RF performance at T_{case} = 25 °C; t_p = 300 μs; δ = 10 %; I_{Dq} = 150 mA; in a class-AB production test circuit.

Test signal	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	1.2 to 1.4	50	500	17	50	20	6

1.2 Features and benefits

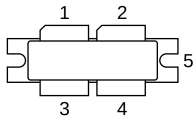
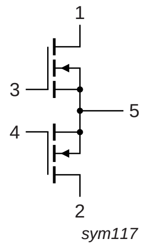
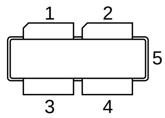
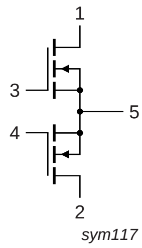
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1.2 GHz to 1.4 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLL6H1214-500 (SOT539A)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		
BLL6H1214LS-500 (SOT539B)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL6H1214-500	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLL6H1214LS-500	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
BLL6H1214-500				
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 500 W		
		t_p = 100 µs; δ = 10 %	0.07	K/W
		t_p = 200 µs; δ = 10 %	0.08	K/W
		t_p = 300 µs; δ = 10 %	0.1	K/W
		t_p = 100 µs; δ = 20 %	0.1	K/W
BLL6H1214LS-500				
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 500 W		
		t_p = 100 µs; δ = 10 %	0.046	K/W
		t_p = 200 µs; δ = 10 %	0.059	K/W
		t_p = 300 µs; δ = 10 %	0.069	K/W
		t_p = 100 µs; δ = 20 %	0.064	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.3	1.8	2.2	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	32	42	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 270 mA	1.7	3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.5 A	-	100	164	mΩ

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 300 µs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 150 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		500	-	-	W
V_{DS}	drain-source voltage	P_L = 500 W	-	-	50	V
G_p	power gain	P_L = 500 W	15	17	-	dB
RL_{in}	input return loss	P_L = 500 W	-	−10	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	600	-	W
η_D	drain efficiency	P_L = 500 W	45	50	-	%

Table 7. RF characteristics *...continued*

Test signal: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 150 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{droop(pulse)}$	pulse droop power	P_L = 500 W	-	0	0.3	dB
t_r	rise time	P_L = 500 W	-	20	50	ns
t_f	fall time	P_L = 500 W	-	6	50	ns

7. Test information

7.1 Ruggedness in class-AB operation

The BLL6H1214-500 and BLL6H1214LS-500 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 150 mA; P_L = 500 W; t_p = 300 μs; δ = 10 %.

7.2 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f (GHz)	Z_S (Ω)	Z_L (Ω)
1.2	1.268 – j2.623	2.987 – j1.664
1.3	2.193 – j2.457	2.162 – j1.326
1.4	2.359 – j2.052	1.604 – j1.887

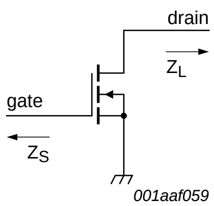


Fig 1. Definition of transistor impedance

7.3 Test circuit

Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	22 μF, 35 V	
C2	multilayer ceramic chip capacitor	51 pF	[1]
C3, C4	multilayer ceramic chip capacitor	100 pF	[1]
C5, C11, C12	multilayer ceramic chip capacitor	1 nf	[2]
C6	multilayer ceramic chip capacitor	47 pF	[1]
C7, C8, C10	multilayer ceramic chip capacitor	51 pF	[3]

Table 9. List of components *...continued*

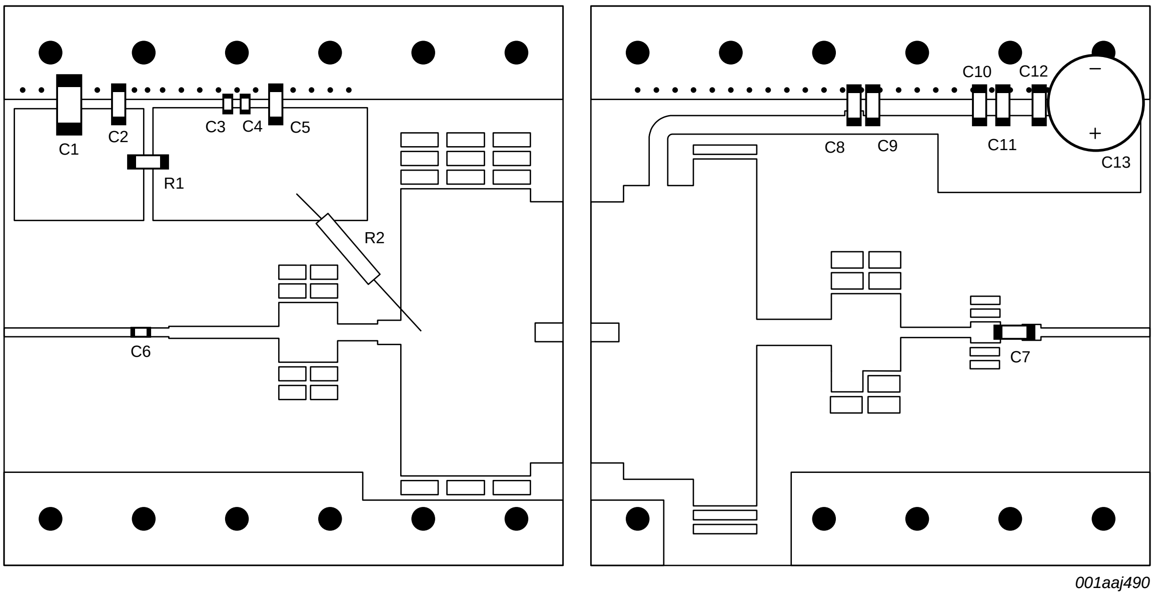
For test circuit see Figure 2.

Component	Description	Value		Remarks
C9	multilayer ceramic chip capacitor	100 pF	[3]	
C13	electrolytic capacitor	10 μF, 63 V		
R1	SMD resistor	56 Ω		0603
R2	metal film resistor	51 Ω		

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 800B or capacitor of same quality.



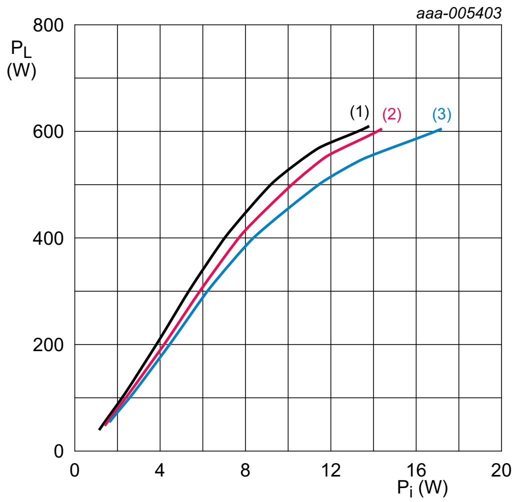
Printed-Circuit Board (PCB): Duroid 6006; ε_r = 6.15 F/m; thickness = 0.64 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 2. Component layout for class-AB production test circuit

7.4 RF performance graphs

7.4.1 Performance curves measured with δ = 10 %, t_p = 300 μs and T_h = 25 °C



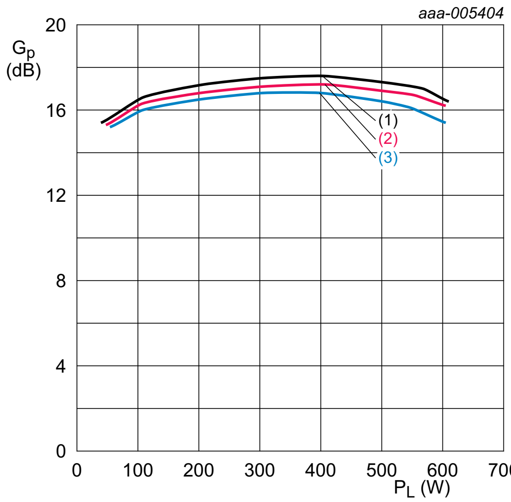
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 3. Output power as a function of input power; typical values



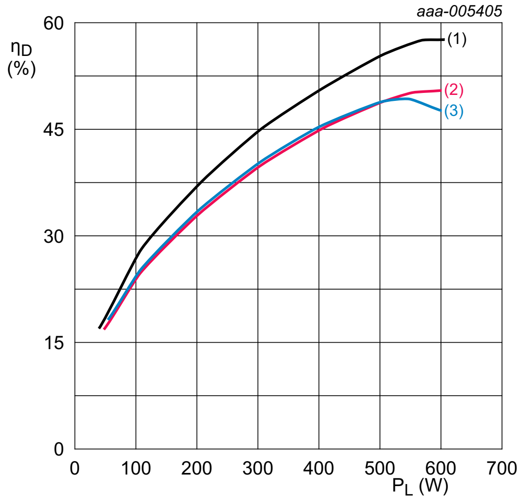
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 4. Power gain as a function of output power; typical values



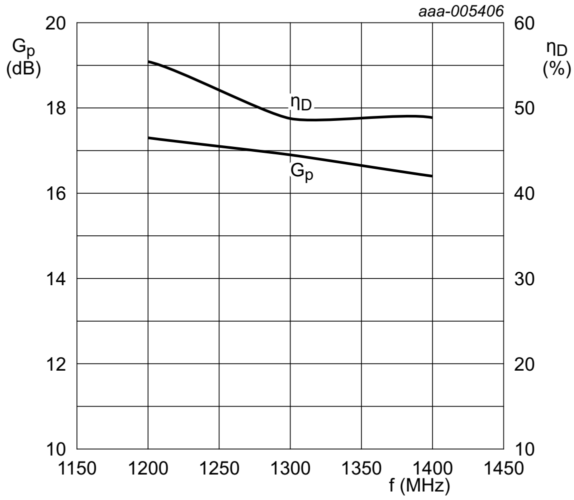
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

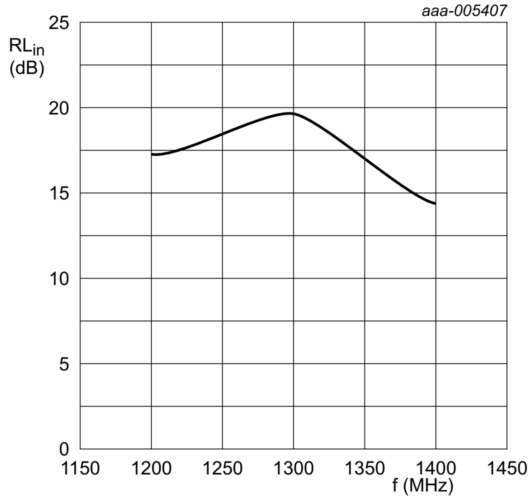
(3) f = 1400 MHz

Fig 5. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; P_L = 500 W; I_{Dq} = 150 mA.

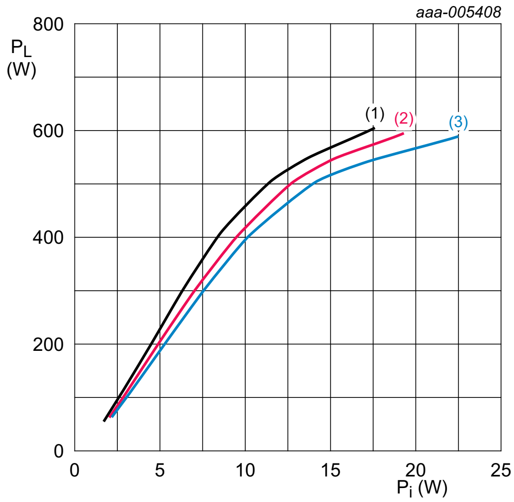
Fig 6. Power gain and drain efficiency as function of frequency; typical values



V_{DS} = 50 V; P_L = 500 W; I_{Dq} = 150 mA.

Fig 7. Input return loss as a function of frequency; typical value

7.4.2 Performance curves measured with δ = 10 %, t_p = 300 μs and T_h = 65 °C



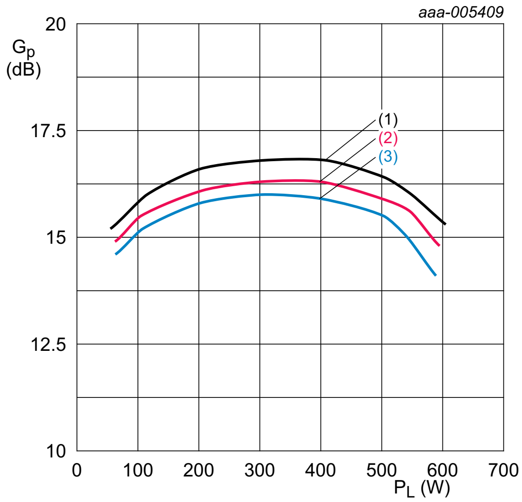
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 8. Output power as a function of input power; typical values



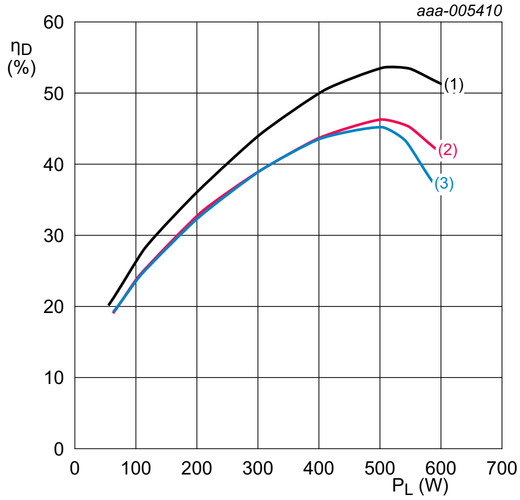
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 9. Power gain as a function of output power; typical values



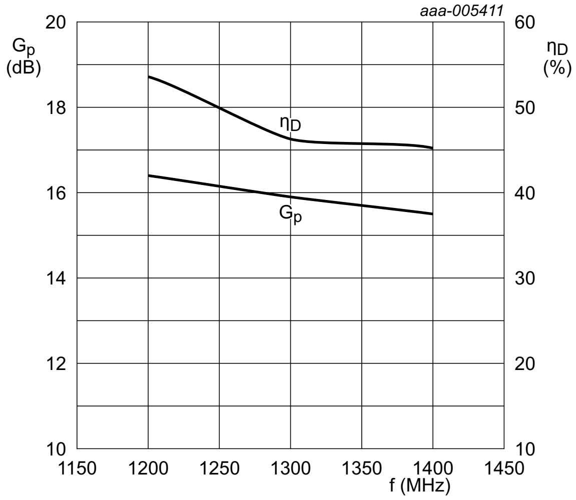
V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

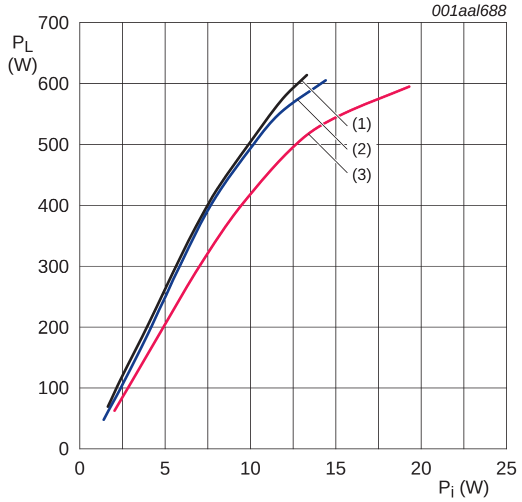
Fig 10. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; P_L = 500 W; I_{Dq} = 100 mA.

Fig 11. Power gain and drain efficiency as function of frequency; typical values

7.4.3 Performance curves measured with δ = 10 %, t_p = 300 μs and f = 1300 MHz



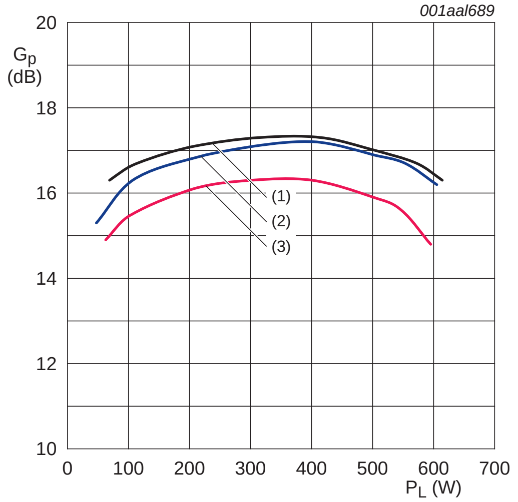
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) T_h = –40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 12. Output power as a function of input power; typical values



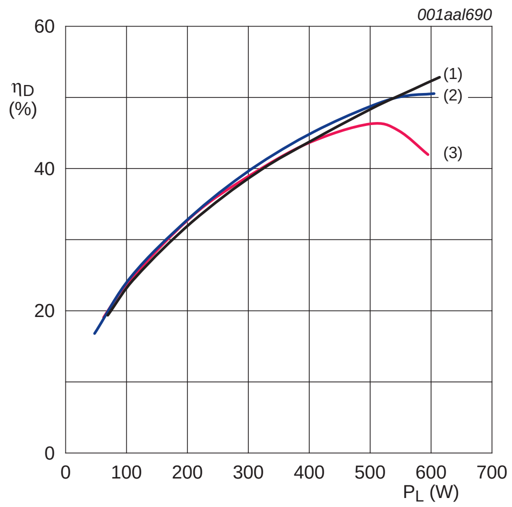
V_{DS} = 50 V;I_{Dq} = 150 mA.

(1) T_h = –40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 13. Power gain as a function of output power; typical values



V_{DS} = 50 V;I_{Dq} = 150 mA.

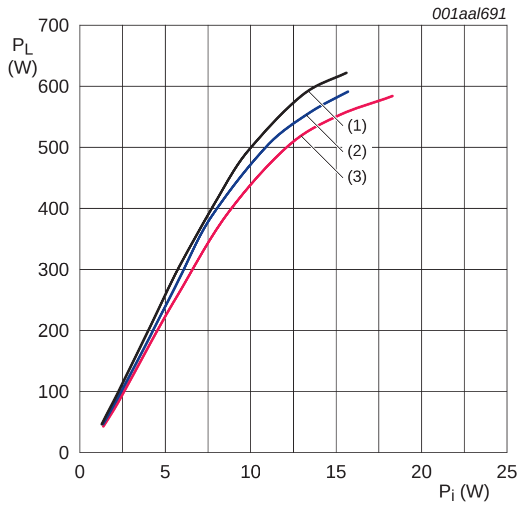
(1) T_h = −40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 14. Drain efficiency as a function of output power; typical values

7.4.4 Performance curves measured with δ = 20 %, t_p = 500 μs and T_h = 25 °C



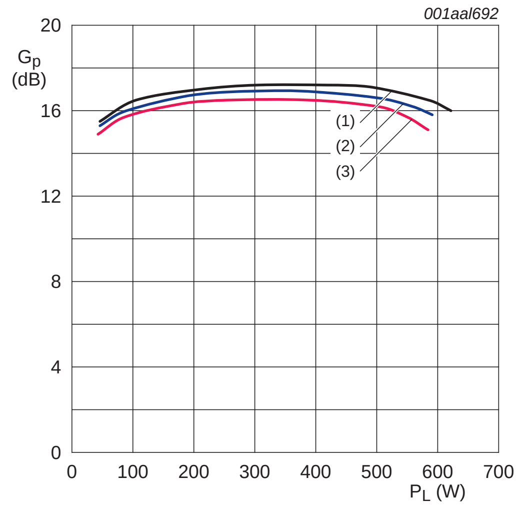
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 15. Output power as a function of input power; typical values



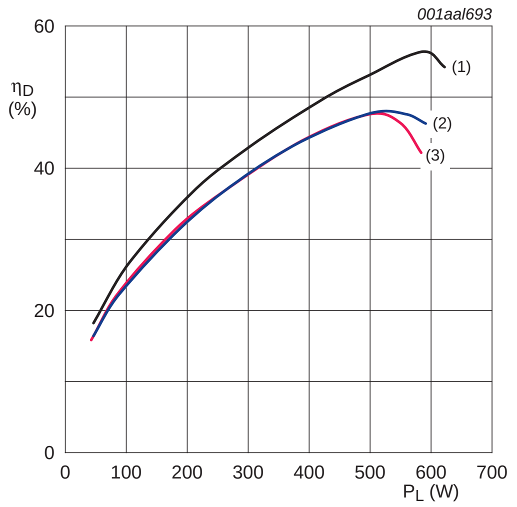
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 16. Power gain as a function of output power; typical values



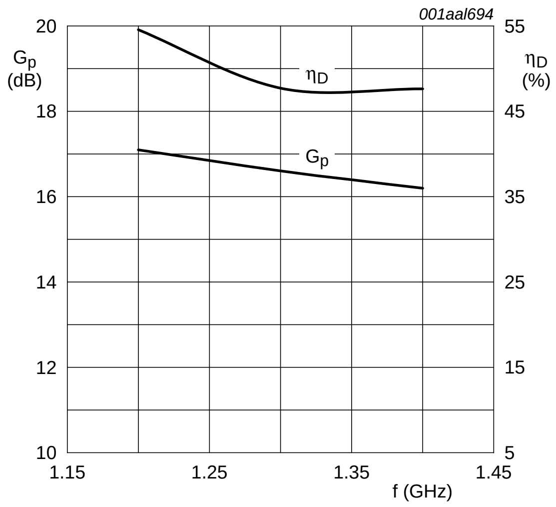
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

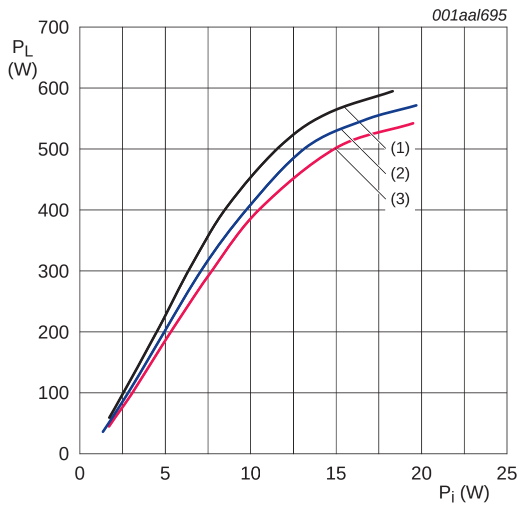
Fig 17. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 150 mA.

Fig 18. Power gain and drain efficiency as function of frequency; typical values

7.4.5 Performance curves measured with δ = 20 %, t_p = 500 μs and T_h = 65 °C



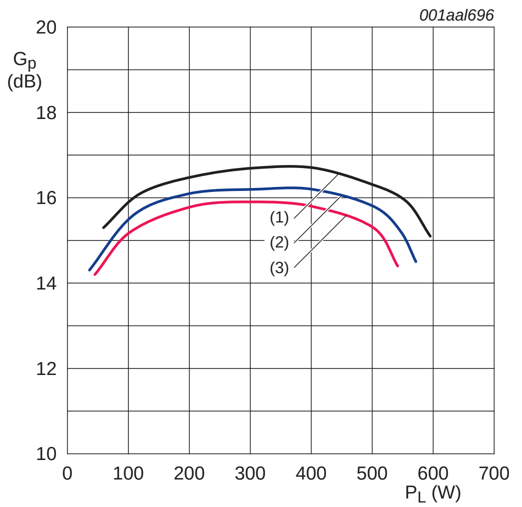
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 19. Output power as a function of input power; typical values



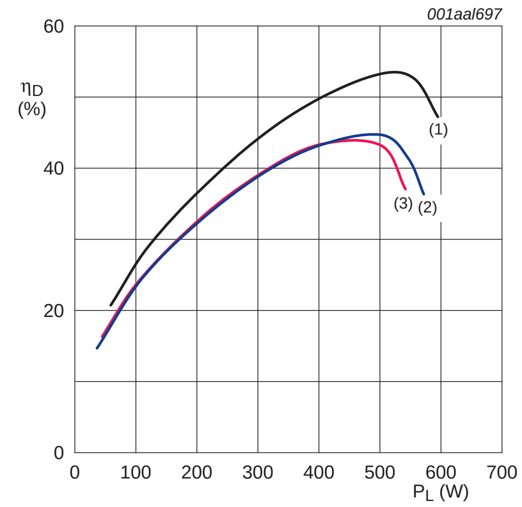
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 20. Power gain as a function of output power; typical values



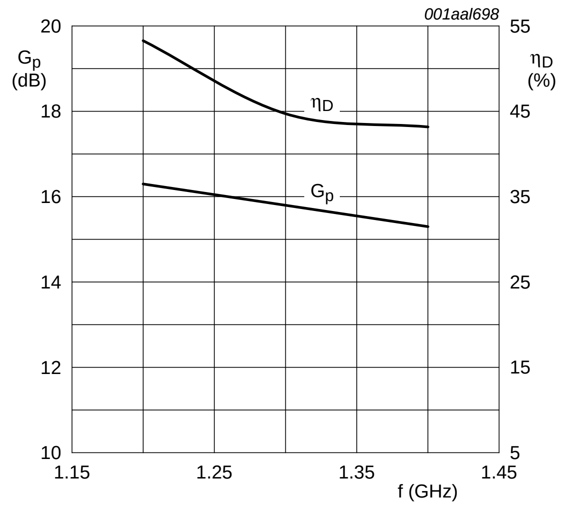
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

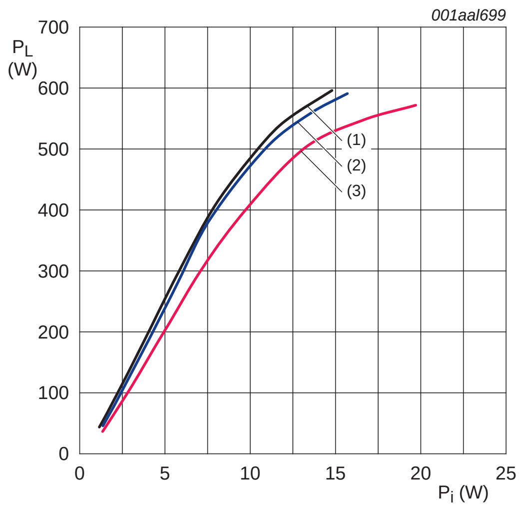
Fig 21. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 150 mA.

Fig 22. Power gain and drain efficiency as function of frequency; typical values

7.4.6 Performance curves measured with δ = 20 %, t_p = 500 μs and f = 1300 MHz



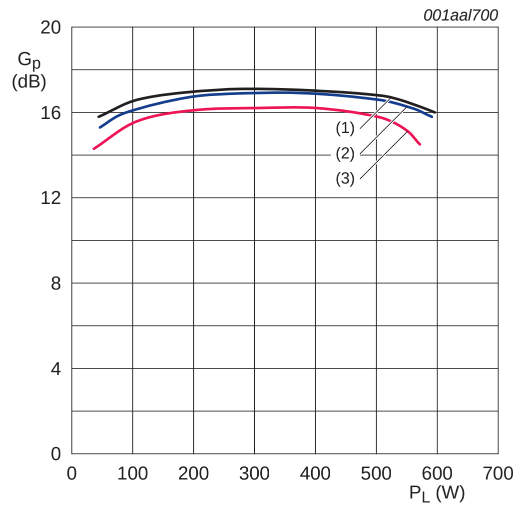
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) T_h = −40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 23. Output power as a function of input power; typical values



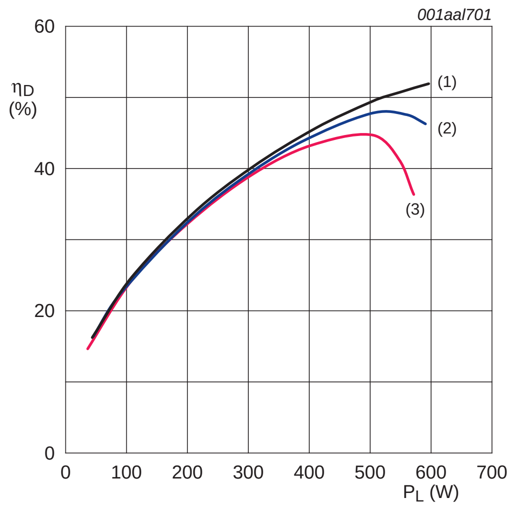
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) T_h = −40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 24. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 150 mA.

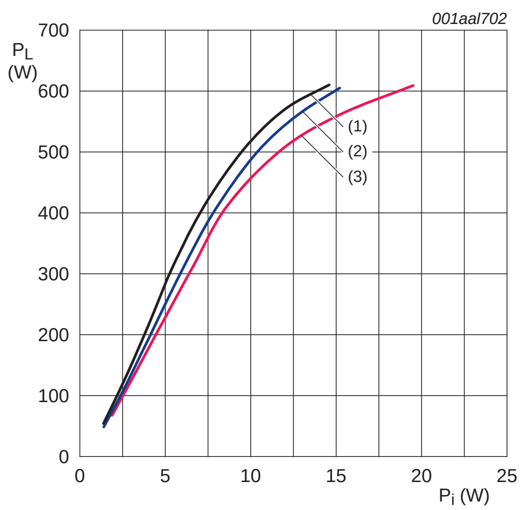
(1) T_h = −40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 25. Drain efficiency as a function of output power; typical values

7.4.7 Performance curves measured with δ = 10 %, t_p = 1 ms and T_h = 25 °C



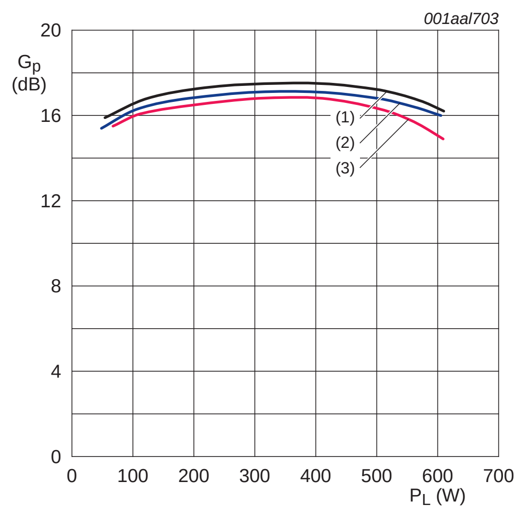
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 26. Output power as a function of input power; typical values



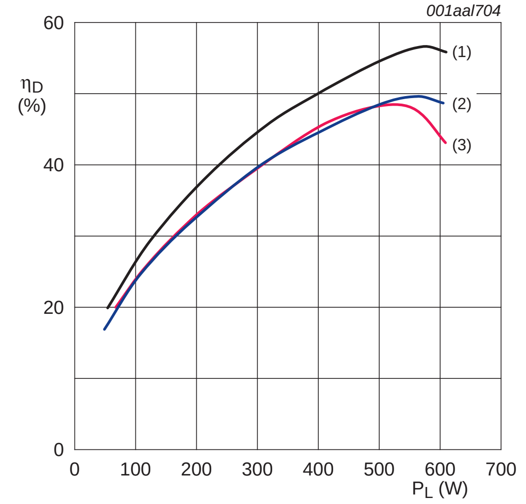
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 27. Power gain as a function of output power; typical values



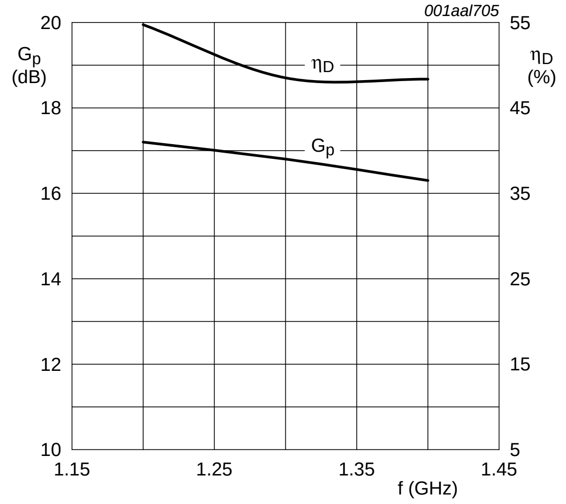
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

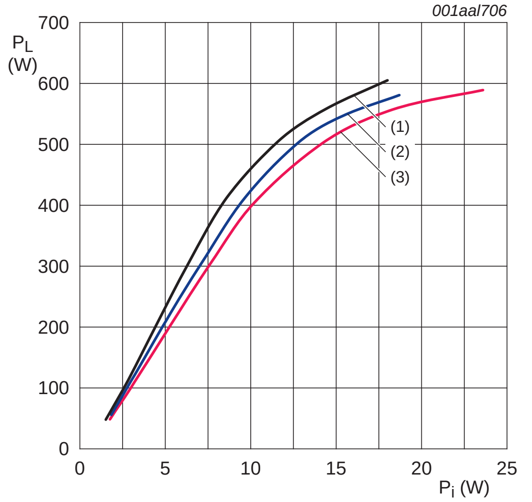
Fig 28. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 150 mA.

Fig 29. Power gain and drain efficiency as function of frequency; typical values

7.4.8 Performance curves measured with δ = 10 %, t_p = 1 ms and T_h = 65 °C



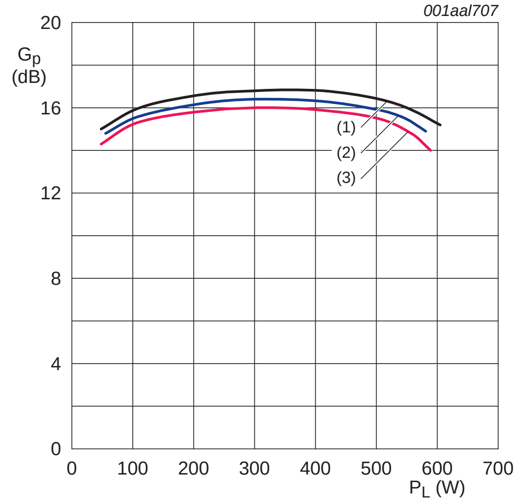
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 30. Output power as a function of input power; typical values



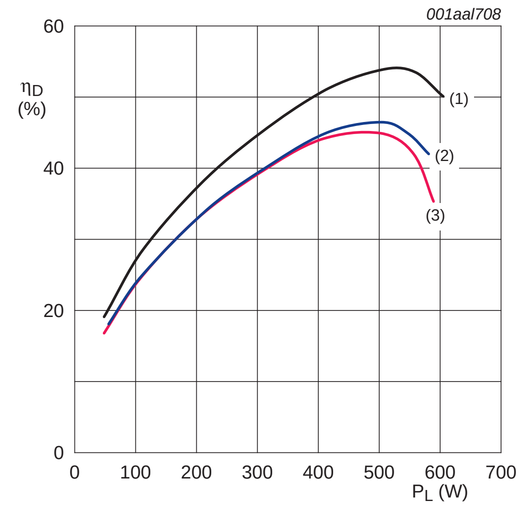
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 31. Power gain as a function of output power; typical values



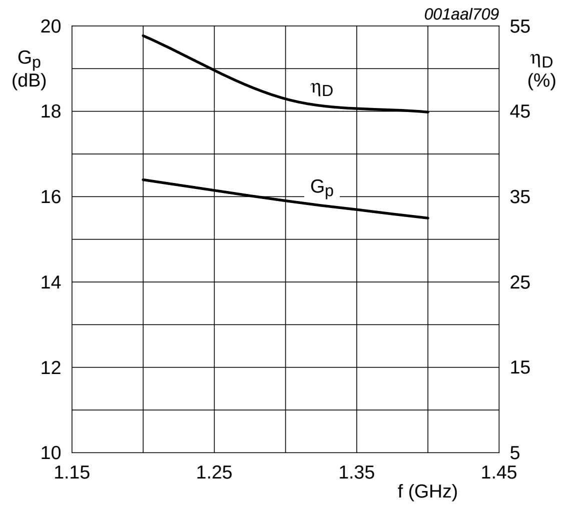
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

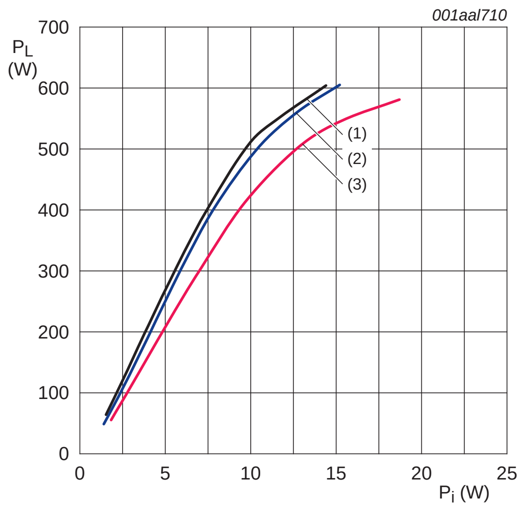
Fig 32. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 150 mA.

Fig 33. Power gain and drain efficiency as function of frequency; typical values

7.4.9 Performance curves measured with δ = 10 %, t_p = 1 ms and f = 1300 MHz



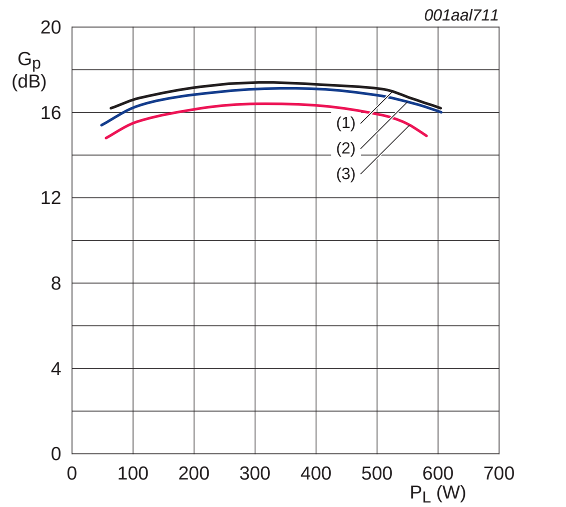
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) T_h = –40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 34. Output power as a function of input power; typical values



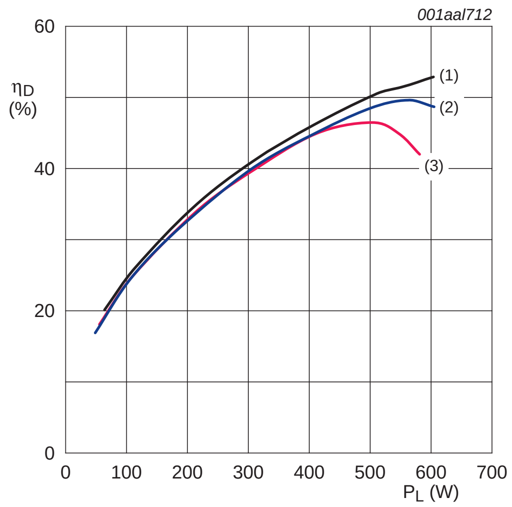
V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) T_h = –40 °C

(2) T_h = 25 °C

(3) T_h = 65°C

Fig 35. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 150 mA.

(1) T_h = −40 °C

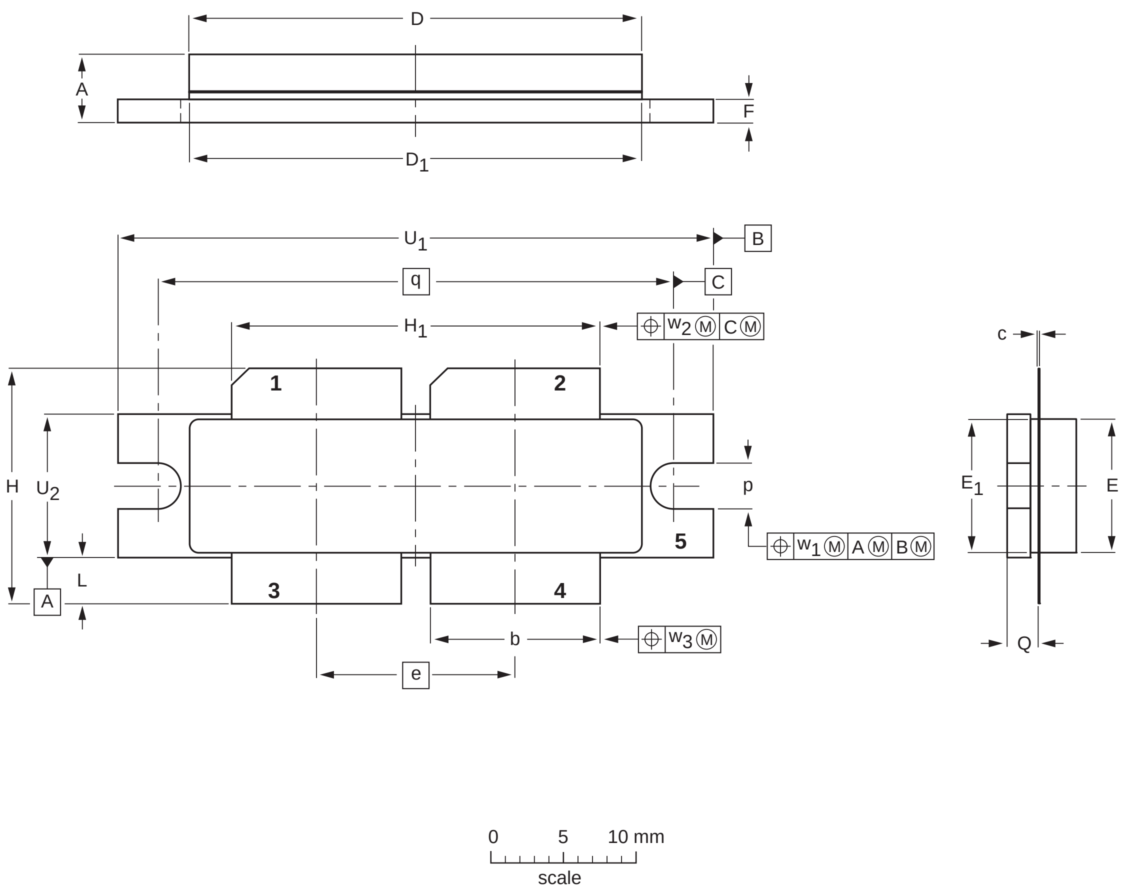
(2) T_h = 25 °C

(3) T_h = 65°C

Fig 36. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

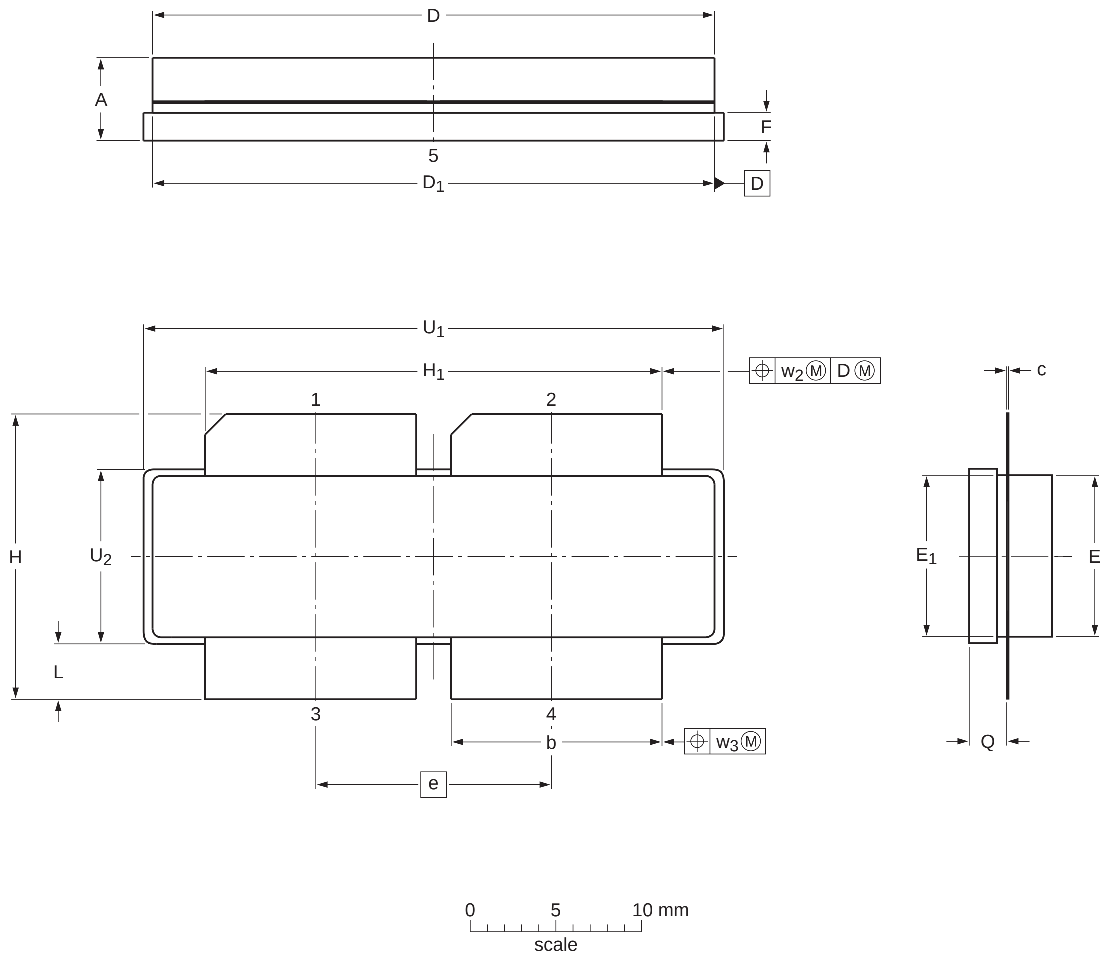
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 37. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 38. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
L-band	Long wave Band
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6H1214-500_1214LS-500 v.3	20130805	Product data sheet	-	BLL6H1214-500 v.2
Modifications:	• This document now describes both the BLL6H1214-500 and BLL6H1214LS-500 products. • Table 1 on page 1: ‘mode of operation’ changed to ‘test signal’. • Table 4 on page 2: removed row ‘I_D’. • Table 7 on page 3: ‘mode of operation’ changed to ‘test signal’. • Section 7 on page 4: moved several sections to this section. • Section 7.4 on page 6: updated figure notes. • Section 7.4.1 on page 6: updated graphs. • Section 7.4.2 on page 7: updated graphs. • Figure 38 on page 17: updated figure.			
BLL6H1214-500 v.2	20100401	Product data sheet	-	BLL6H1214-500 v.1
BLL6H1214-500 v.1	20090120	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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