



# Z86C61/62/96

## CMOS Z8 MICROCONTROLLER

### FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines
Z86C61	16	236	32
Z86C62	16	236	52
Z86C96	16	236	52

**Note:** \*General-Purpose

- 3.0V to 5.5V Operating Range
- Low Power Consumption: 200 mW (max)
- Fast Instruction Pointer: 0.75  $\mu$ s @ 16 MHz
- Two Standby Modes: STOP and HALT
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds: 16 and 20 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive

### GENERAL DESCRIPTION

The Z86C61/62/96 microcontroller is a member of the Z8 single-chip microcontroller family with 16 KB of ROM and 236 bytes of RAM. The Z86C96 is ROMless.

The Z86C61 is offered in 40-pin DIP and 44-pin PLCC style packages, however, the ROMless pin option is available on the 44-pin version only. The Z86C62/96 is offered in 64-pin DIP and 68-pin PLCC style packages. A ROMless pin option enables these MCUs to address both external memory and preprogrammed ROM, making them well-suited for high-volume applications or where code flexibility is required.

With 16 KB of ROM and 236 bytes of general-purpose RAM, these low-cost, low power consumption CMOS Z86C61/62/96 MCUs offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C61/62/96 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C61 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. The Z86C62/96 has 52 pins for input and output, and these lines are grouped into six, 8-bit ports and one 4-bit port. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this configuration: Program Memory, Data Memory, and 236 General-Purpose Registers.

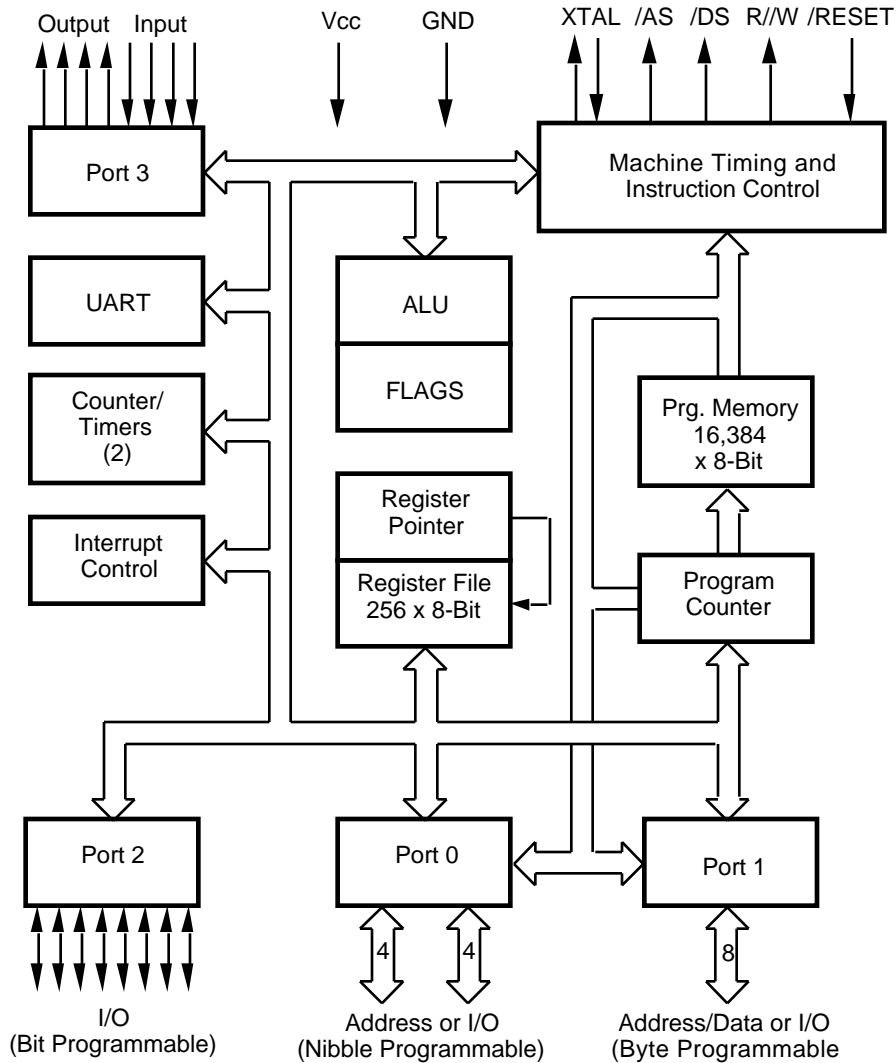
**GENERAL DESCRIPTION** (Continued)

To unburden the program from coping with the real-time tasks, such as counting/timing and serial data communication, the Z86C61/62/96 offers two on-chip counter/timers with a large number of user selectable modes, and an on-board UART (Figures 1, 2, and 3).

**Notes:** All Signals with a preceding front slash, "/", are active Low. For example B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>



**Figure 1. Z86C61 Functional Block Diagram**

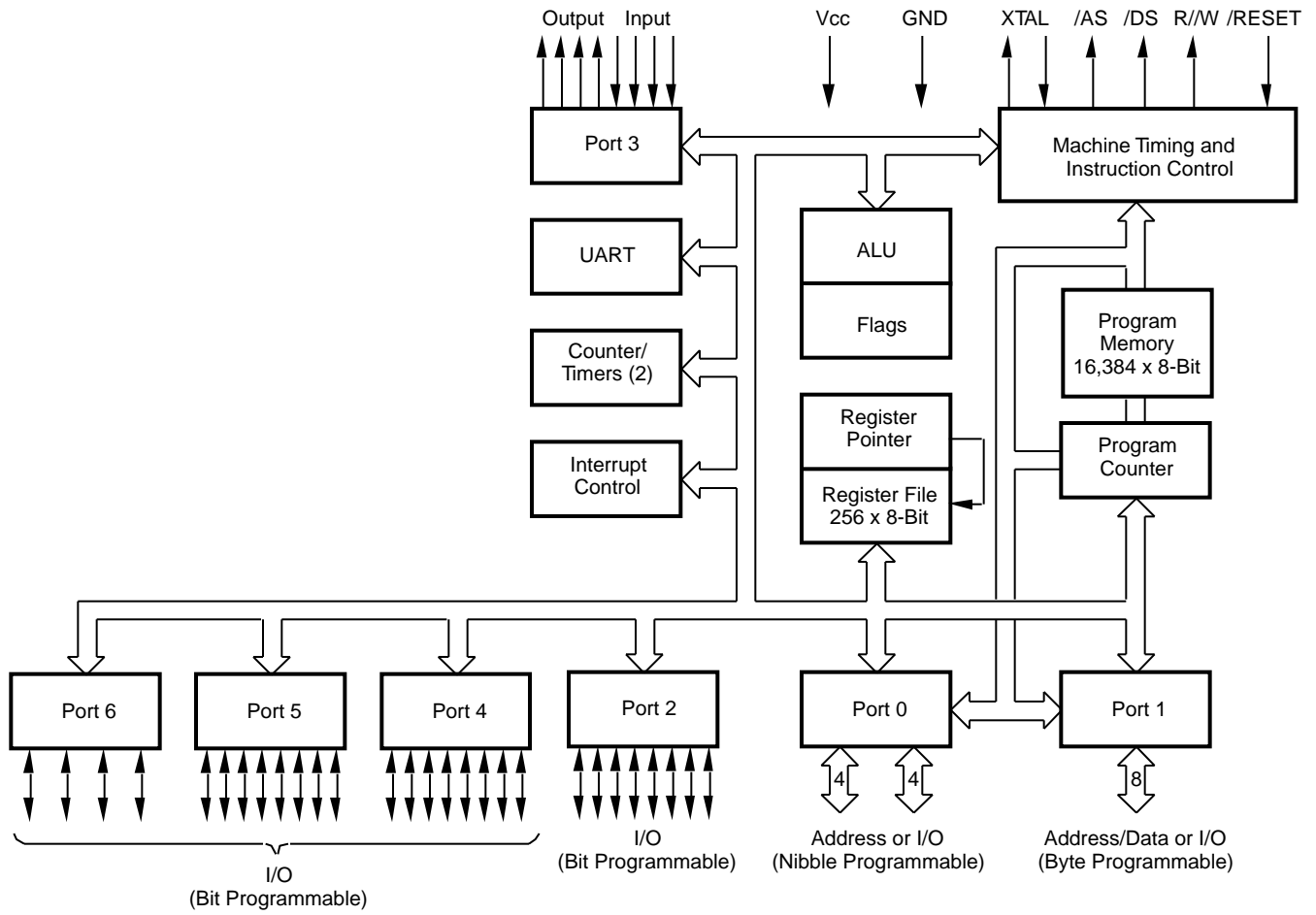


Figure 2. Z86C62 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

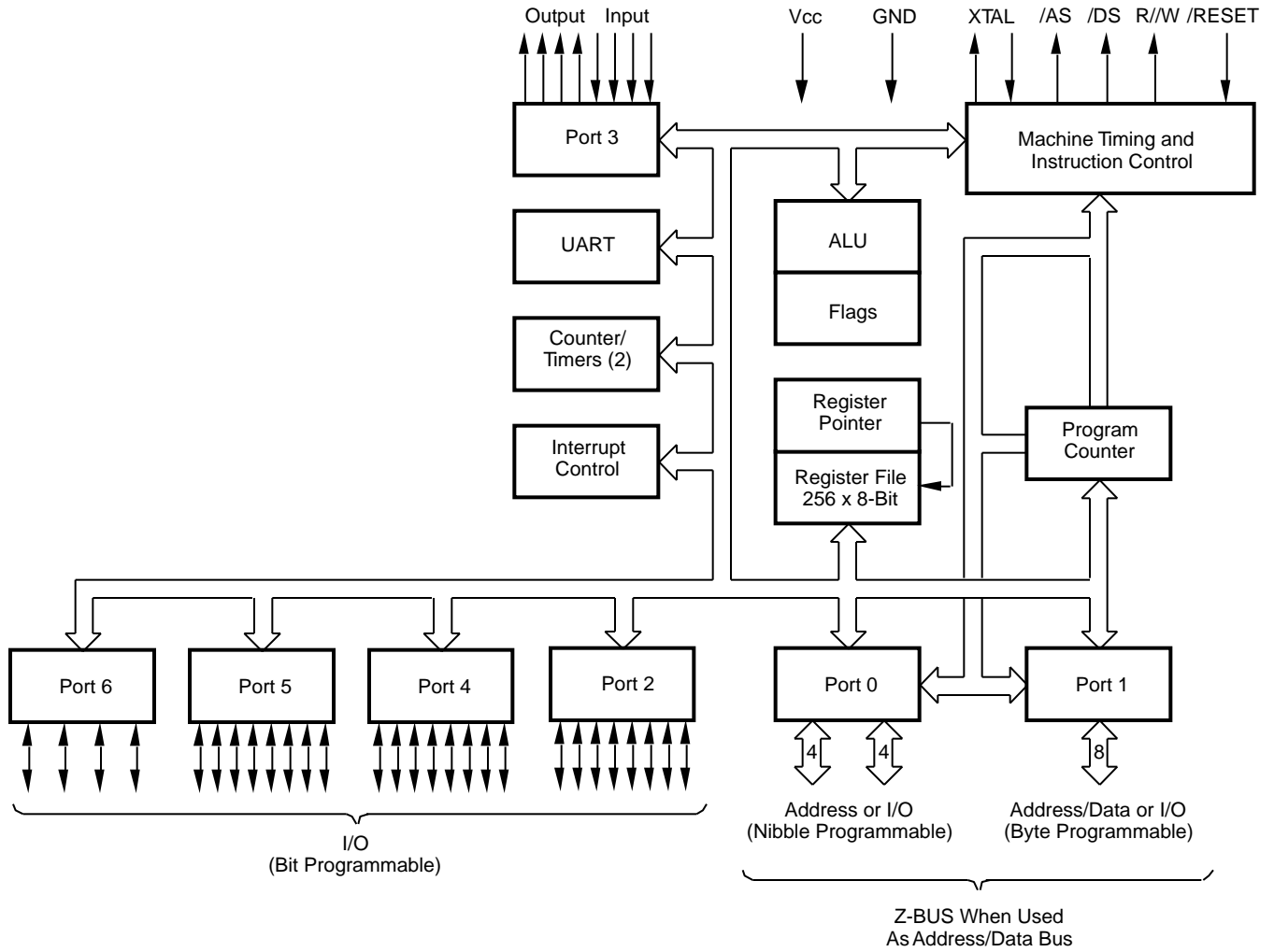


Figure 3. Z86C96 Functional Block Diagram

## PIN DESCRIPTION

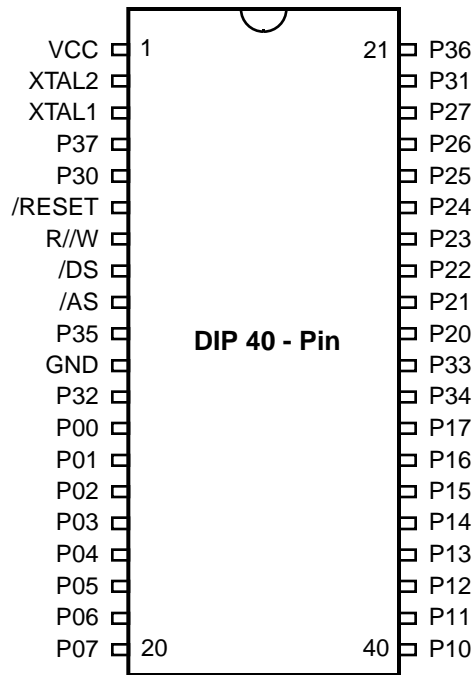
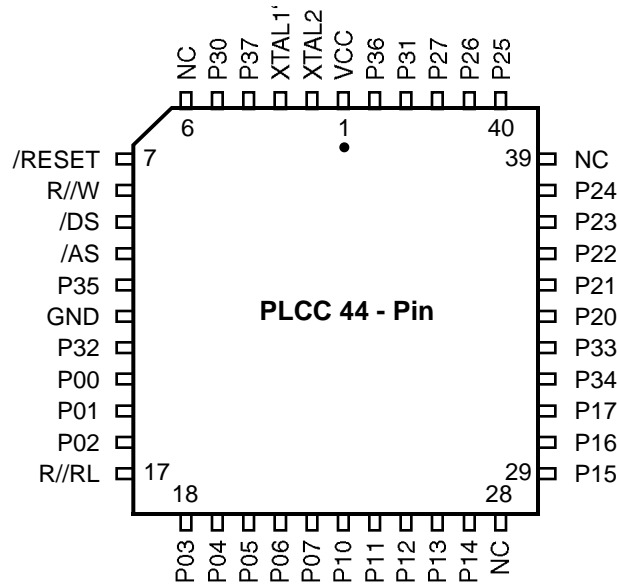


Figure 4. Z86C61 40-Pin DIP Pin Assignments

Table 1. Z86C61 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V <sub>CC</sub>	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R/W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

**PIN DESCRIPTION** (Continued)



**Figure 5. Z86C61 44-Pin PLCC Pin Assignments**

**Table 2. Z86C61 44-Pin PLCC Pin Assignments**

Pin #	Symbol	Function	Direction
1	V <sub>CC</sub>	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8	R//W	Read/Write	Output
9	/DS	Data Strobe	Output
10	/AS	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02-P00	Port 0, Pins 0,1,2	In/Output
17	R//RL	ROM/ROMless control	Input
18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output

**Table 2. Z86C61 44-Pin PLCC Pin Assignments**

Pin #	Symbol	Function	Direction
23-27	P14-P10	Port 1, Pins 0,1,2,3,4	In/Output
28	N/C	Not Connected	Input
29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
39	N/C	Not Connected	Input
40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

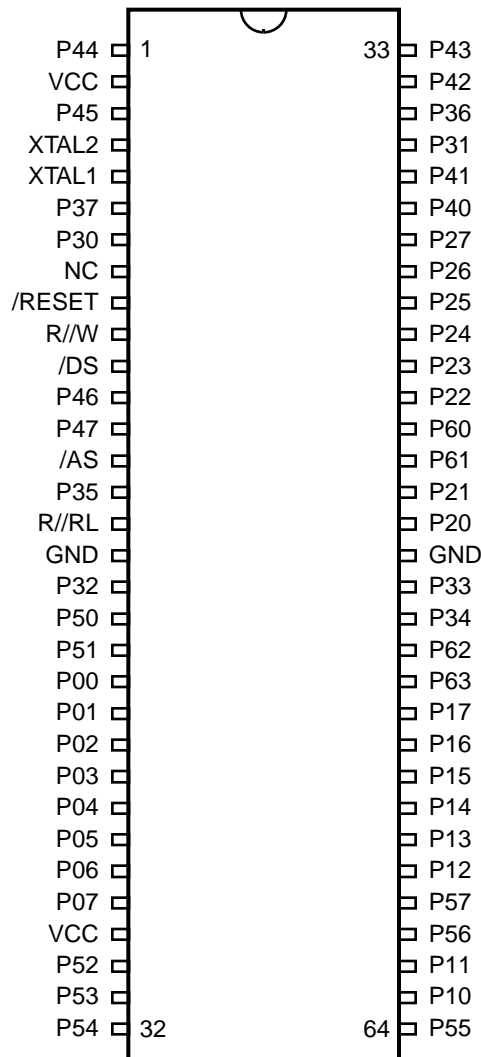
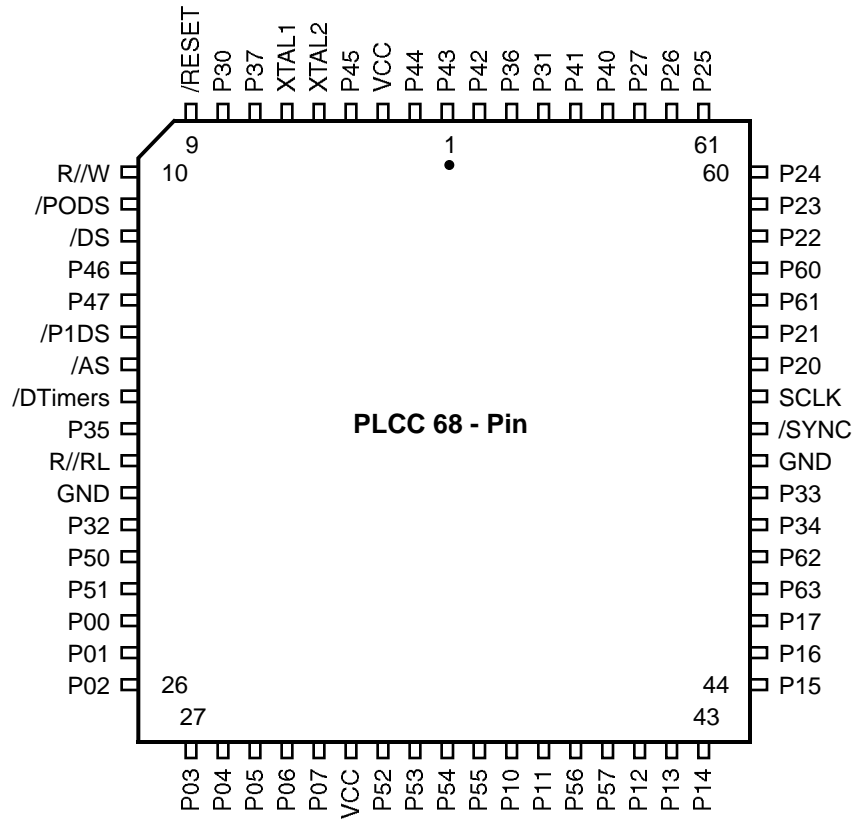


Figure 6. Z86C62/C96 64-Pin DIP Pin Assignments

Table 3. Z86C62/C96 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V <sub>CC</sub>	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R/W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	R//RL	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V <sub>CC</sub>	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

**PIN DESCRIPTION (Continued)**



**Figure 7. Z86C62/C96 68-Pin PLCC Pin Assignments**

Table 4. Z86C62/C96 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output
3	V <sub>CC</sub>	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output
6	XTAL1	Crystal, Oscillator Clock	Input
7	P37	Port 3, Pin 7	Output
8	P30	Port 3, Pin 0	Input
9	/RESET	Reset	Input
10	R/W	Read/Write	Output
11	/P0DS	Port 0 Data Strobe	Output
12	/DS	Data Strobe	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output
15	/P1DS	Port 1, Data Strobe	Output
16	/AS	Address Strobe	Output
17	/DTIMER	DTIMER	Input
18	P35	Port 3, Pin 5	Output
19	R//RL	ROM/ROMless control	Input
20	GND	Ground	Input
21	P32	Port 3, Pin 2	Input
22-23	P51-P50	Port 5, Pins 0,1	In/Output
24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
32	V <sub>CC</sub>	Power Supply	Input
33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
37-38	P11-P10	Port 1, Pins 0,1	In/Output
39-40	P56-P57	Port 5, Pins 6,7	In/Output
41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
47-48	P63-P62	Port 6, Pins 3,2	In/Output
49	P34	Port 3, Pin 4	Output
50	P33	Port 3, Pin 3	Input
51	GND	Ground	Input
52	/SYNC	Synchronization	Output
53	SCLK	System Clock	Output
54-55	P21-P20	Port 2, Pins 0,1	In/Output
56-57	P60-P61	Port 6, Pins 1,0	In/Output
58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
64-65	P41-P40	Port 4, Pins 0,1	In/Output
66	P31	Port 3, Pin 1	Input
67	P36	Port 3, Pin 6	Output
68	P42	Port 4, Pin 2	In/Output

## ABSOLUTE MAXIMUM RATINGS

Sym	Description	Min	Max	Units
$V_{CC}$	Supply Voltage*	-0.3	+7.0	V
$T_{STG}$	Storage Temp	-65	+150	C
$T_A$	Oper Ambient Temp	†	†	

**Notes:**

\*Voltages on all pins with respect to GND.

†See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 4).

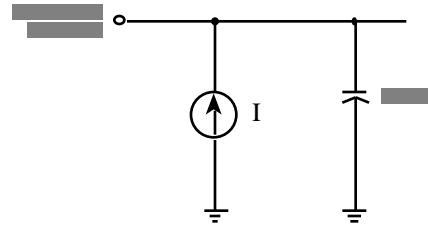


Figure 8. Test Load Diagram

## DC ELECTRICAL CHARACTERISTICS

Z86C61/62/96

Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		$T_A = -40^\circ\text{C to } +105^\circ\text{C}$		Typical @ 25°C	Units	Conditions
		Min	Max	Min	Max			
	Max Input Voltage		7		7		V	$I_{IN} < 250 \mu\text{A}$
$V_{CH}$	Clock Input High Voltage	$0.85 V_{CC}$	$V_{CC} + 0.3$	$0.85 V_{CC}$	$V_{CC} + 0.3$		V	Driven by External Clock Generator
$V_{CL}$	Clock Input Low Voltage	$V_{SS} - 0.3$	0.8	$V_{SS} - 0.3$	0.8		V	Driven by External Clock Generator
$V_{IH}$	Input High Voltage	2	$V_{CC} + 0.3$	2	$V_{CC} + 0.3$		V	
$V_{IL}$	Input Low Voltage	$V_{SS} - 0.3$	$0.2 V_{CC}$	$V_{SS} - 0.3$	$0.2 V_{CC}$		V	
$V_{OH}$	Output High Voltage	2.4		2.4			V	$I_{OH} = -2.0 \text{ mA}$
$V_{OH}$	Output High Voltage		$V_{CC} - 100 \text{ mV}$		$V_{CC} - 100 \text{ mV}$		V	$I_{OH} = -100 \mu\text{A}$
$V_{OL}$	Output Low Voltage		0.4		0.4		V	$I_{OL} = +5.0 \text{ mA}$ [3]
$V_{OL}$	Output Low Voltage		0.6		0.6		V	$I_{OL} = +4.0 \text{ mA}$ [2]
$V_{RH}$	Reset Input High Voltage	$0.85 V_{CC}$	$V_{CC} + 0.3$	$0.85 V_{CC}$	$V_{CC} + 0.3$		V	
$V_{RI}$	Reset Input Low Voltage	-0.3	$0.2 V_{CC}$	-0.3	$0.2 V_{CC}$		V	
$I_{IL}$	Input Leakage	-2	2	-2	2		$\mu\text{A}$	$V_{IN} = 0\text{V}, V_{CC}$
$I_{OL}$	Output Leakage	-2	2	-2	2		$\mu\text{A}$	$V_{IN} = 0\text{V}, V_{CC}$
$I_{IR}$	Reset Input Current		-80		-80		$\mu\text{A}$	$V_{RL} = 0\text{V}$
$I_{CC}$	Supply Current		35		35	24	mA	[1] @ 16 MHz
$I_{CC}$	Supply Current		40		40	30	mA	[1] @ 20 MHz
$I_{CC1}$	Standby Current		15		15	4.5	mA	[1] HALT Mode $V_{IN} = 0\text{V}, V_{CC}$ @ 16 MHz
$I_{CC2}$	Standby Current		10		20	5	$\mu\text{A}$	[1] STOP Mode $V_{IN} = 0\text{V}, V_{CC}$

## Notes:

1. All inputs driven to either 0V or  $V_{CC}$ , outputs floating.
2.  $V_{CC} = 3.0\text{V to } 3.6\text{V}$
3.  $V_{CC} = 4.5\text{V to } 5.5\text{V}$

DC ELECTRICAL CHARACTERISTICS (Continued)

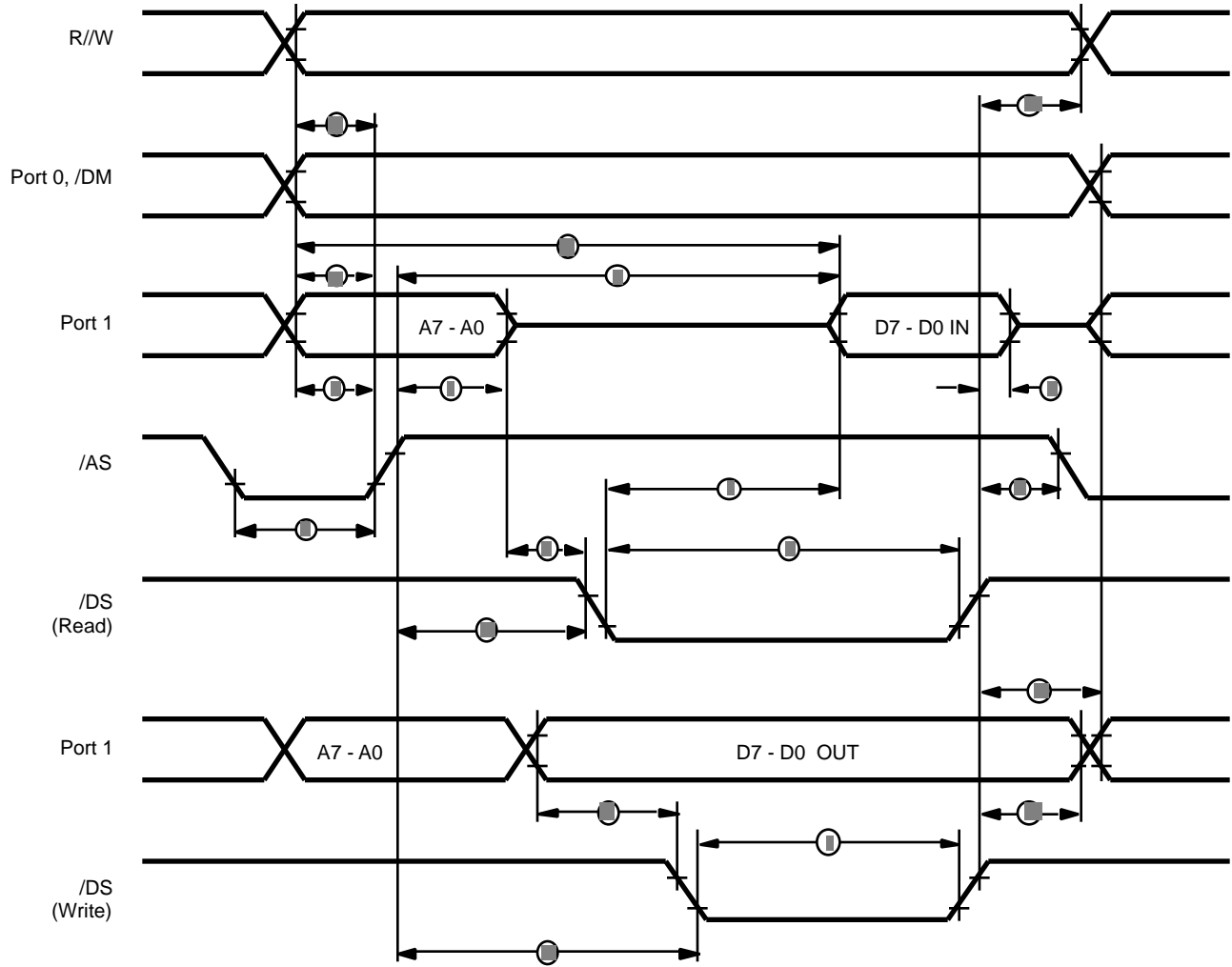


Figure 9. External I/O or Memory Read/Write

**AC CHARACTERISTICS**External I/O or Memory Read and Write Timing  
Z86C61/62/96 (16 MHz)

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		$T_A = -40^\circ\text{C to } +105^\circ\text{C}$		Units	Notes
			16 MHz		16 MHz			
			Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	2,3
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	2,3
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	1,2,3
4	TwAS	/AS Low Width	40		40		ns	2,3
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	1,2,3
7	TwDSW	/DS (Write) Low Width	80		80		ns	1,2,3
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	1,2,3
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	2,3
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	2,3
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	2,3
12	TdR/W(AS)	R/W Valid to /AS rise Delay	25		25		ns	2,3
13	TdDS(R/W)	/DS rise to R/W Not Valid	35		35		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	2,3
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	1,2,3
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	2,3
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	2,3

**Notes:**

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.

**Standard Test Load**

All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

**Table 5. Clock Dependent Formulas**

Number	Symbol	Equation
1	TdA(AS)	$0.40 \text{ TpC} + 0.32$
2	TdAS(A)	$0.59 \text{ TpC} - 3.25$
3	TdAS(DR)	$2.83 \text{ TpC} + 6.14$
4	TwAS	$0.66 \text{ TpC} - 1.65$
6	TwDSR	$2.33 \text{ TpC} - 10.56$
7	TwDSW	$1.27 \text{ TpC} + 1.67$

**Table 5. Clock Dependent Formulas**

Number	Symbol	Equation
8	TdDSR(DR)	$1.97 \text{ TpC} - 42.5$
10	TdDS(A)	$0.8 \text{ TpC}$
11	TdDS(AS)	$0.59 \text{ TpC} - 3.14$
12	TdR/W(AS)	$0.4 \text{ TpC}$
13	TdDS(R/W)	$0.8 \text{ TpC} - 15$
14	TdDW(DSW)	$0.4 \text{ TpC}$
15	TdDS(DW)	$0.88 \text{ TpC} - 19$
16	TdA(DR)	$4 \text{ TpC} - 20$
17	TdAS(DS)	$0.91 \text{ TpC} - 10.7$
18	TdDM(AS)	$0.9 \text{ TpC} - 26.3$

## AC CHARACTERISTICS

External I/O or Memory Read and Write Timing  
Z86C61/62/96 (20 MHz)

No	Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		$T_A = -40^\circ\text{C to } +105^\circ\text{C}$		Units	Notes
			20 MHz		20 MHz			
			Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	2,3
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	2,3
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	1,2,3
4	TwAS	/AS Low Width	30		30		ns	2,3
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	1,2,3
7	TwDSW	/DS (Write) Low Width	65		65		ns	1,2,3
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	1,2,3
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	2,3
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	2,3
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	2,3
12	TdR/W(AS)	R/W Valid to /AS rise Delay	20		20		ns	2,3
13	TdDS(R/W)	/DS rise to R/W Not Valid	25		25		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	2,3
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	1,2,3
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	2,3
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	2,3

**Notes:**

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.

**AC CHARACTERISTICS**  
Additional Timing Diagram

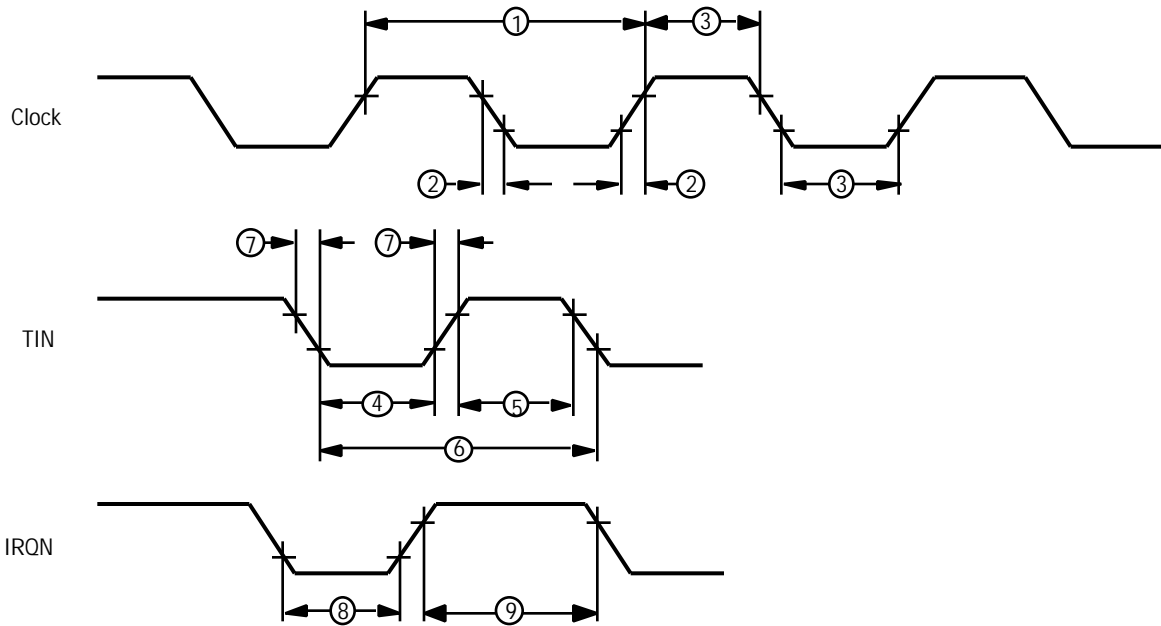


Figure 10. Additional Timing

## AC CHARACTERISTICS

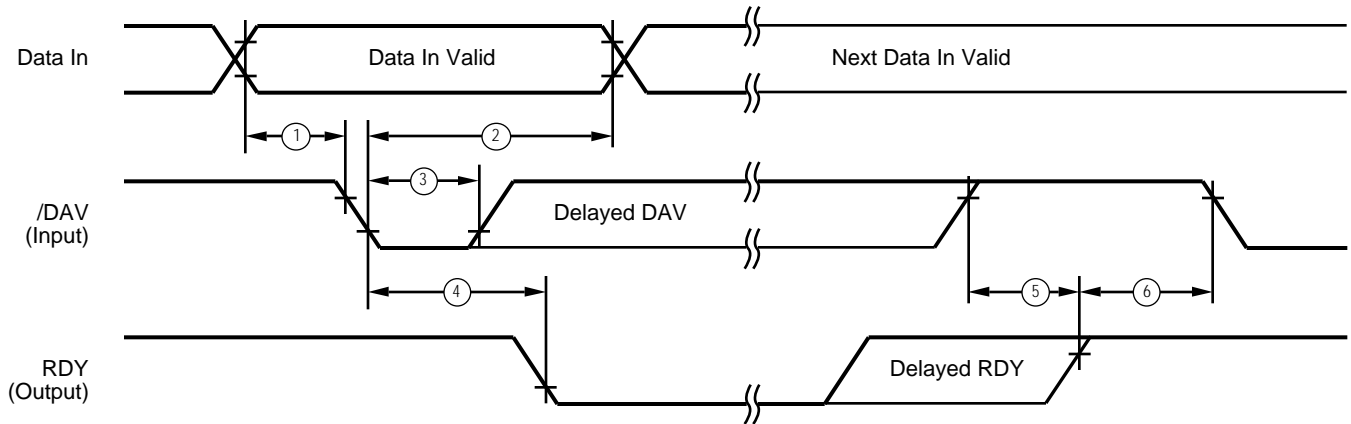
### Additional Timing Table Z86C61/62/96

No	Symbol	Parameter	$T_A = 0^\circ\text{C to }+70^\circ\text{C}$		$T_A = -40^\circ\text{C to }+105^\circ\text{C}$		Units	Notes
			20/16 MHz		20/16 MHz			
			Min	Max	Min	Max		
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10	10		ns	1
3	TwC	Input Clock Width	25		25		ns	1
4	TwTinL	Timer Input Low Width	75		75		ns	2
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	2
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	2
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	2
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	2,4
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	2,5
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	2,3

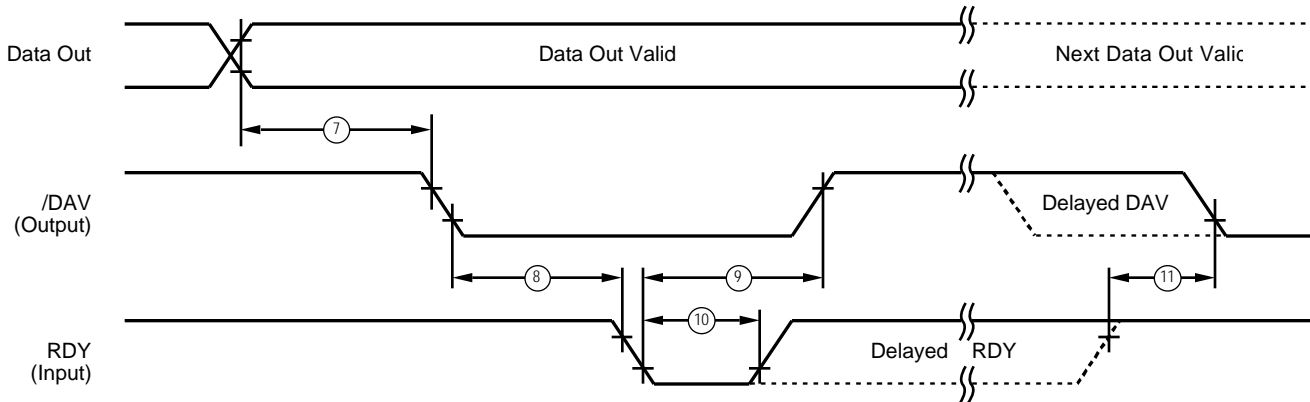
**Notes:**

1. Clock timing references use  $0.8V_{CC}$  for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request through Port 3.
4. Interrupt request through Port 3 (P33-P31).
5. Interrupt request through Port 30.

**AC CHARACTERISTICS**  
Handshake Timing Diagrams



**Figure 11. Input Handshake Timing**



**Figure 12. Output Handshake Timing**

## AC CHARACTERISTICS

### Handshake Timing Table Z86C61/62/96

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		$T_A = -40^\circ\text{C to } +105^\circ\text{C}$		Data Direction
			20/16 MHz		20/16 MHz		
			Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV fall to RDY fall Delay	115		115		IN
5	TdDAVId(RDY)	DAV rise to RDY rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY rise to DAV fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV fall to RDY fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY fall to DAV rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY rise to DAV fall Delay	115		115		OUT

## PIN FUNCTIONS

**R//RL** (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C96 ROMless Z8. (Note: When left unconnected or pulled High to VCC the part functions as a normal Z86C61/62 ROM version.) This pin is only available on the 44-pin version of the Z86C61, and both versions of the Z86C62.

**/DS** (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

**/AS** (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address out-put is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

**XTAL1, XTAL2** Crystal 1, Crystal 2 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

**R//W** (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

**/RESET** (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C61/62/96 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time must be held Low for 50 ms, or until VCC is stable, whichever is longer.

**/P0DS** Port 0 Data Strobe (output, active Low). Signal used to emulate Port 0 when in ROMless mode.

**/P1DS** Port 1 Data Strobe (output, active Low). Signal used to emulate Port 1 when in ROMless mode.

**/DTIMERS** Disable Timers (input, active Low). All timers are stopped by the Low level at this pin. This pin has an internal pull up resistor.

**SCLK** (output). System clock pin.

**/SYNC** Instruction SYNC Signal (output, active Low). This signal indicates the last clock of the current executing instruction.

**Port 0 (P07-P00)**. Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 14).

PIN FUNCTIONS (Continued)

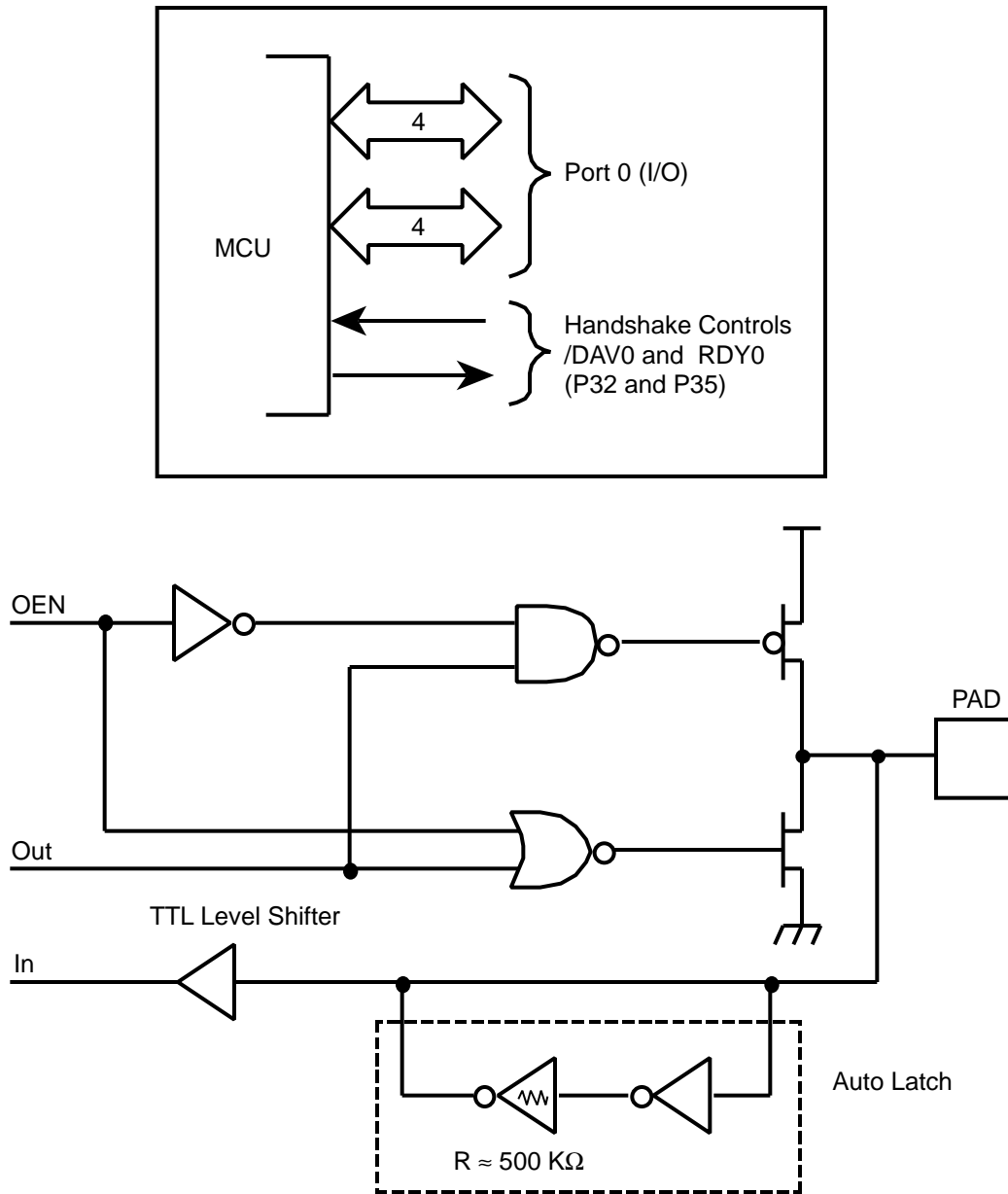


Figure 13. Port 0 Configuration

**Port 1 (P17-P10).** Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C61/62/96, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control. In this configuration, Port 3 line P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 16,384 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the microcontroller to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 14).

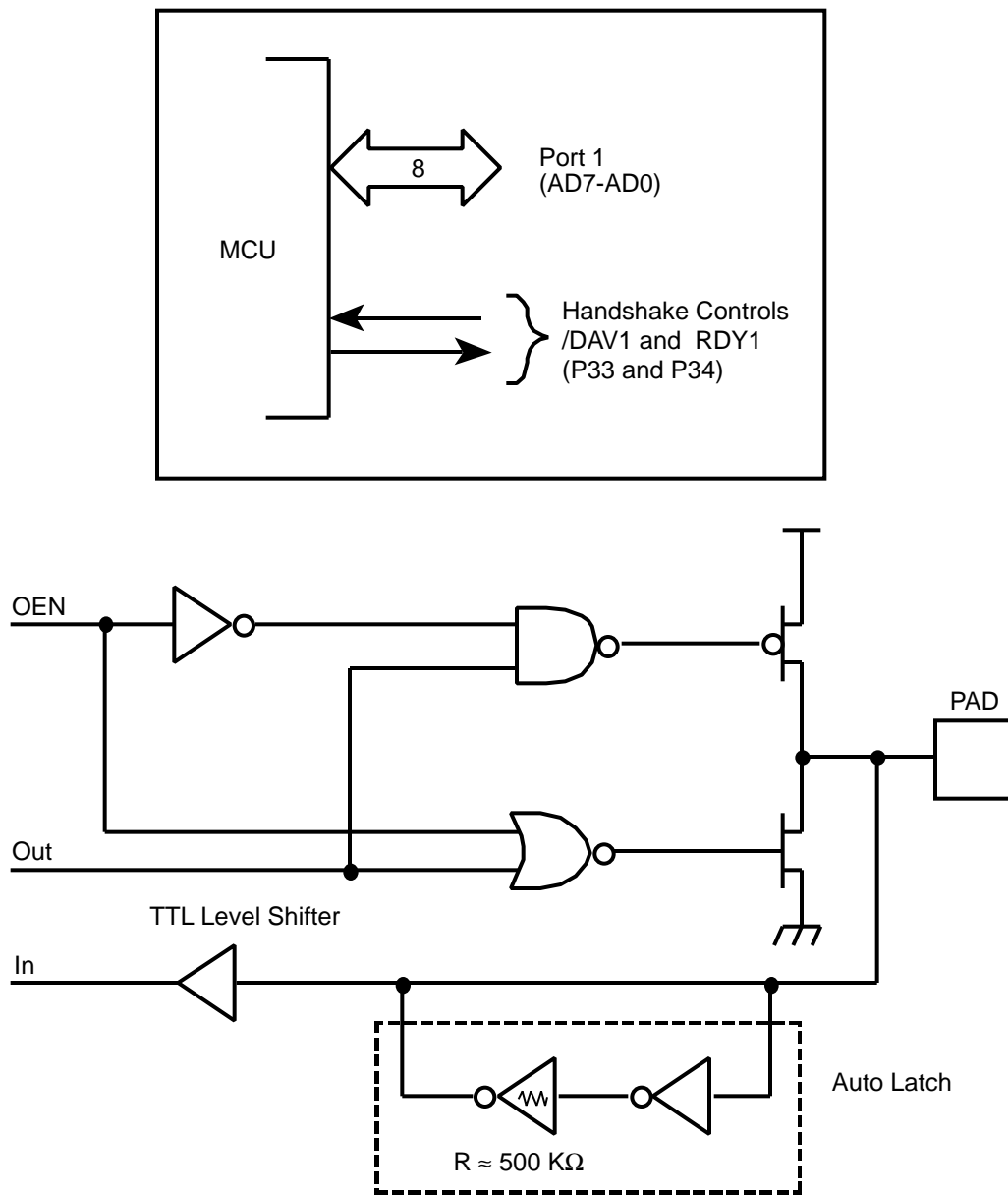


Figure 14. Port 1 Configuration

**PIN FUNCTIONS** (Continued)

**Port 2** (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port

2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 15).

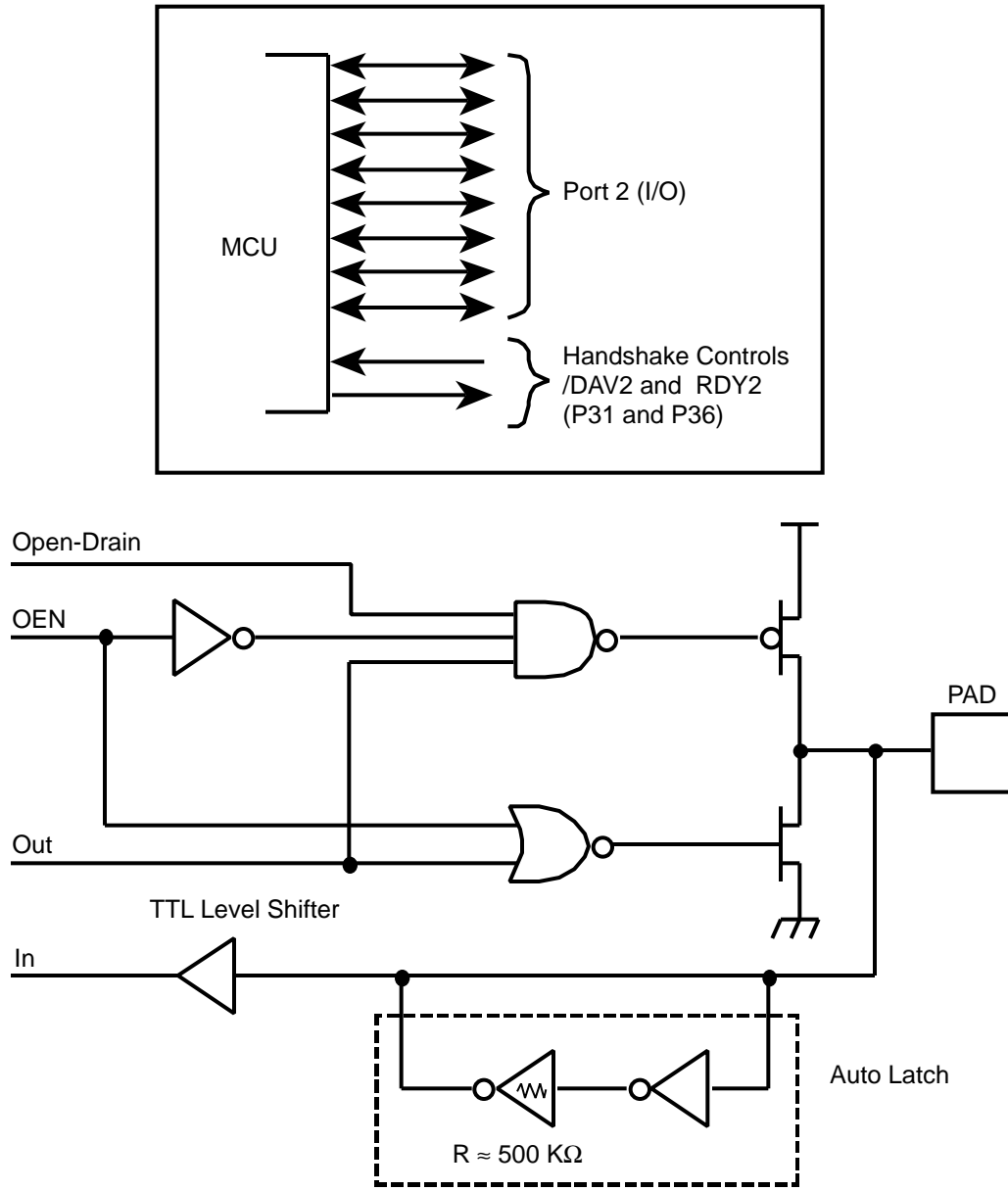


Figure 15. Port 2 Configuration

**Port 3** (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-

P34) output ports. Port 3, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 16).

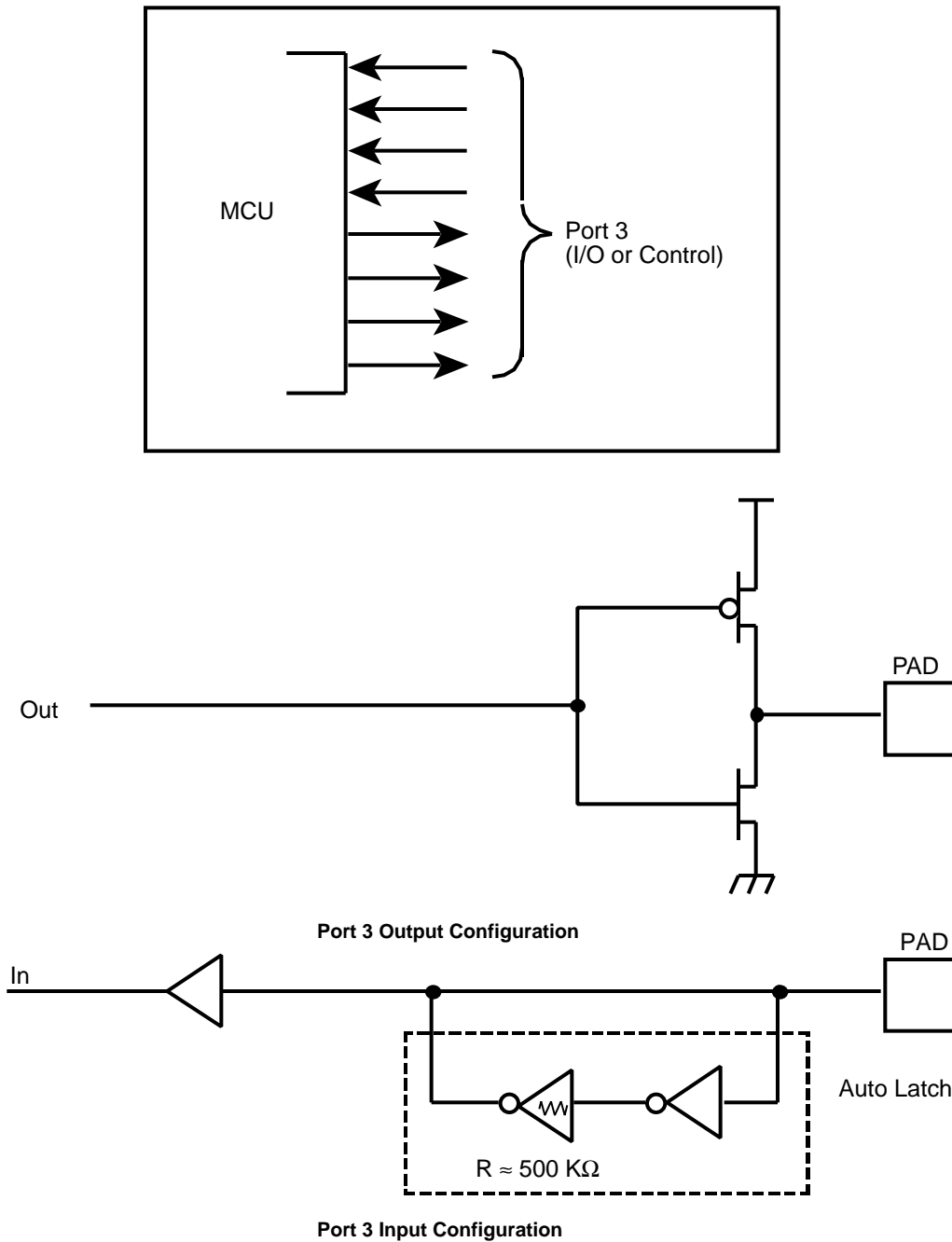


Figure 16. Port 3 Configuration

## PIN FUNCTIONS (Continued)

Port 3 can be configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals

(IRQ3-IRQ0); timer input and output signals ( $T_{IN}$  and  $T_{OUT}$ ), and Data Memory Select (/DM).

**Table 6. Port 3 Pin Assignments**

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	$T_{IN}$	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	$T_{OUT}$				R/D		
P37	OUT						Serial Out	
T0			IRQ4					
T1			IRQ5					

**Notes:**

HS = Handshake Signals

D = Data Available

R = Ready

### Uart Operation

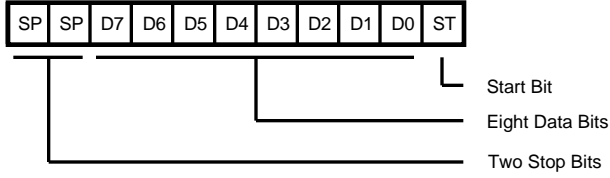
Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C61/62/96 automatically adds a start bit and two stop bits to transmitted data (Figure 17). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

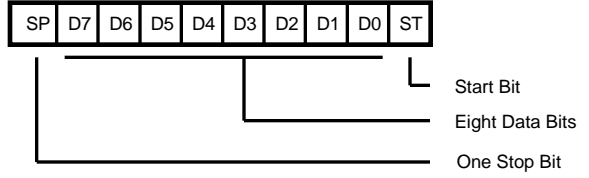
Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

**Note:** UART function is only available in standard timing mode (i.e., P01M D5 = 0).

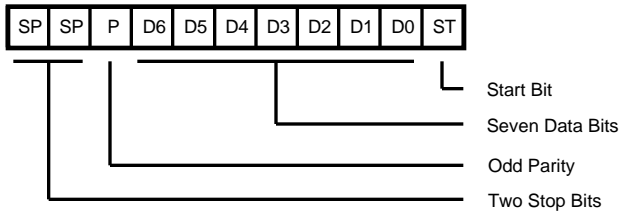
Transmitted Data (No Parity)



Received Data (No Parity)



Transmitted Data (With Parity)



Received Data (With Parity)

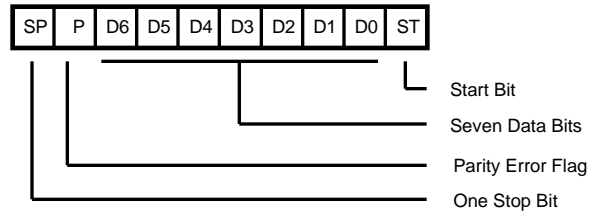


Figure 17. Serial Data Formats

**PIN FUNCTIONS** (Continued)

**Port 4** (P47-P40). Port 4 is an 8-bit, bit programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 4 is always available for I/O operation (Figure 18). Port address (F)02.

**Port 5** (P57-P50). Same as Port 4. Port address (F)04.

**Port 6** (P63-P60). Same as Port 4. (Note: this is a 4-bit port, bits D3-D0.) Port address (F)07.

**Auto Latch.** The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

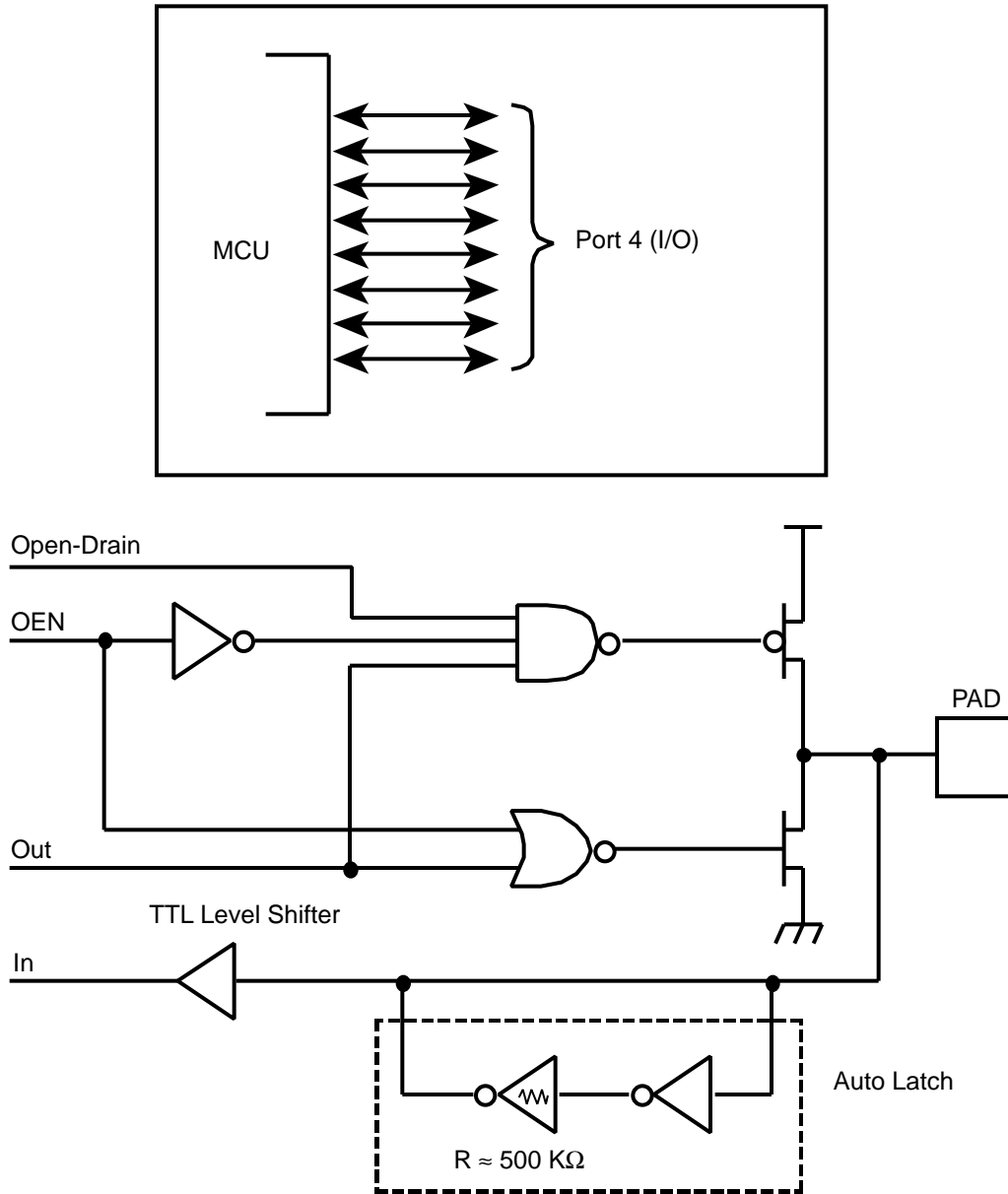


Figure 18. Port 4 Configuration

## FUNCTIONAL DESCRIPTION

### Address Space

**Program Memory.** The Z86C61/62 can address up to 48 KB of external program memory (Figure 19). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 16383 consists of on-chip ROM. At addresses 16384 and greater, the Z86C61/62 executes external program memory fetches. The Z86C96, and the Z86C61/62 in ROMless mode, can address up to 64 KB of external program memory. Program execution begins at external location 000CH after a reset.

**Data Memory (/DM).** The ROM version can address up to 48 KB of external data memory space beginning at location 16384. The ROMless version can address up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 20). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

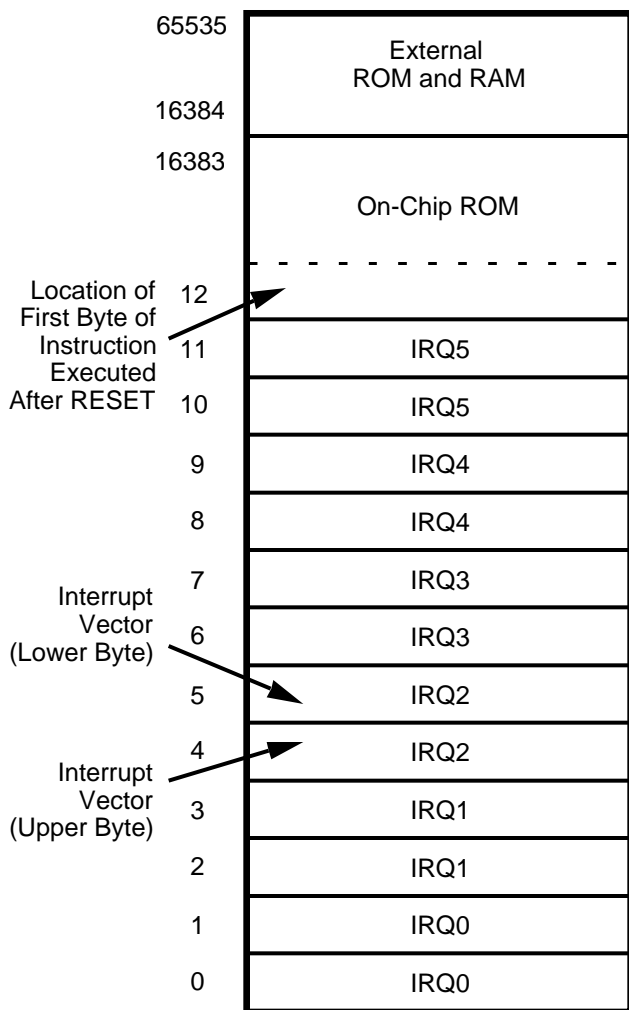


Figure 19. Program Memory Configuration

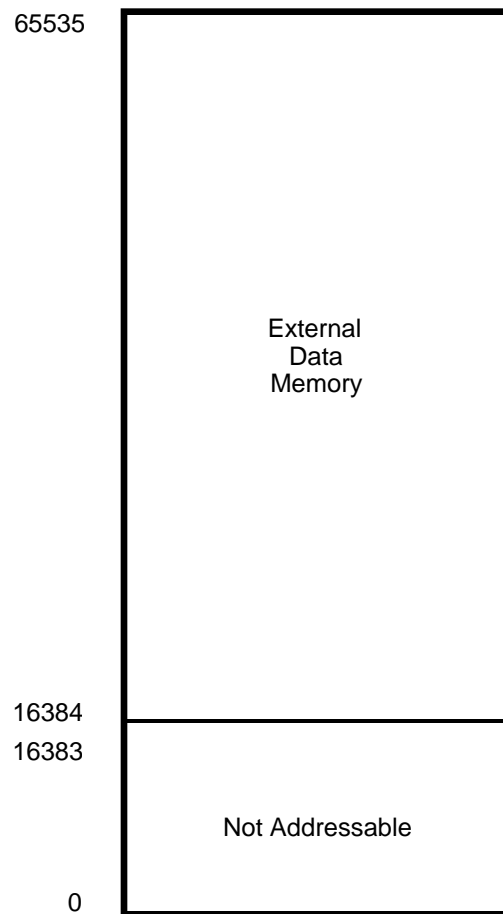


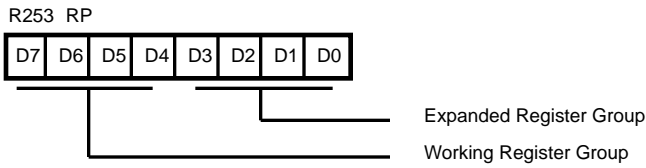
Figure 20. Data Memory Configuration

**FUNCTIONAL DESCRIPTION (Continued)**

**Register File.** The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 18). There are eight further registers for I/O ports 4, 5 and 6 in the Expanded Register File (Bank F, R9-R2) (Figure 20).

The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C61/62/96 also allows short 4-bit register addressing using the Register Pointer (Figure 21). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

**Note:** Register Bank E0-EF can only be accessed through working registers and indirect addressing modes.



Default Setting After Reset = 00000000

**Figure 21. Register Pointer Register**

Location		Identifiers
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239	General-Purpose Registers	
R4		
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

**Figure 22. Register File**

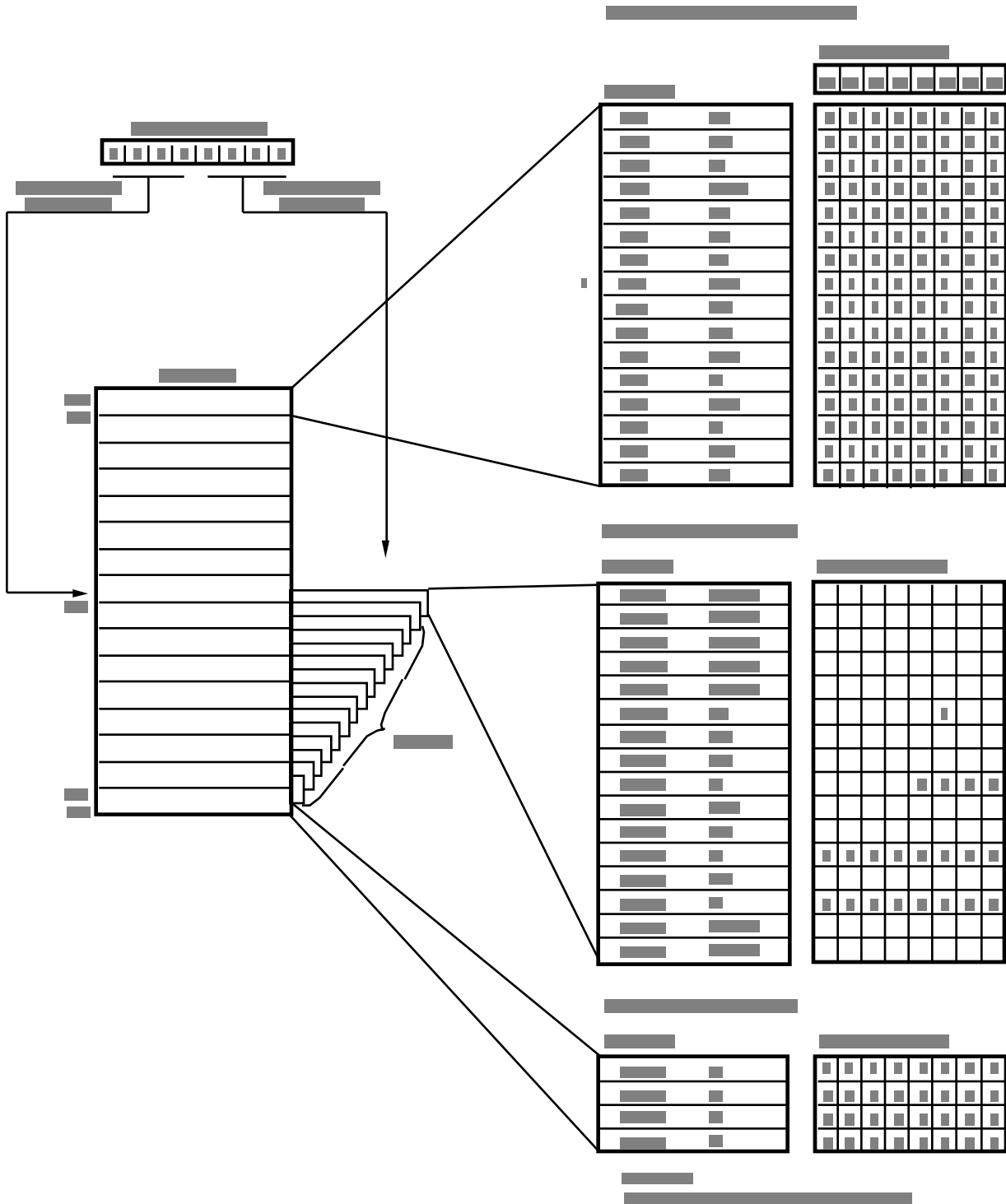


Figure 23. Expanded Register File Architecture

## FUNCTIONAL DESCRIPTION (Continued)

**Expanded Register File.** The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of Register RP select the working register group. Bits 3-0 of Register RP select the expanded register group (Figure 21). Eight I/O port registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

The upper nibble of the register pointer (Figure 20) selects which group of 16 bytes in the register file, out of the full 236, will be accessed. The lower nibble selects the expanded register file bank and in the case of the Z86C61/62/96, only Bank F is implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86C61: (See Figures 21 and 22)

R253 RP = 00H	R0 = Port 0	R2 = Port 2
	R1 = Port 1	R3 = Port 3

But If:

R253 RP = 0FH	R0 = Reserved
	R1 = Reserved
	R2 = Port 4
	R3 = Port 4, Direction Register
	R9 = Port 6, Mode Register

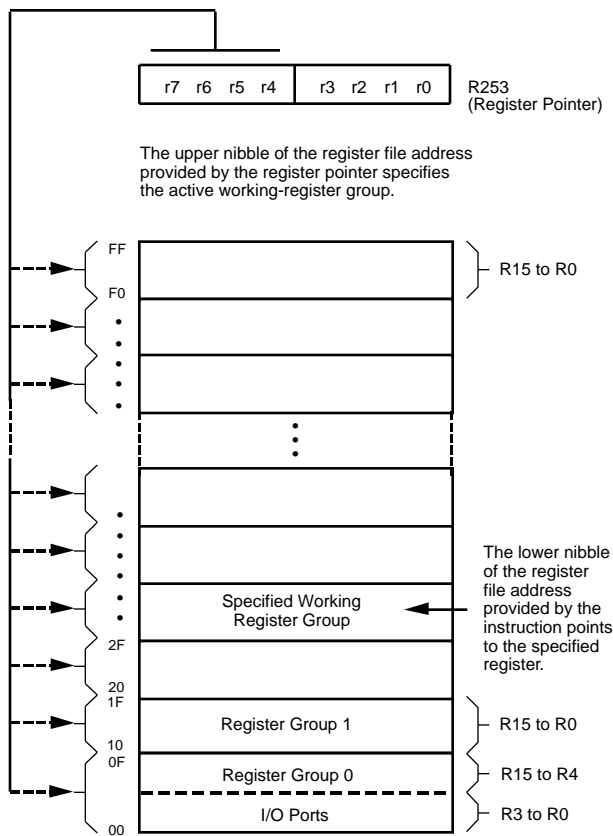
Further examples:

SRP #0FH	Set working group 0 and Bank F
LD R2, #10010110	Load value into Port 4 using working register addressing.
LD 2, #10010110	Load value into Port 4 using absolute addressing.
LD 9, #11110000	Load value into Port 6 mode.
SRP #1FH	Set working group 1 and Bank F
LD R2, #11010110	Load value into general purpose register 12H
LD 12H, #11010110	Load value into general purpose register 12H
LD 2, #10010110	Load value into Port 4

**RAM Protect.** The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

**ROM Protect.** The first 16 Kbytes of program memory is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions by external program memory when pointing to internal memory locations. Therefore these instructions can be used only when they are executed from internal memory, or if they are executed from external memory and pointing to external memory locations.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.



**Figure 24. Register Pointer**

**Stack.** The Z86C61/62/96 has a 16-bit Stack Pointer (R255-R254) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 16384 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH-Bit 8-15) can be used as a general purpose register when using internal stack only.

**Counter/Timers.** There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 22).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output (TOUT) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

FUNCTIONAL DESCRIPTION (Continued)

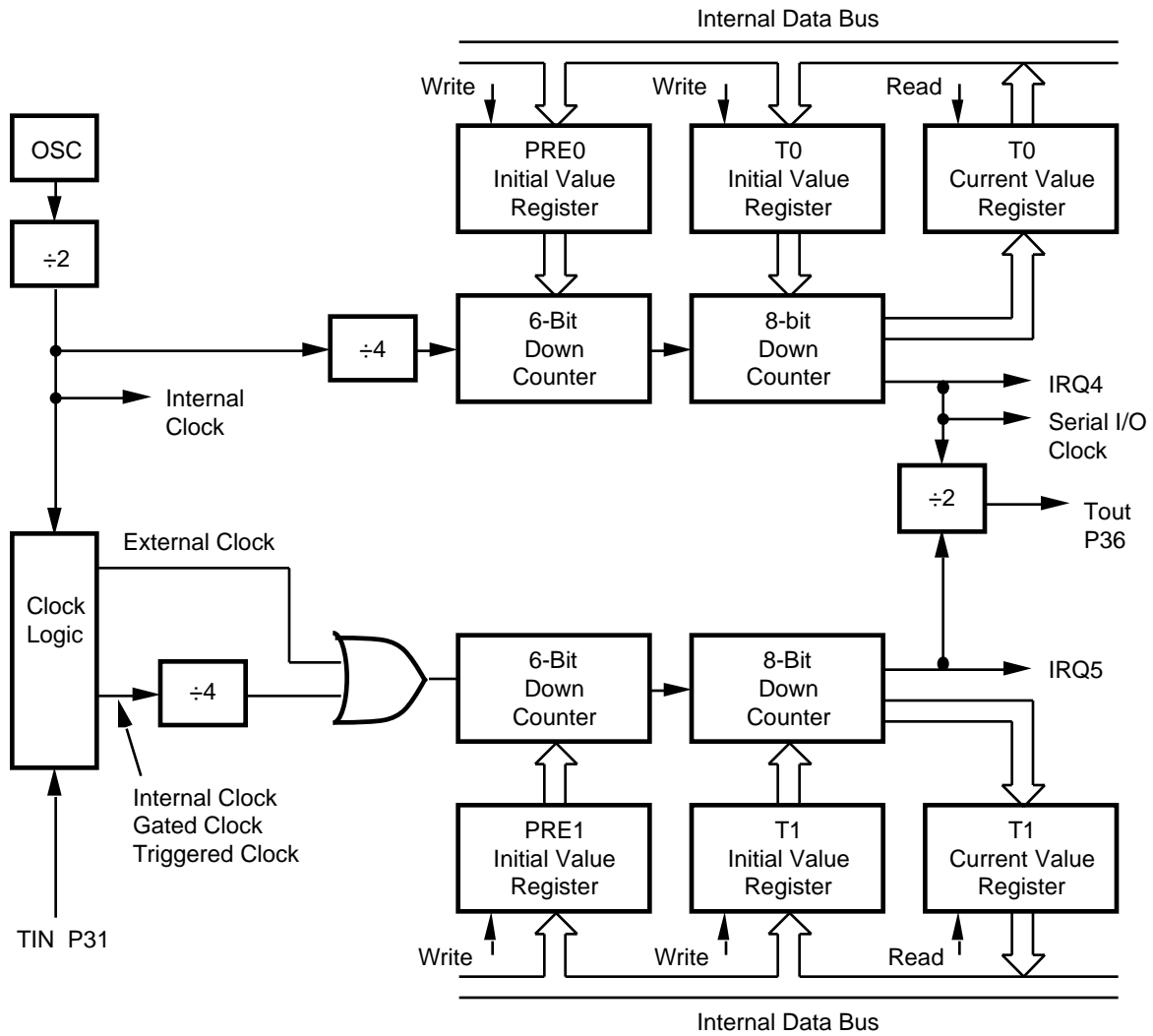


Figure 25. Counter/Timer Block Diagram

**Interrupts.** The Z86C61/62/96 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one is Serial In, and two in the counter/timers (Figure 26). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C61/62/96 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register onto the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

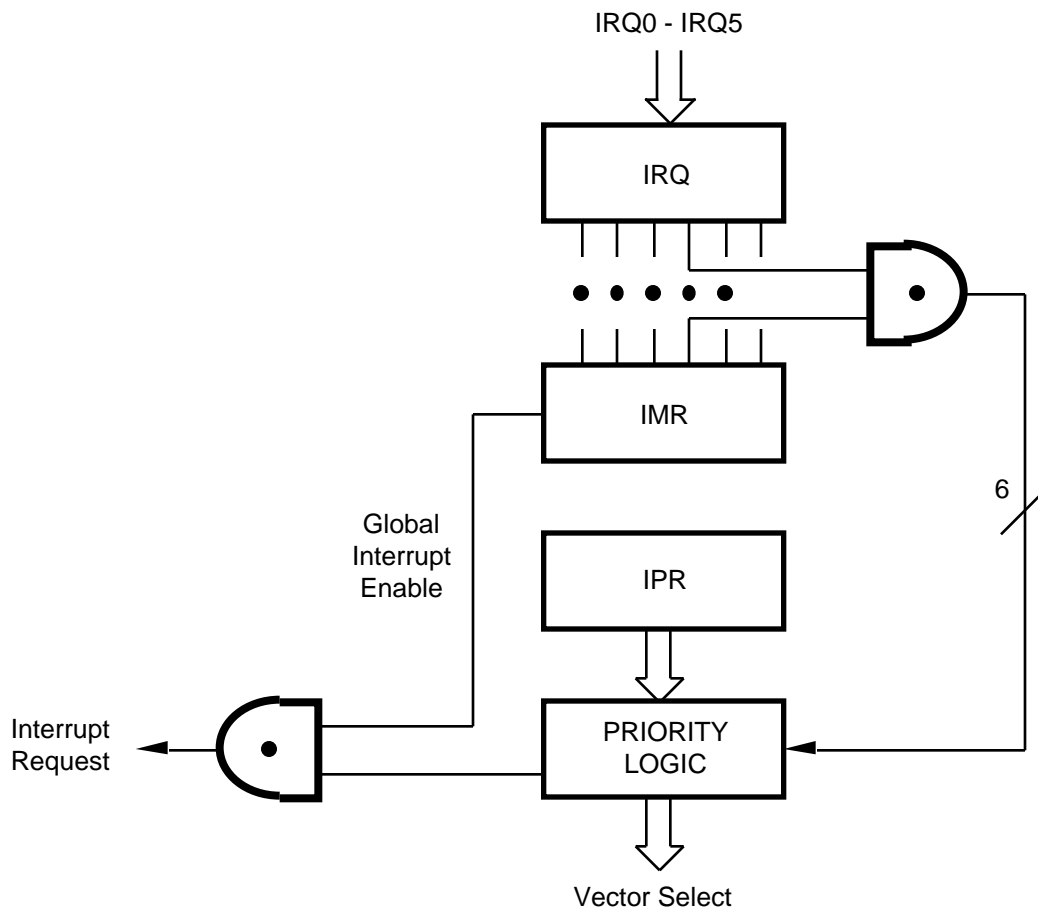


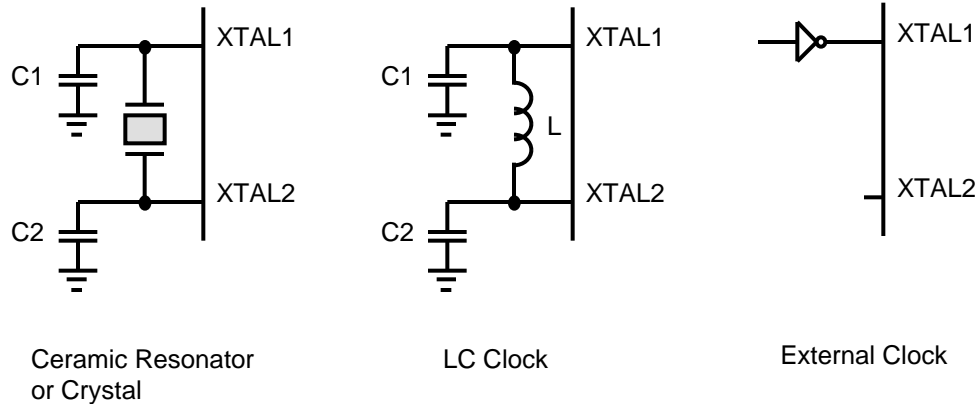
Figure 26. Interrupt Block Diagram

**FUNCTIONAL DESCRIPTION** (Continued)

**Clock.** The Z86C61/62/96 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal

should be connected across XTAL1 and XTAL2 using the recommended capacitors ( $10\text{ pF} < CL < 100\text{ pF}$ ) from each pin to device ground (Figure 27).

**Note:** Actual capacitor values specified by the crystal manufacturer.



**Figure 27. Oscillator Configuration**

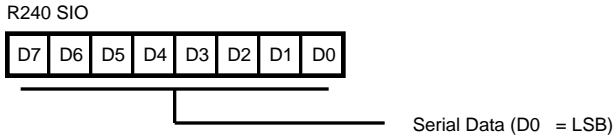
**HALT.** Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

**STOP.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5  $\mu\text{A}$  (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000CH.

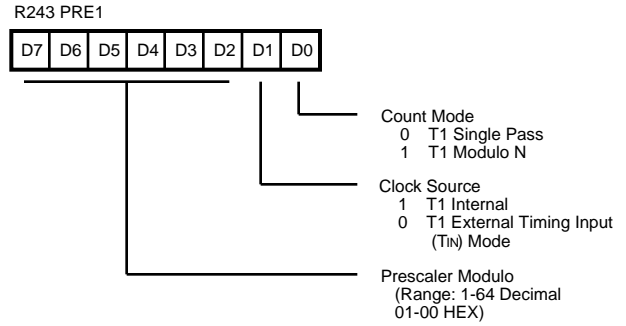
In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.,

FF	NOP	; clear the pipeline
6F	STOP	; enter STOP mode
		or
FF	NOP	; clear the pipeline
7F	HALT	; enter HALT mode

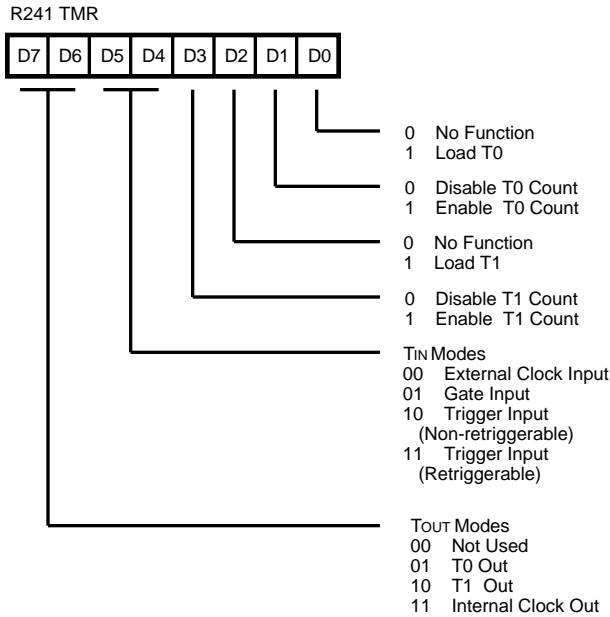
Z8 CONTROL REGISTER DIAGRAMS



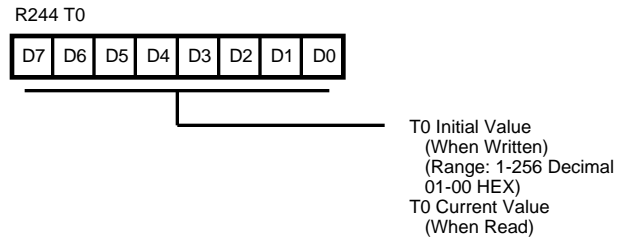
**Figure 28. Serial I/O Register (F0H: Read/Write)**



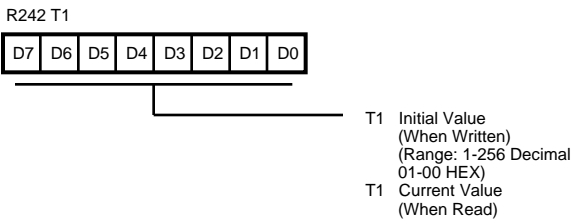
**Figure 31. Prescaler 1 Register (F3H: Write Only)**



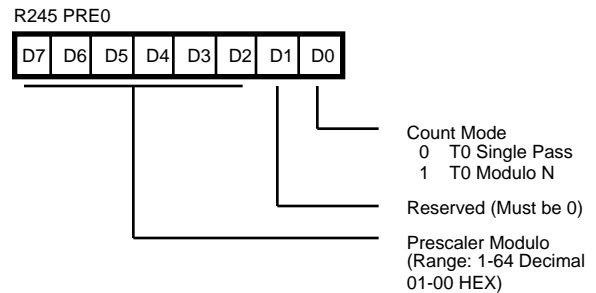
**Figure 29. Timer Mode Register (F1H: Read/Write)**



**Figure 32. Counter/Timer 0 Register (F4H: Read/Write)**



**Figure 30. Counter/Timer1 Register (F2H: Read/Write)**



**Figure 33. Prescaler 0 Register (F5H: Write Only)**

Z8 CONTROL REGISTER DIAGRAMS (Continued)

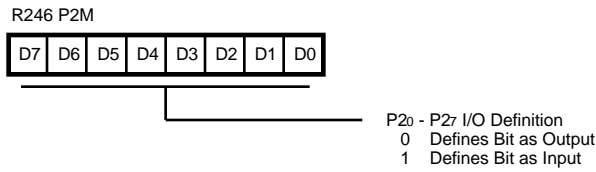


Figure 34. Port 2 Mode Register (F6H: Write Only)

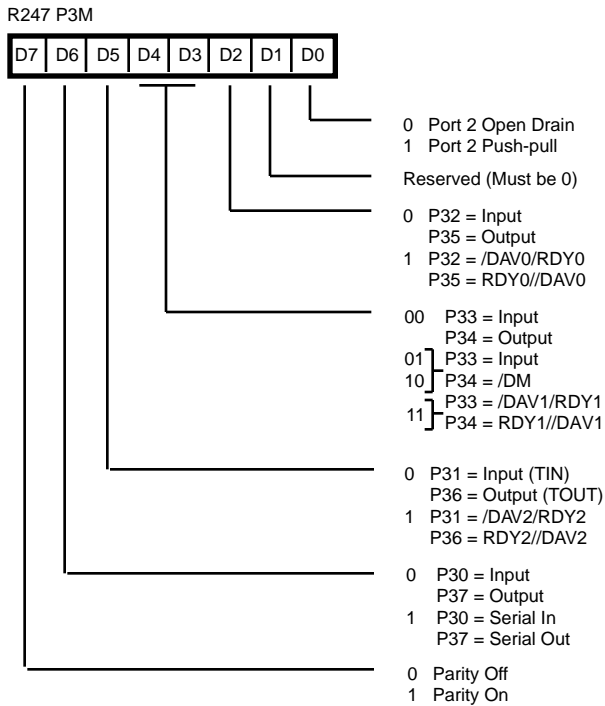


Figure 35. Port 3 Mode Register (F7H: Write Only)

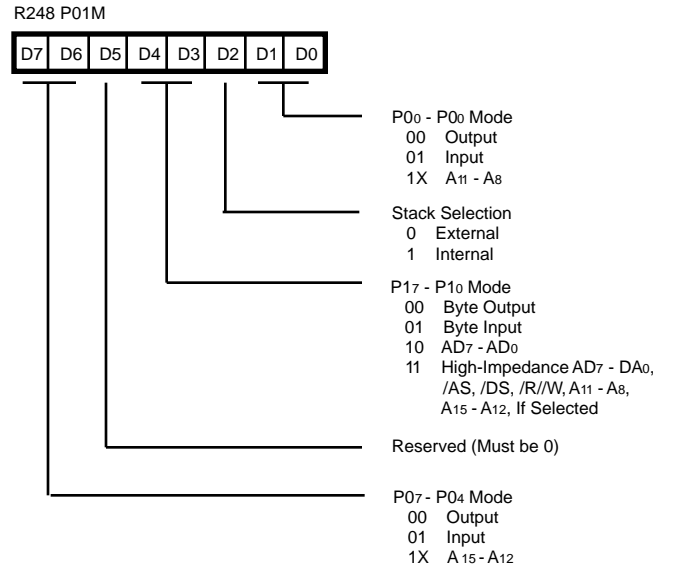


Figure 36. Port 0 and 1 Mode Register (F8H: Write Only)

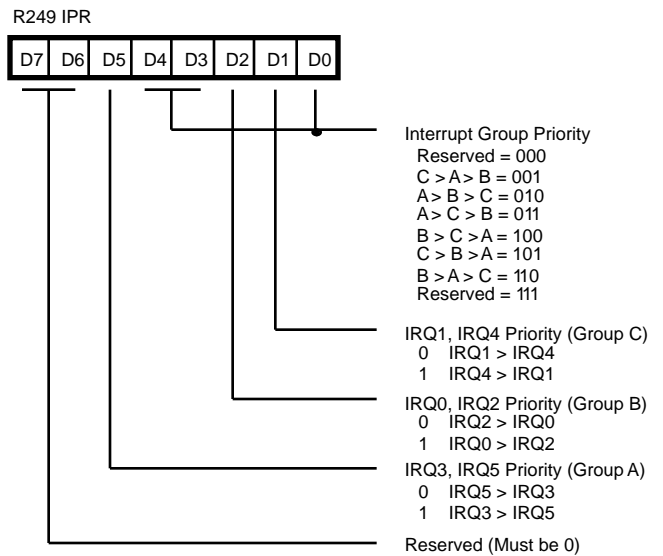
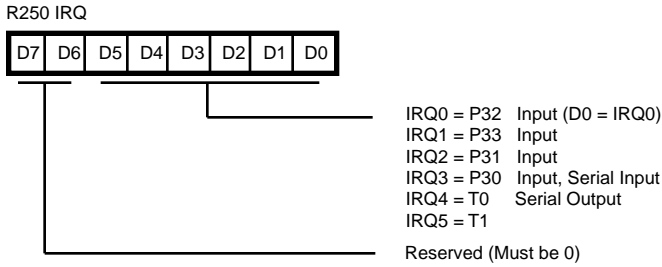
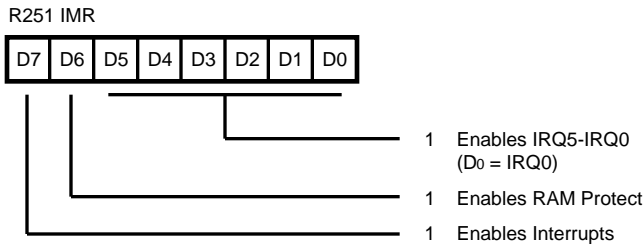


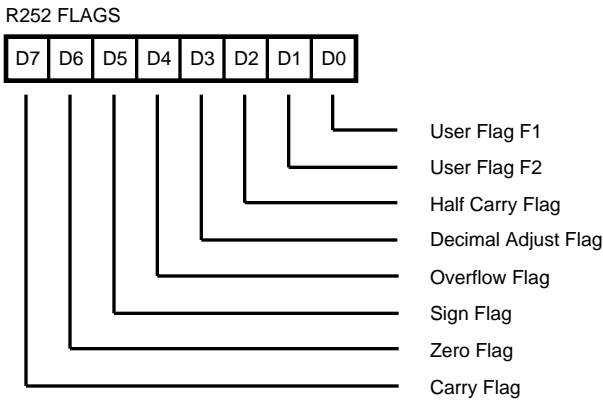
Figure 37. Interrupt Priority Register (F9H: Write Only)



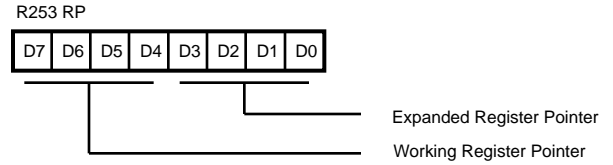
**Figure 38. Interrupt Request Register (FAH: Read/Write)**



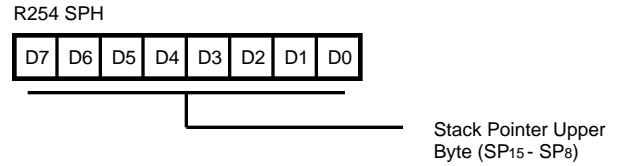
**Figure 39. Interrupt Mask Register (FBH: Read/Write)**



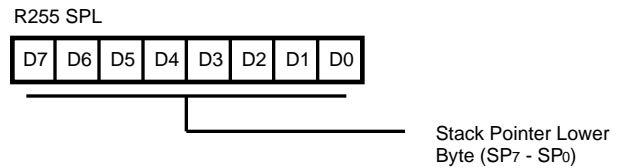
**Figure 40. Flag Register (FCH: Read/Write)**



**Figure 41. Register Pointer Register (FDH: Read/Write)**



**Figure 42. Stack Pointer Register (FEH: Read/Write)**



**Figure 43. Stack Pointer Register (FFH: Read/Write)**

Z8 EXPANDED REGISTER FILE CONTROL REGISTERS

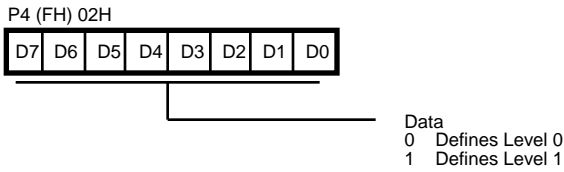
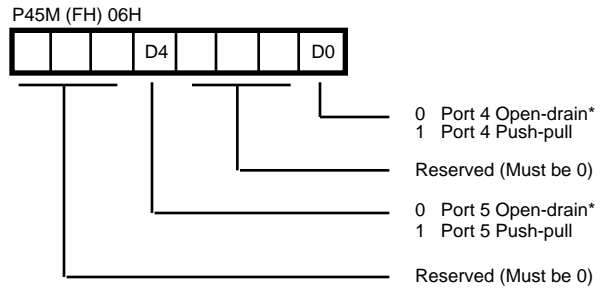


Figure 44. Port 4 Data Register  
(F 02: Read/Write)



\*Default Value After RESET

Figure 48. Port 4/5 Configuration Register  
(F 06: Write Only)

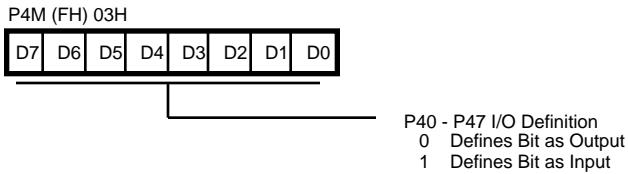


Figure 45. Port 4 Mode Register  
(F 03: Write Only)

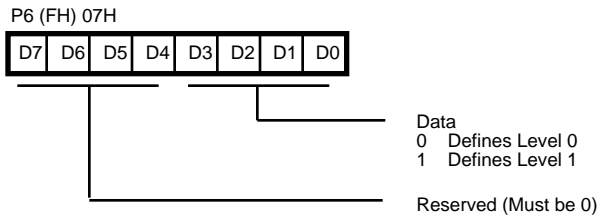


Figure 49. Port 6 Data Register  
(F 07: Read/Write)

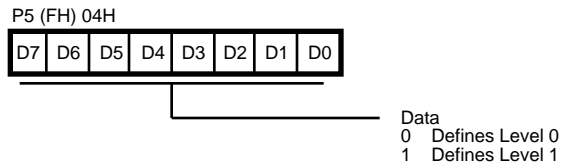
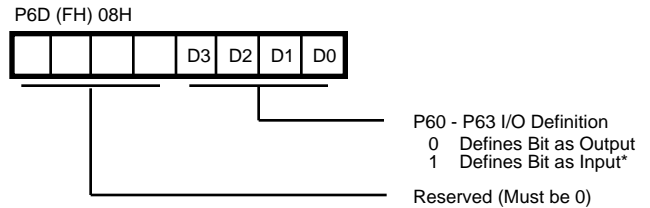
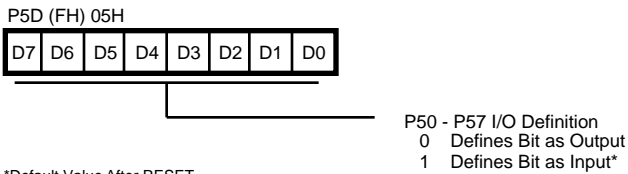


Figure 46. Port 5 Data Register  
(f 04: Read/Write)



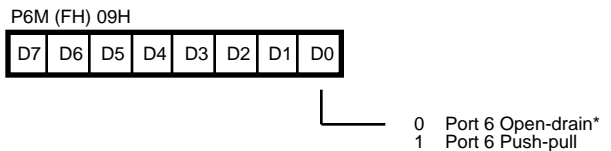
\*Default Value After RESET

Figure 50. Port 6 Mode Register  
(F 08: Write Only)



\*Default Value After RESET

Figure 47. Port 5 Mode Register  
(F 05: Write Only)



\*Default Value After RESET

Figure 51. Port 6 Mode Register  
(F 09: Write Only)

PACKAGE INFORMATION

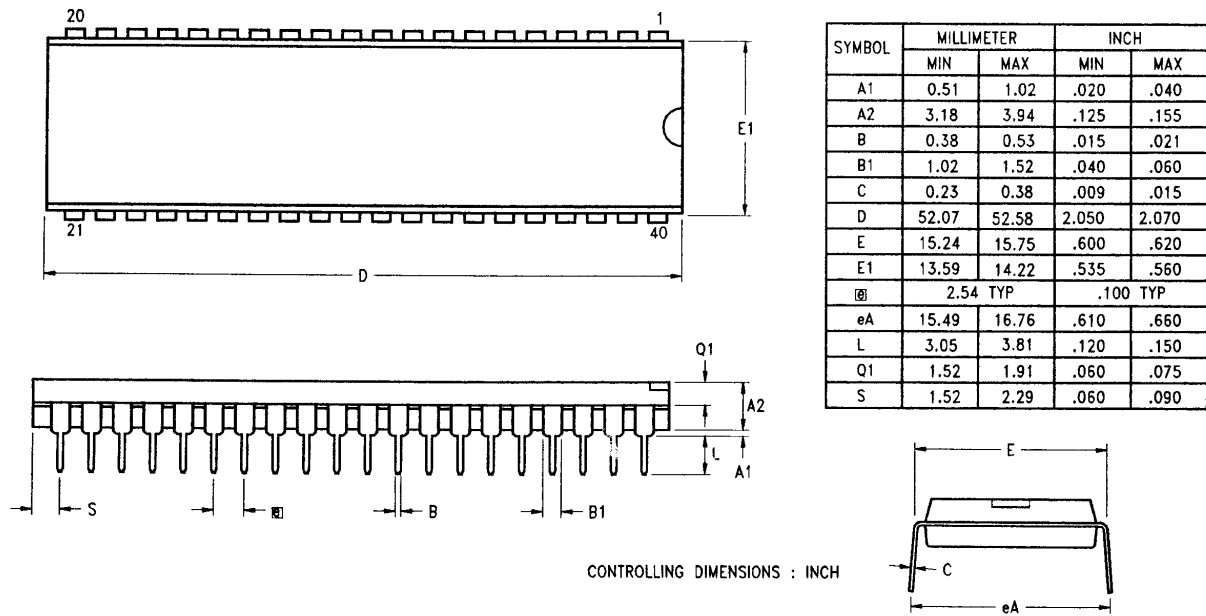


Figure 52. 40-Pin DIP Package Diagram

Figure 53. 44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)

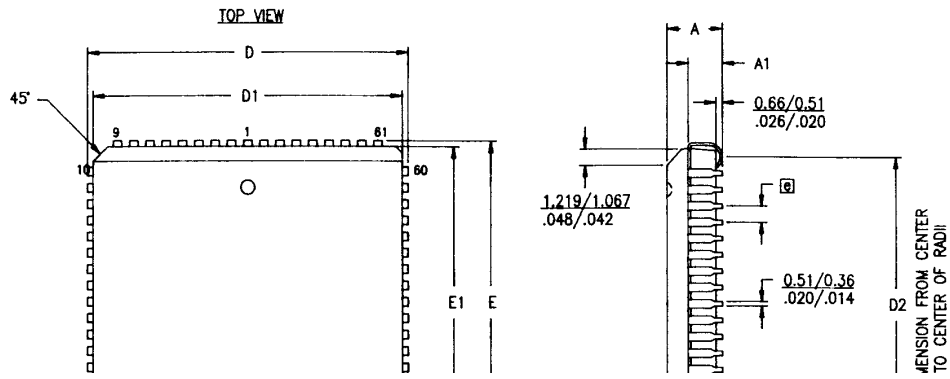


Figure 54. 64-Pin DIP Package Diagram

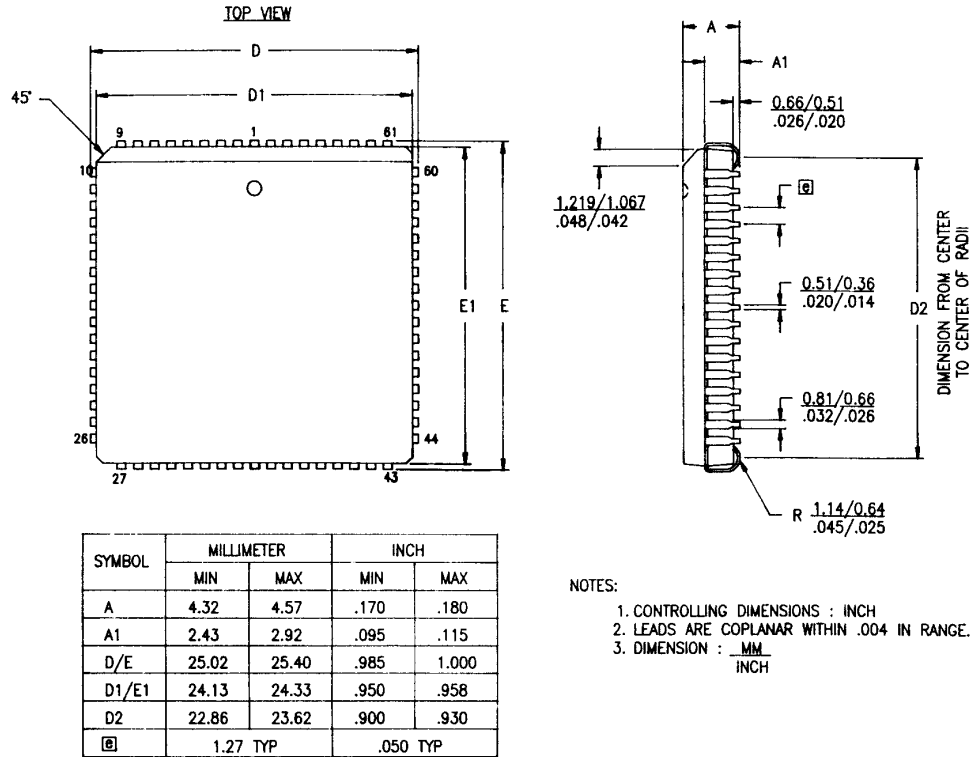


Figure 55. 68-Pin PLCC Package Diagram

## ORDERING INFORMATION

### Z86C61/62/96

#### 16 MHz

**40-pin DIP**      **44-pin PLCC**  
Z86C6116PSC      Z86C6116VSC

#### 16 MHz

**64-pin DIP**      **68-pin PLCC**  
Z86C6216PSC      Z86C6216VSC

#### 20 MHz

**64-pin DIP**      **68-pin PLCC**  
Z86C9620PSC      Z86C9620VSC

For fast results, contact your Zilog sales office for assistance in ordering the part desired.

### Codes

#### Package

P = Plastic DIP  
V = Plastic Chip Carrier

#### Preferred Temperature

S = 0°C to +70°C

#### Longer Lead Time

E = -40°C to 105°C

#### Speeds

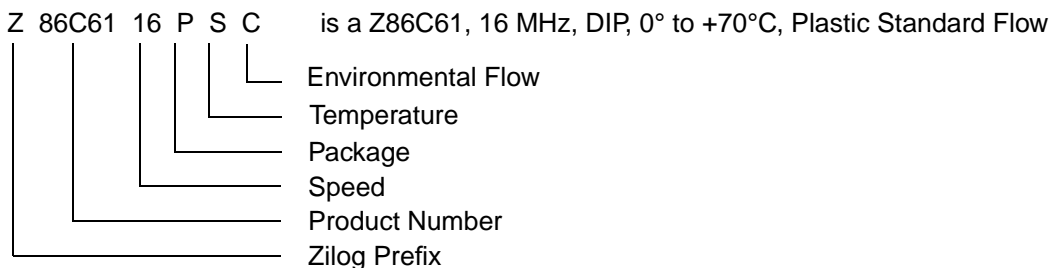
16 = 16 MHz

20 = 20 MHz

#### Environmental

C = Plastic Standard

Example:



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