

1.2V - 8V, 3A PFET Load Switch with Configurable Slew Rate, Fast Transient Isolation and Hysteretic Control

Check for Samples: [TPS27082L](#)

FEATURES

- **Low ON Resistance, High Current PFET**
 - $R_{ON} = 32m\Omega$ (Typical) at $V_{GS} = -4.5V$
 - $R_{ON} = 44m\Omega$ (Typical) at $V_{GS} = -3.0V$
 - $R_{ON} = 85m\Omega$ (Typical) at $V_{GS} = -1.8V$
 - $R_{ON} = 97m\Omega$ (Typical) at $V_{GS} = -1.5V$
 - $R_{ON} = 155m\Omega$ (Typical) at $V_{GS} = -1.2V$
- **Configurable Turn-ON and Turn-OFF Slew Rate**
 - 10 μ sec Default Minimum Output Rise Time at $V_{IN}=5V$
- **Configurable Turn-ON and Turn-OFF Slew Rate**
- **Supports a Wide Range of V_{IN} 1.2V up to 8V**
- **Excellent OFF Isolation Even Under Fast Input Transients**
- **1.0V up to 8V NMOS Control Logic Interface With Configurable Hysteresis**
- **Fully Protected Against ESD (All Pins)**
 - HBM 2kV, CDM 500V
- **Very Low ON-state Quiescent Current (Down to 1.2 μ A)**
- **Very Low OFF-state Leakage Current (Typ 100nA)**
- **Available in 2.9mm x 1.6mm x 0.75mm SOT-23 (DDC) Package**

APPLICATIONS

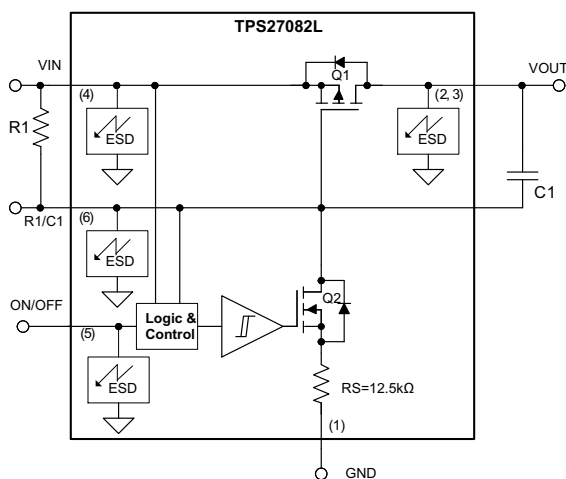
- **High Side Load Switch**
- **Inrush-current Control**
- **Power Sequencing and Control**
- **Stand-by Power Isolation**
- **Portable Power Switch**

DESCRIPTION

The TPS27082L IC is a high side load switch that integrates a Power PFET and a control circuit in a tiny TSOT-23 package. TPS27082L requires very low ON-state quiescent current and offers very low OFF-state leakage thus optimizing system power efficiency.

TPS27082L ON/OFF logic interface features hysteresis, thus providing a robust logic interface even under very noisy operating conditions. TPS27082L ON/OFF interface supports direct interfacing to low voltage GPIOs down to 1V. The TPS27082L level shifts ON/OFF logic signal to V_{IN} levels without requiring an external level shifter.

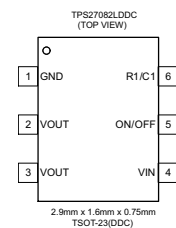
TPS27082L features a novel OFF isolation circuit that prevents PMOS from turning ON in applications that may have fast transients, at the V_{IN} pin when the load switch is in the OFF-state.



Simplified Block & Application Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



TPS27082L Package (DDC)

Component Table (Typical Application)

Component	Description
R1	Level Shift Pull-up Resistor
C1	Optional ⁽¹⁾

(1) Required for load inrush current (slew rate) control.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾⁽³⁾

Specified at $T_J = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
$V_{IN_{max}}$, $V_{OUT_{max}}$	VIN, VOUT pin maximum voltage with respect to GND pin	-0.1	8	V
$V_{ON/OFF}$	ON/OFF control voltage	-0.3	8	V
I_{Q1-ON}	Max continuous drain current of Q1		3	A
	Max pulsed drain current of Q1 ⁽⁴⁾		9.5	
P_D	Max power dissipation at $T_A = 25^{\circ}\text{C}$, $T_J = 150^{\circ}\text{C}$ ⁽⁴⁾	6 Pin-TSOT, $\theta_{JA} = 105^{\circ}\text{C/W}$		1190 mW
All pins	ESD Rating – HBM		2000	V
	ESD Rating – CDM		500	V
T_A	Operating free-air ambient temperature range	-40	125 ⁽⁵⁾	$^{\circ}\text{C}$
T_{J-max}	Operating virtual junction temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Operating at the absolute T_{J-max} of 150°C can affect reliability – for higher reliability it is recommended to ensure $T_J < 125^{\circ}\text{C}$
- (3) Refer to TI’s design support web page at www.ti.com/thermal for improving device thermal performance.
- (4) Pulse Width < $300\mu\text{s}$, Duty Cycle < 2%
- (5) T_{J-max} limits and other related conditions apply. Refer to SOA charts, [Figure 8](#) through [Figure 13](#)

DISSIPATION RATINGS⁽¹⁾⁽²⁾⁽³⁾

BOARD	PACKAGE	θ_{JC}	θ_{JA} ⁽⁴⁾	$T_A < 25^{\circ}\text{C}$	$T_A = 70^{\circ}\text{C}$	$T_A = 85^{\circ}\text{C}$	$T_A = 105^{\circ}\text{C}$	DERATING FACTOR ABOVE $T_A = 25^{\circ}\text{C}$
High-K (JEDEC 51-7)	6-Pin TSOT (DDC)	43°C/W	105°C/W	1190 mW	760 mW	619 mW	428 mW	9.55 mW/ $^{\circ}\text{C}$

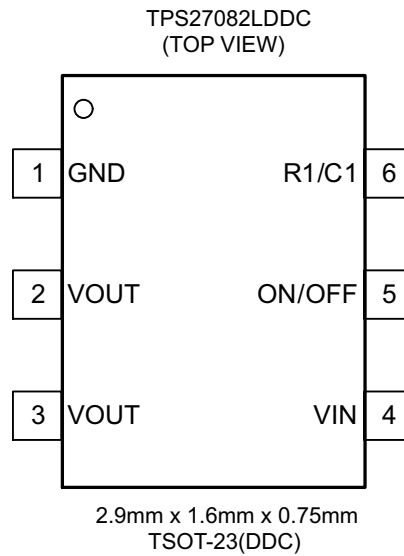
- (1) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
- (2) Refer to TI’s design support web page at www.ti.com/thermal for improving device thermal performance
- (3) Package thermal data based on a $76 \times 114 \times 1.6\text{mm}$, 4-layer board with 2-oz Copper on outer layers
- (4) Operating at the absolute T_{J-max} of 150°C can affect reliability; $T_J \leq 125^{\circ}\text{C}$ is recommended

ELECTRICAL CHARACTERISTICS

 Full temperature range spans $T_J = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = T_J = 25^{\circ}\text{C}$			FULL TEMP RANGE ⁽¹⁾		UNIT
		MIN	TYP	MAX	MIN	MAX	
OFF CHARACTERISTICS							
BV_{IN}	VIN breakdown voltage	$V_{ON/OFF} = 0\text{ V}, V_{GS}(Q1) = 0\text{ V}, I_{D}(Q1) = 250\text{ }\mu\text{A}$			-8	-8	V
I_{FIN}	VIN pin total forward leakage current ⁽²⁾	$V_{IN} = 8\text{ V}, V_{ON/OFF} = 0\text{ V}, R_L = 2.5\text{ }\Omega$			0.15	30	μA
		$V_{IN} = 5\text{ V}, V_{ON/OFF} = 0\text{ V}, R_L = 2.5\text{ }\Omega$			0.04	12	
ON CHARACTERISTICS⁽³⁾							
V_{T+} (VIH)	Positive going ON/OFF threshold voltage ⁽⁴⁾	$V_{IN} = 5.0\text{ V}, R_1 = 125\text{ k}\Omega^{(1)}, R_L = 2.5\text{ }\Omega$				1.0	V
		$V_{IN} = 5.0\text{ V}, R_1 = 1\text{ M}\Omega, R_L = 2.5\text{ }\Omega$				1.0	
V_{T-} (VIL)	Negative going ON/OFF threshold voltage ⁽⁴⁾	$V_{IN} = 5.0\text{ V}, I_{D}(Q1) < 175\text{ }\mu\text{A}, R_1 = 125\text{ k}\Omega^{(1)}$				400	mV
		$V_{IN} = 5.0\text{ V}, I_{D}(Q1) < 175\text{ }\mu\text{A}, R_1 = 1\text{ M}\Omega$				270	
ΔV_T ($V_{T+} - V_{T-}$)	ON/OFF input logic hysteresis ⁽⁴⁾	$V_{IN} = 5.0\text{ V}, R_1 = 125\text{ k}\Omega^{(1)}$				600	mV
		$V_{IN} = 5.0\text{ V}, R_1 = 1\text{ M}\Omega$				730	
$R_{Q1(ON)}$	Q1 Channel ON resistance ⁽⁵⁾	$V_{GS_{Q1}} = -4.5\text{ V}, I_D = 3.0\text{ A}$			32	52	64
		$V_{GS_{Q1}} = -3.0\text{ V}, I_D = 2.5\text{ A}$			44	66	84
		$V_{GS_{Q1}} = -2.5\text{ V}, I_D = 2.5\text{ A}$			50	76	92
		$V_{GS_{Q1}} = -1.8\text{ V}, I_D = 2.0\text{ A}$			82	113	147
		$V_{GS_{Q1}} = -1.5\text{ V}, I_D = 1.0\text{ A}$			97	150	173
		$V_{GS_{Q1}} = -1.2\text{ V}, I_D = 0.50\text{ A}$			155	250	260
$R_{GND_{ON}}$	R1/C1 pin to GND pin resistance when Q2 is ON	$V_{ON/OFF} = 1.8\text{ V}$			12.5	14.2	14.5
Q1 DRAIN-SOURCE DIODE PARAMETERS⁽¹⁾⁽³⁾⁽⁶⁾							
$I_{F_{SD}}$	Source-drain diode peak forward current	$V_{F_{SD}(Q1)} = 0.8\text{ V}, V_{ON/OFF} = 0\text{ V}$			1.0		A
$V_{F_{SD}}$	Source-drain diode forward voltage	$I_{F_{SD}(Q1)} = -0.6\text{ A}, V_{ON/OFF} = 0\text{ V}$				1.0	V

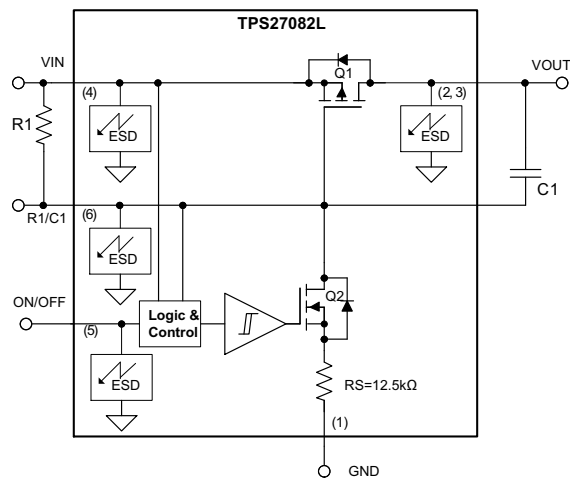
- (1) Specified by design only
- (2) Refer to $I_{F_{VIN}}$ plots for more information
- (3) Pulse width < 300 μs , Duty cycle < 2%
- (4) Refer to charts for more information on V_{T+}/V_{T-} thresholds
- (5) Refer to SOA charts for operating current information
- (6) Not rated for continuous current operation



TPS27082LD and TPS27082LDRV PINOUT

PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
GND	1	Connect to the system GND
VOUT	2, 3	Drain Terminal of Power PFET (Q1) – If required, connect a slew control capacitor between pins VOUT and R1/C1
VIN	4	Source Terminal of Power PFET (Q1) – connect a pull-up resistor between the pins VIN and R1/C1
ON/OFF	5	Active high enable – when driven with a high impedance driver, connect an external pull down resistor to GND
R1/C1	6	Gate Terminal of Power PFET (Q1)



Typical Application Diagram

APPLICATION INFORMATION

The TPS27082L IC is a high side load switch that integrates a Power PFET and its control circuit in a tiny TSOT-23 package. TPS27082L supports up to 8V supply input and up to 3A of load current. The TPS27082L can be used in a variety of applications. Figure 1 shows a general application of TPS27082L to control capacitive load inrush current.

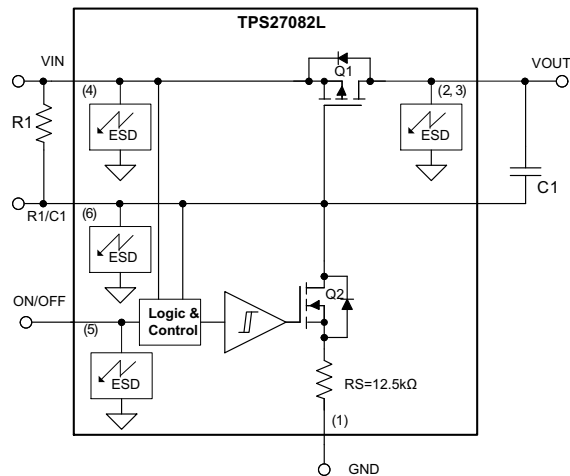


Figure 1. Typical Application Diagram

Configuring Q1 ON resistance

V_{GS-Q1} , Gate-Source voltage, of PMOS transistor Q1 sets its ON resistance $R_{Q1(ON)}$. Connecting a high value pull up resistor R1 maximizes ON state V_{GS-Q1} and thus minimizes the VIN to VOUT voltage drop. Use the following equation for calculating V_{GS-Q1} :

$$V_{GS-Q1} = -VIN \times \frac{R1}{R1 + 12.5 \text{ k}\Omega} \text{ V} \quad (1)$$

e.g. R1= 125kΩ, VIN = 5V sets $V_{GS-Q1} = -4.5V$

NOTE

It is recommended to keep $R1 \geq 125 \text{ k}\Omega$. Higher value resistor R1 reduces ON-state quiescent current, increases turn-OFF delay, while reducing ON/OFF negative going threshold voltage V_{T-} .

Configuring Turn-ON slew rate

Switching a large capacitive load CL instantaneously results in a load inrush current given by the following equation:

$$I_{inrush} = C_{load} \times \frac{dv}{dt} = C_{load} \times \frac{V_{OUT_{final}} - V_{OUT_{initial}}}{V_{out} \text{ Slew Rate}} \quad (2)$$

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate (dv/dt) at the output thus leading to a higher load inrush current. To control the inrush current connect a capacitor C1 as shown in the Figure 1. Use the following approximate empirical equation to configure the TPS27082L slew rate to a specific value.

$$t_{rise} = \frac{50 \times 10^3 \times C1}{VIN^{2/3}} \text{ sec} \quad (3)$$

Where t_{rise} is the time delta starting from the ON/OFF signal's rising edge to charge up the load capacitor CL from 10% to 90% of VIN voltage.

Table 1. Capacitor C1 Selection for Standard Output Rise Time

t _{rise} (μSec) (Typical)	C1 (F) R1 = 125 kΩ				
	VIN=7V	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.2V
5	0	0	0	0	0
50	3.46n	2.77n	2.10n	1.41n	1.08n
100	6.91n	5.54n	4.21n	2.82n	2.16n
250	17.3n	13.8n	10.5n	7.05n	5.40n
470	32.5n	26.0n	19.8n	13.3n	10.1n
1000	69.1n	55.4n	42.1n	28.2n	21.6n

Note: The t_{rise} equation and the capacitor C1 values recommended in the table above are under typical conditions and are accurate to within ±20%. Ensure R1 > 125kΩ; and select a closest standard valued capacitor C1.

Configuring Turn-OFF delay

TPS27082L PMOS turn-OFF delay from the falling edge of ON/OFF logic signal depends upon the component values of resistor R1 and capacitor C1. Lower values of resistor R1 ensures quicker turn-OFF.

$$t_{off} > (R1 \times C1 \text{ sec}) \quad (4)$$

OFF Isolation Under VIN Transients

TPS27082L architecture helps isolate fast transients at the VIN when PFET is in the OFF state. Best transient isolation is achieved when an external capacitor C1 is not connected across VOUT and R1/C1 pins. When a capacitor C1 is present the VIN to VOUT coupling is capacitive and is set by the C1 to CL capacitance ratio. TPS27082L architecture prevents direct conduction through PFET.

Low Voltage ON/OFF Interface

To turn ON the load switch apply a voltage > 1.0V at the ON/OFF pin. The TPS27082L features hysteresis at its ON/OFF input. The turn-ON and turn-OFF thresholds are dependent upon the value of resistor R1. Refer to the [ELECTRICAL CHARACTERISTICS](#) Table and [Figure 14](#) for details on the positive and negative going ON/OFF thresholds.

In applications where ON/OFF signal is not available connect ON/OFF pin to the VIN pin. The TPS27082L will turn ON and OFF in sync with the input supply connected to VIN.

On-chip Power Dissipation

Use below approximate equation to calculate TPS27082L's on-chip power dissipation P_D:

$$PD = I_{DQ1}^2 \times R_{Q1(ON)} \quad (5)$$

Where, I_{DQ1} is the DC current flowing through the transistor Q1. Refer to the [ELECTRICAL CHARACTERISTICS](#) Table and the [Figure 16](#) through [Figure 22](#) to estimate R_{Q1(ON)} for various values of VGSQ1.

Note: MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 going into saturation region set VGS > VDS+1.0V. E.g. VGS > 1.5V and VDS < 200mV ensures switching region.

Thermal Reliability

For higher reliability it is recommended to limit TPS27082L IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to restrict the die junction temperature target to safe limits:

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \quad (6)$$

Where T_{J(MAX)} is the target maximum junction temperature, T_A is the operating ambient temperature, and θ_{JA} is the package junction to ambient thermal resistance.

Improving Package Thermal Performance

The package θ_{JA} value under standard conditions on a High-K board is available in the Dissipation Rating Table. θ_{JA} value depends upon the PC board layout. An external heat sink and/or a cooling mechanism like a cold air fan can help reduce θ_{JA} and thus improving device thermal capability. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

APPLICATION EXAMPLES

TFT LCD Module Inrush Current Control

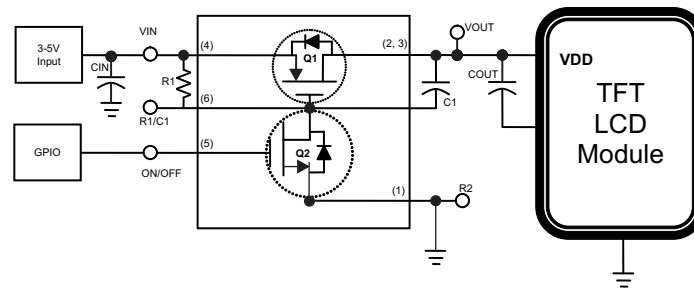


Figure 2. Inrush Current Control Using TPS27082L

LCD panels require inrush current control to prevent permanent system damages during turn-ON and turn-OFF events.

Standby Power Isolation

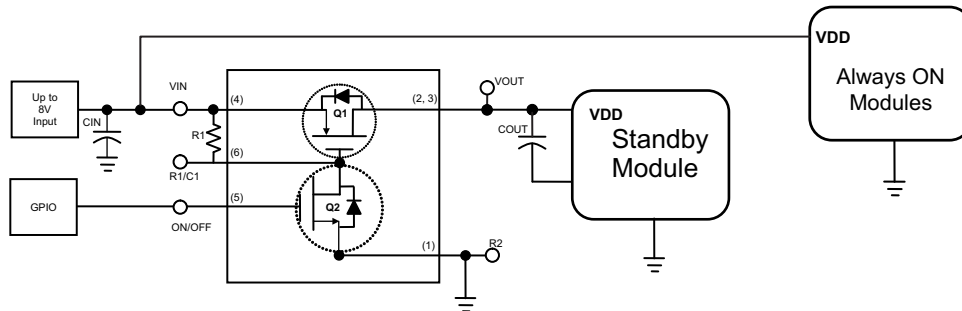


Figure 3. boost

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27082L requires only a single pull-up resistor. In this configuration the VOUT voltage rise time is approximately 250ns when VIN = 5V.

Boost Regulator with True Shutdown

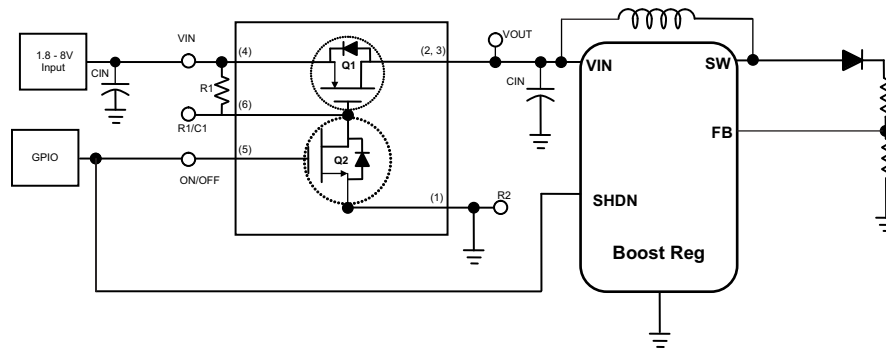


Figure 4. True Shutdown Using TPS27082L

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator is shut down. Adding a TPS27082L in the input side power path prevents this leakage current and thus providing a true shutdown.

Single Module Multiple Power Supply Sequencing

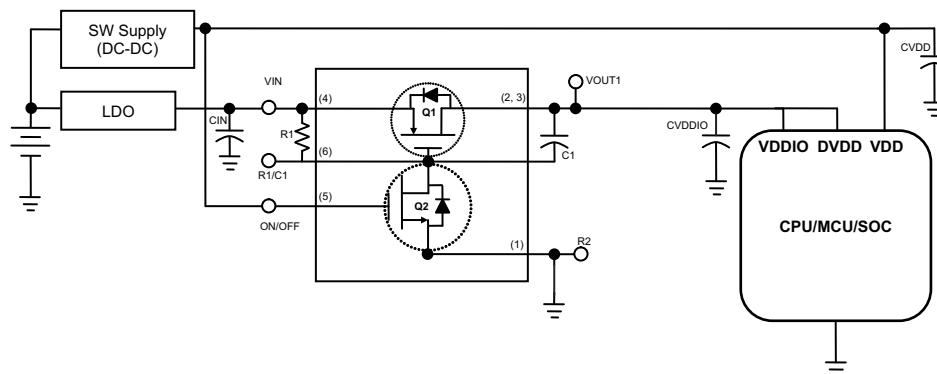


Figure 5. Power Sequencing Using TPS27082L, Example 1

Most modern SOC and CPUs require multiple voltage inputs for its Analog, Digital cores and IO interfaces. These ICs require that these supplies be applied simultaneously or in a certain sequence. TPS27082L when configured, as shown in Figure 5, with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, will delay the early arriving LDO output to match up with late arriving DC-DC output and thus achieving power sequencing.

Multiple Modules Interdependent Power Supply Sequencing

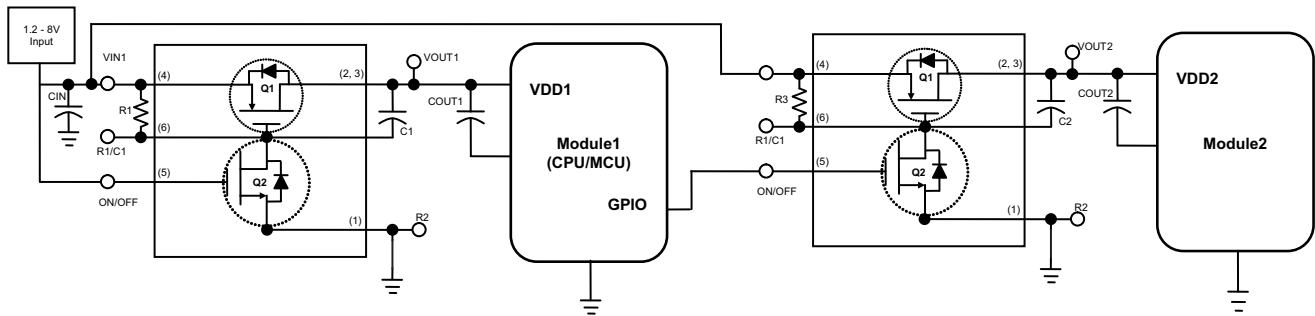


Figure 6. Power Sequencing Using TPS27082L, Example 2

For system integrity reasons a certain power sequencing may be required among various modules. As shown in Figure 6, Module 2 will power up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. TPS27082L when used as shown in Figure 6 will not only sequence the Module 2 power, but also it will help prevent inrush current into the power path of Module 1 and 2.

Multiple Modules Interdependent Supply Sequencing without a GPIO Input

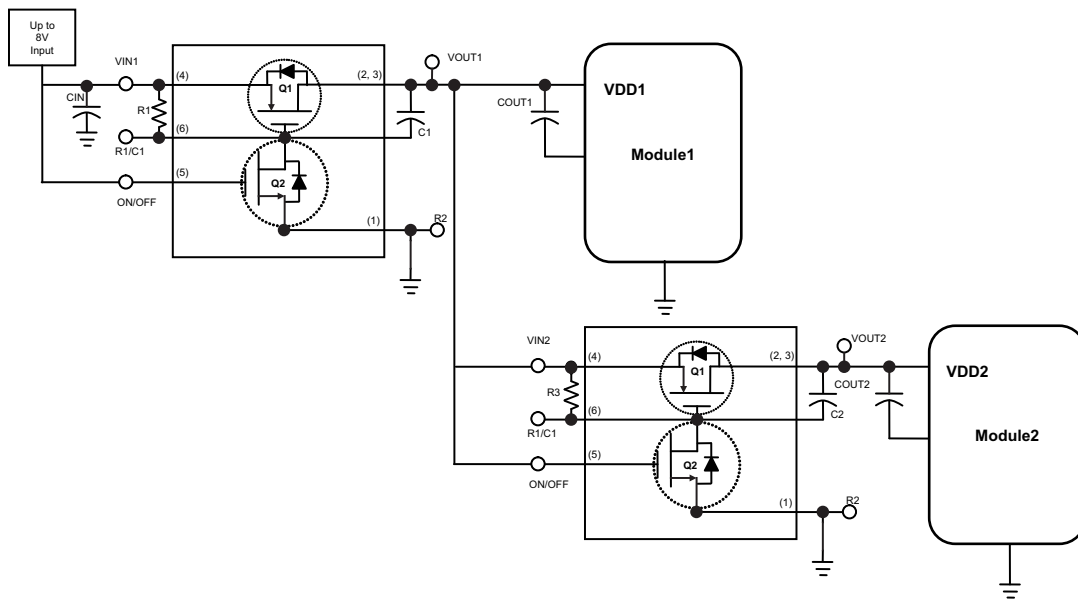


Figure 7. Power Sequencing using TPS27082L, Example 3

When a GPIO signal is not available connecting the ON/OFF pin of TPS27082 connected to Module 2 will power up Module 2 after Module 1, when resistor R4 and capacitor C1 are chosen appropriately. The two TPS27082L in this configuration will also control load inrush current.

PFET Q1 Minimum Safe Operating Area

(Refer to [DISSIPATION RATINGS](#)⁽¹⁾⁽²⁾⁽³⁾ for PC board details)

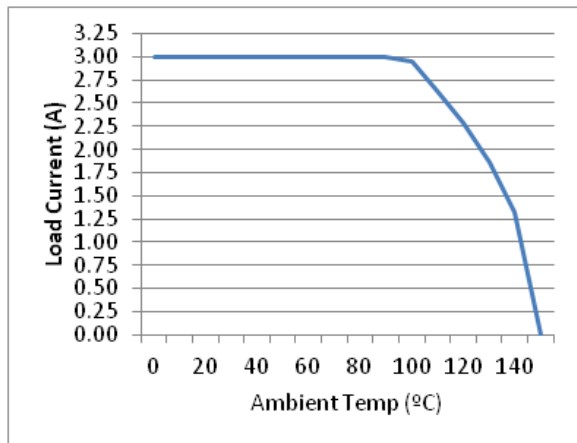


Figure 8. Q1 SOA at VGS_Q1=-4.5V

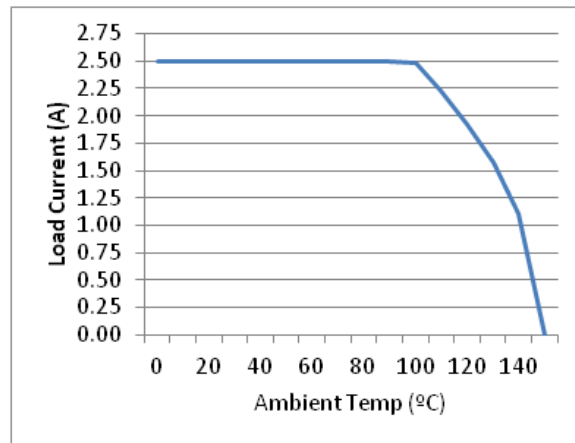


Figure 9. Q1 SOA at VGS_Q1=-3.0V

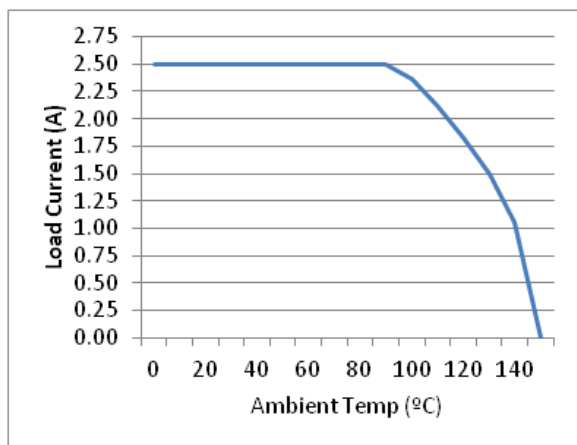


Figure 10. Q1 SOA at VGS_Q1=-2.5V

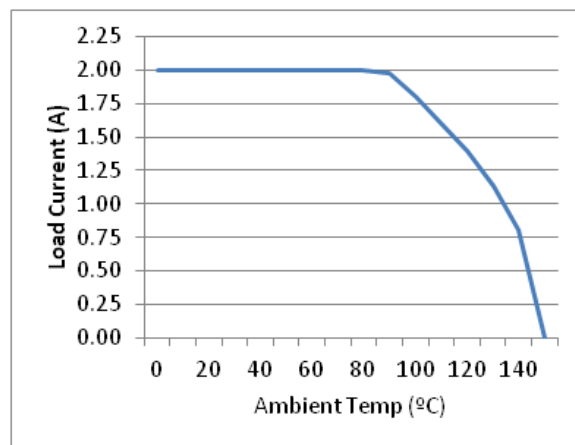


Figure 11. Q1 SOA at VGS_Q1=-1.8V

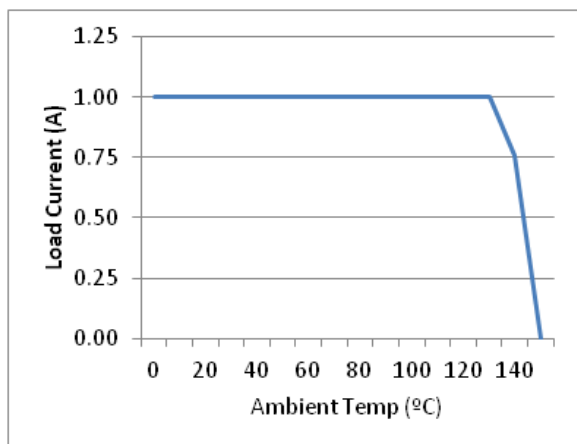


Figure 12. Q1 SOA at VGS_Q1=-1.5V

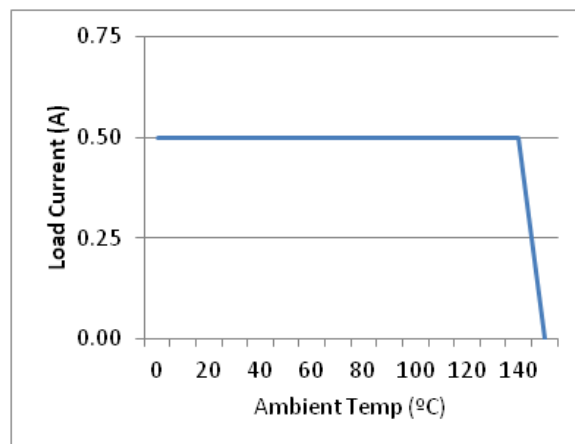


Figure 13. Q1 SOA at VGS_Q1=-1.2V

(1) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
 (2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
 (3) Package thermal data based on a 76x114x1.6mm, 4-layer board with 2-oz Copper on outer layers

PFET Q1 Minimum Safe Operating Area (continued)

(Refer to [DISSIPATION RATINGS](#)⁽¹⁾⁽²⁾⁽³⁾ for PC board details)

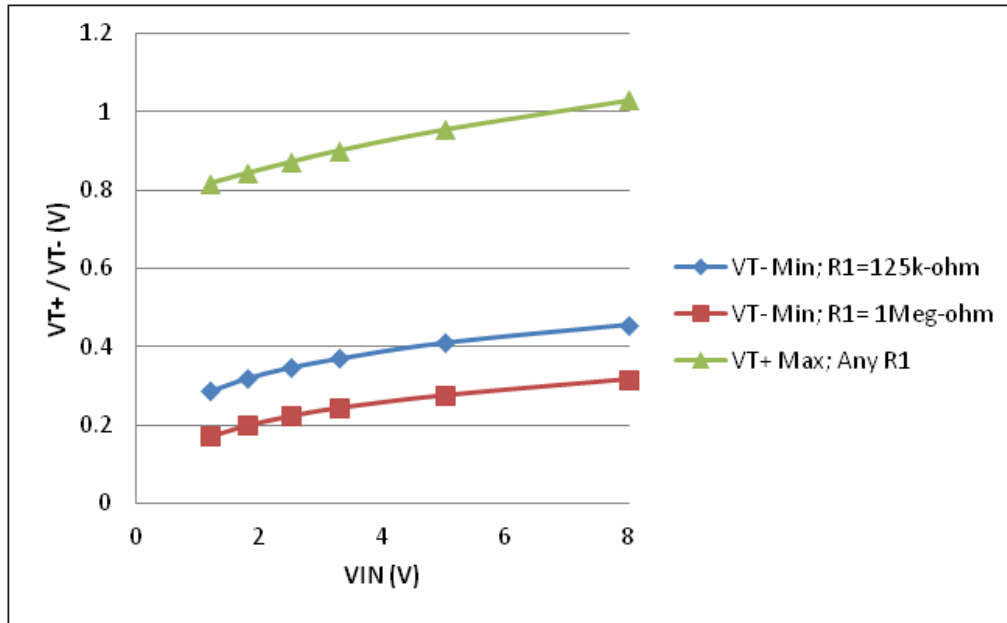


Figure 14. ON/OFF Positive and Negative Going Threshold Voltage

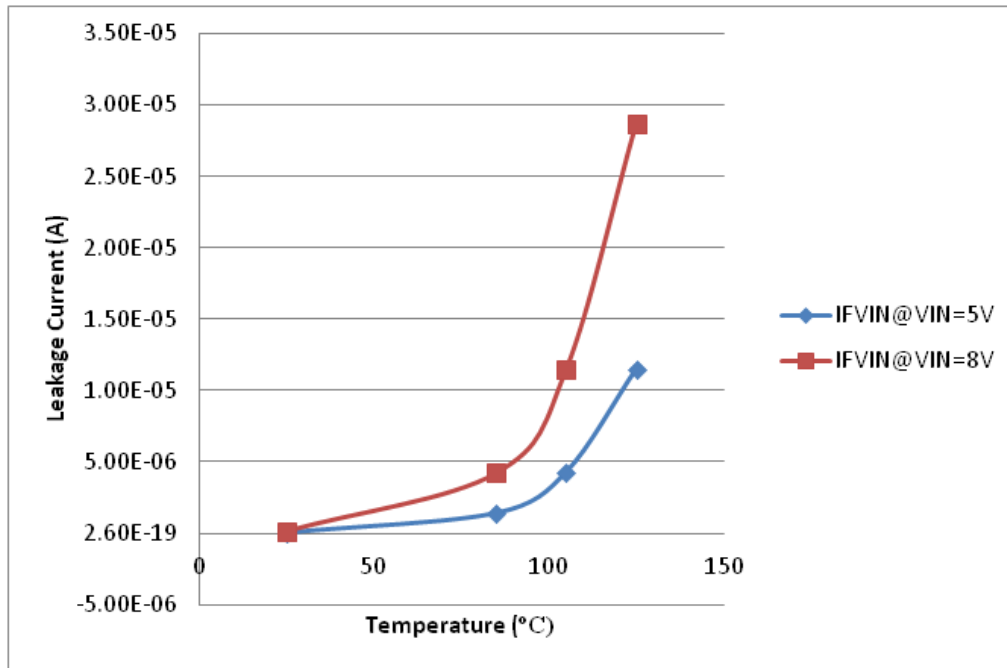


Figure 15. VIN Pin Leakage Current

Typical VIN to VOUT Voltage Drop Characteristic Plots

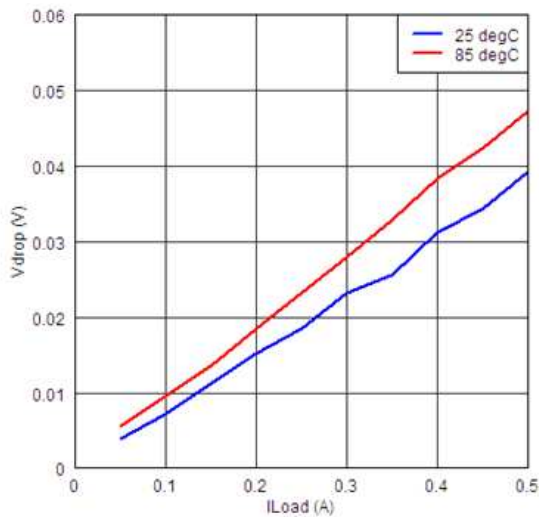


Figure 16. Vdrop vs IL; VGS_Q1 = -1.2V

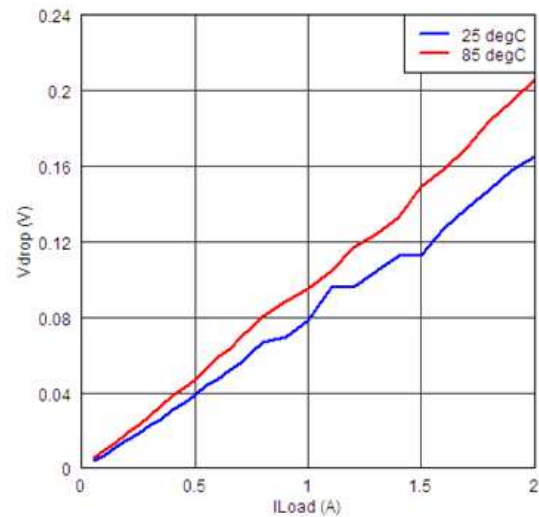


Figure 17. Vdrop vs IL; VGS_Q1 = -1.8V

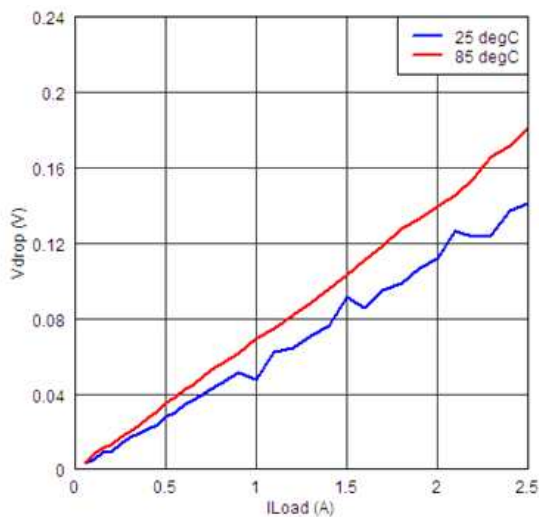


Figure 18. Vdrop vs IL; VGS_Q1 = -2.5V

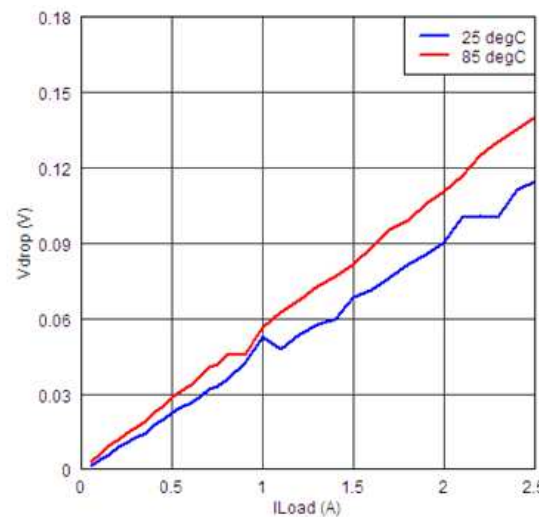


Figure 19. Vdrop vs IL; VGS_Q1 = -3.3V

Typical VIN to VOUT Voltage Drop Characteristic Plots (continued)

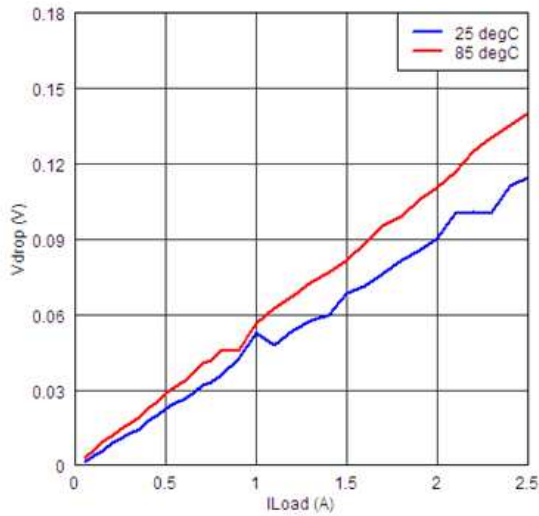


Figure 20. Vdrop vs IL; VGS_Q1 = -4.5V

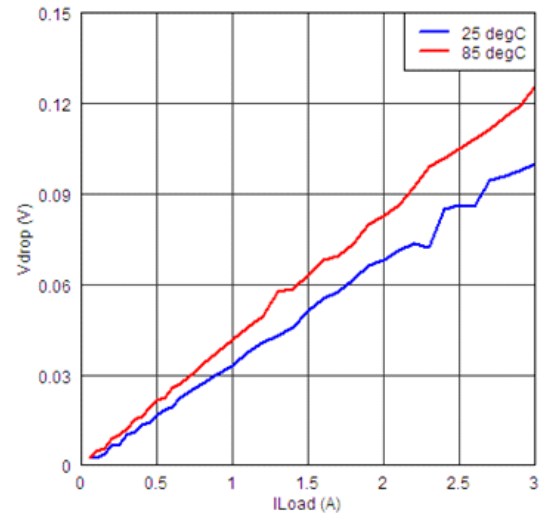


Figure 21. Vdrop vs IL; VGS_Q1 = -5.5V

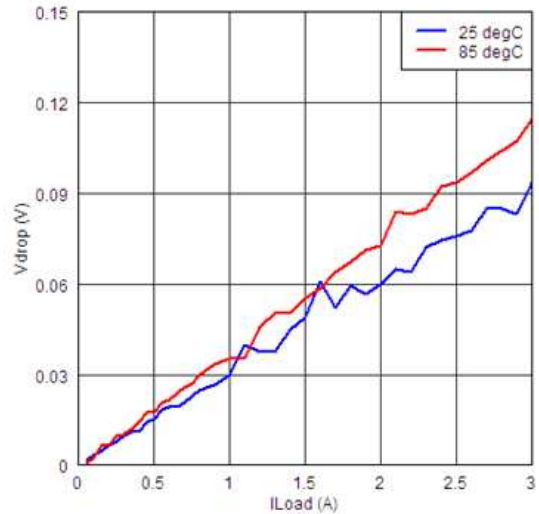


Figure 22. Vdrop vs IL; VGS_Q1 = -7V

REVISION HISTORY

Changes from Original (December 2012) to Revision A **Page**

- Updated wording in the document. 1
-

Changes from Revision A (April 2013) to Revision B **Page**

- Removed Ordering Information table. 2
 - Fixed UNIT typo for ON/OFF input logic hysteresis PARAMETER. 3
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS27082LDDCR	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	BUA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27082LDDCR	SOT	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

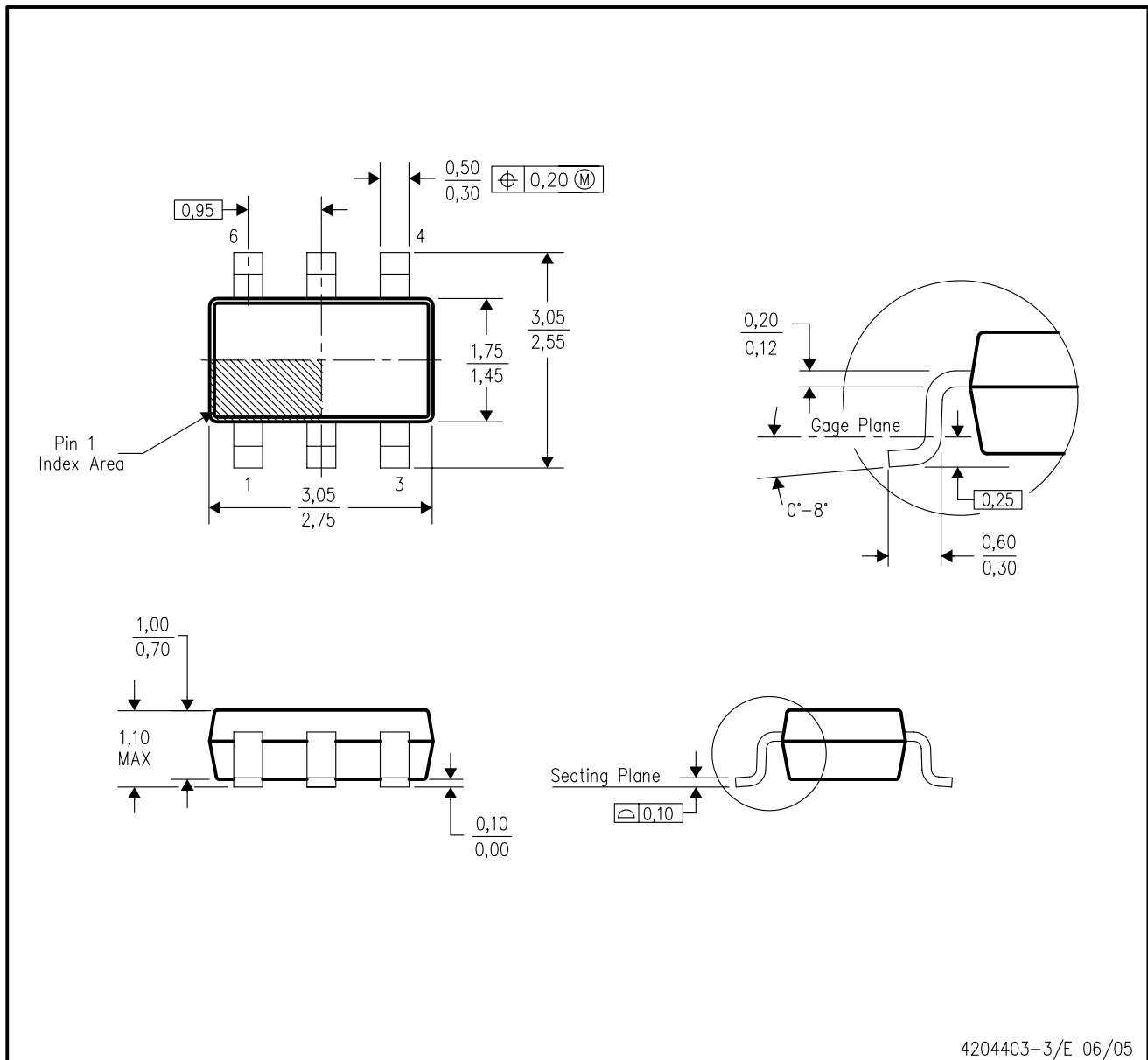


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27082LDDCR	SOT	DDC	6	3000	180.0	180.0	30.0

DDC (R-PDSO-G6)

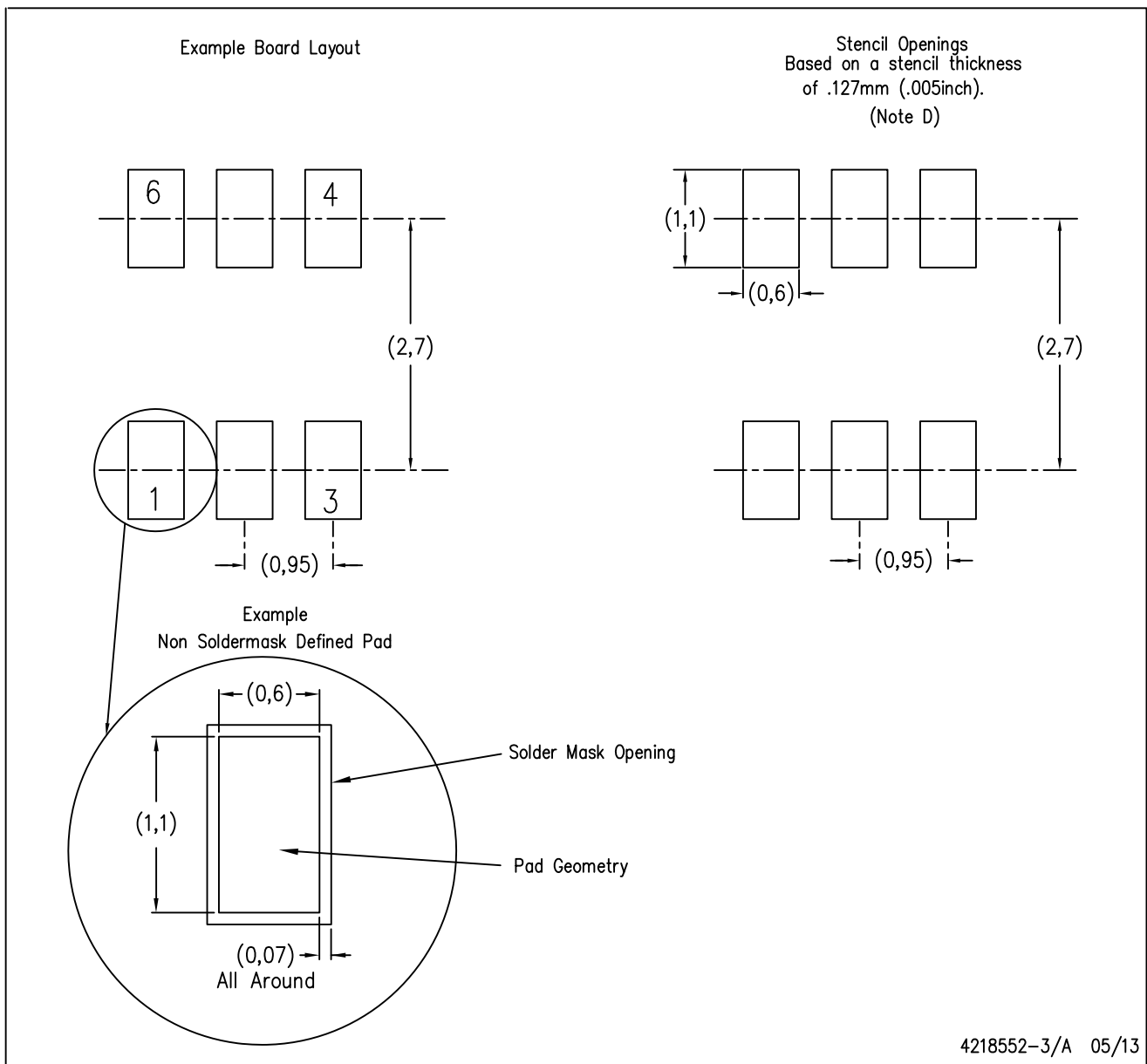
PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-193 variation AA (6 pin).

DDC (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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