# NOIP1SN1300A, NOIP1SN0500A, NOIP1SN0300A

# **PYTHON 0.3/0.5/1.3 Megapixel** Global Shutter CMOS Image Sensors

#### Features

- SXGA: 1280 x 1024 Active Pixels, 1/2" Optical Format SVGA: 800 x 600 Active Pixels, 1/3.6" Optical Format VGA: 640 x 480 Active Pixels, 1/4" Optical Format
- 4.8 μm x 4.8 μm Low Noise Global Shutter Pixels with In-pixel CDS
- Monochrome (SN) or Color (SE)
- Zero ROT Mode Enabling Faster Frame Rate
- Frame Rate at Full Resolution (LVDS)
  - 210/175 frames per second @ SXGA (Zero ROT/Normal ROT)
  - 560/420 frames per second @ SVGA (Zero ROT/Normal ROT)
  - 860/620 frames per second @ VGA (Zero ROT/Normal ROT)
- 43 Frames per Second (fps) at Full Resolution (CMOS)
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 8-bit or 10-bit Output Mode
- Four Low Voltage Differential Signaling (LVDS) High Speed Serial Outputs or Parallel CMOS Output
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter, Rolling Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR)
- Dual Power Supply (3.3 V and 1.8 V)
- -40°C to +85°C Operational Temperature Range
- 48-pin LCC and Bare Die
- 590 mW Power Dissipation (LVDS)
- 375 mW Power Dissipation (CMOS)
- These Devices are Pb-Free and are RoHS Compliant

#### Applications

- Machine Vision
- Motion Monitoring
- Security
- Barcode Scanning (2D)

#### Description

The Python's high sensitivity 4.8 µm x 4.8 µm pixels support low noise "pipelined" and "triggered" global shutter readout modes. In global shutter mode, the sensor supports correlated double sampling (CDS) readout, reducing noise and increasing dynamic range.



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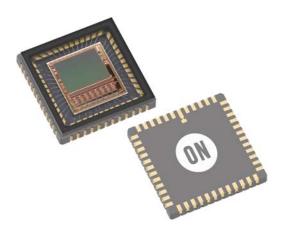


Figure 1. PYTHON 1300 Photograph

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image's black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to 8 regions can be programmed, achieving even higher frame rates.

The image data interface of the P1-SN/SE part consists of four LVDS lanes, facilitating frame rates up to 210 frames per second in Zero ROT mode. Each channel runs at 720 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiving end. The P2-SN/SE part provides a parallel CMOS output interface at reduced frame rate.

The PYTHON low resolution family is packaged in a 48-pin LCC package and is available in a monochrome and color version. For NIR variants, please contact your local distributor or email us at imagesensors@onsemi.com.

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#### **SPECIFICATIONS**

#### **Key Specifications**

#### **Table 1. GENERAL SPECIFICATIONS**

| Parameter                                 | Specification   |
|---|---|
| Pixel type                                | In-pixel CDS. Global shutter pixel architecture   |
| Shutter type                              | Pipelined and triggered global shutter  |
| Frame rate<br>Zero ROT/Normal<br>ROT mode | P1–SN/SE:<br>210/175 fps @ SXGA<br>560/420 fps @ SVGA<br>860/620 fps @ VGA<br>P2–SN/SE: 43 fps                          |
| Master clock                              | P1–SN/SE:<br>72 MHz when PLL is used,<br>360 MHz (10–bit) / 288 MHz (8–bit)<br>when PLL is not used<br>P2–SN/SE: 72 MHz |
| Windowing                                 | 8 Randomly programmable windows.<br>Normal, sub-sampled and binned<br>readout modes                                     |
| ADC resolution                            | 10-bit, 8-bit (Note 1)  |
| LVDS outputs                              | P1-SN/SE: 4/2/1 data + sync + clock   |
| CMOS outputs                              | P2-SN/SE: 10-bit parallel output,<br>frame_valid, line_valid, clock   |
| Data rate                                 | P1–SN/SE:<br>4 x 720 Mbps (10–bit) /<br>4 x 576 Mbps (8–bit)<br>P2–SN/SE: 72 MHz  |
| Power dissipation                         | P1–SN/SE: 590 mW, 10–bit mode<br>P2–SN/SE: 375 mW   |
| Package type                              | 48-pin LCC  |

| Parameter                            | Specification  |
|--------------------------------------|--|
| Active pixels                        | SXGA: 1280 (H) x 1024 (V)<br>SVGA: 800 (H) x 600 (V)<br>VGA: 640 (H) x 480 (V) |
| Pixel size                           | 4.8 μm x 4.8 μm  |
| Conversion gain                      | 0.096 LSB10/e <sup>-</sup><br>140 μV/e <sup>-</sup>                            |
| Dark temporal noise                  | < 9e⁻ (Normal ROT, 1x gain)<br>< 7e⁻ (Normal ROT, 2x gain)                     |
| Responsivity at 550 nm               | 7.7 V/lux.s  |
| Parasitic Light<br>Sensitivity (PLS) | <1/8000  |
| Full Well Charge                     | 10000 e⁻   |
| Quantum Efficiency at 550 nm         | 56%  |
| Pixel FPN                            | < 0.5 LSB10  |
| PRNU                                 | < 10 LSB10   |
| MTF                                  | 68% @ 535 nm – X-dir & Y-dir   |
| PSNL at 20°C                         | 120 LSB10/s, 1200 e <sup>-</sup> /s  |
| Dark signal at 20°C                  | 5 e <sup>-</sup> /s, 0.5 LSB10/s   |
| Dynamic Range                        | > 60 dB in global shutter mode   |
| Signal to Noise Ratio<br>(SNR max)   | 40 dB  |

1. The ADC is 11-bit, down-scaled to 10-bit. The PYTHON uses a larger word-length internally to provide 10-bit on the output.

To receive a detailed product data sheet and supporting documentation, visit the CISP Extranet at www.onsemi.com/MyON.

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