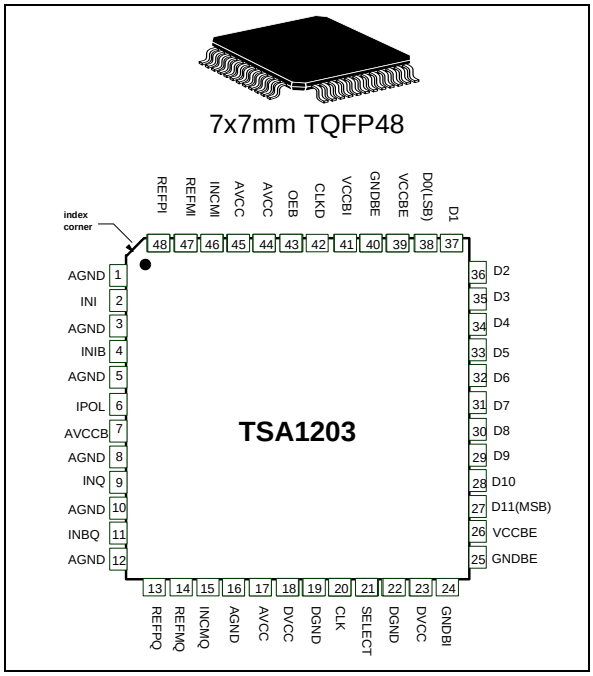
TSA1203

Dual-channel 12-bit 40Msps 215mW A/D converter

Features

- Low power consumption: 215 mW@40 Msps
- Single supply voltage: 2.5 V
- Independent supply for CMOS output stage with 2.5 V/3.3 V capability
- SFDR = -75 dBc @ F_{in} = 10 MHz
- 1GHz analog bandwidth track-and-hold
- Common clocking between channels
- Dual simultaneous sample and hold inputs
- Multiplexed binary word outputs
- Built-in reference voltage with external bias capability



Applications

- Medical imaging and ultrasound
- 3G base station
- I/Q signal processing applications
- High-speed data acquisition systems
- Portable instrumentation

Description

The TSA1203 is a new generation high-speed, dual-channel analog-to-digital converter implemented in a mainstream 0.25 µm CMOS technology that offers high performance and very low power consumption.

The TSA1203 is specifically designed for applications requiring a very low noise floor, high SFDR and good insulation between channels. It is based on a pipeline structure and digital error correction to provide high static linearity at F_S = 40 Msps, and F_{in} = 10 MHz.

Each channel has an integrated voltage reference to simplify the design and minimize external components. It is nevertheless possible to use the circuit with external references.

The ADC binary word outputs are multiplexed in a common bus with a small number of pins.
A tri-state capability is available for the outputs, allowing chip selection. The inputs of the ADC must be differentially driven.

The TSA1203 is available in extended temperature range (-40° C to +85° C), in a small 48-pin TQFP package.

Contents

1 Schematic diagram

Figure 1. TSA1203 block diagram

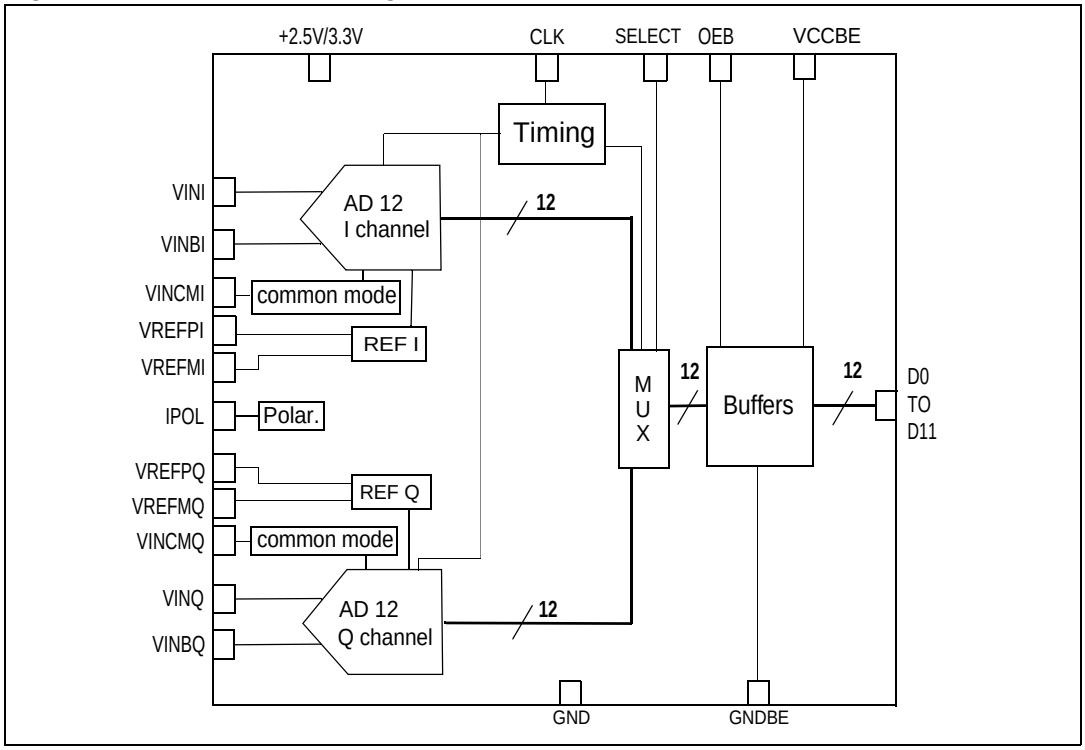
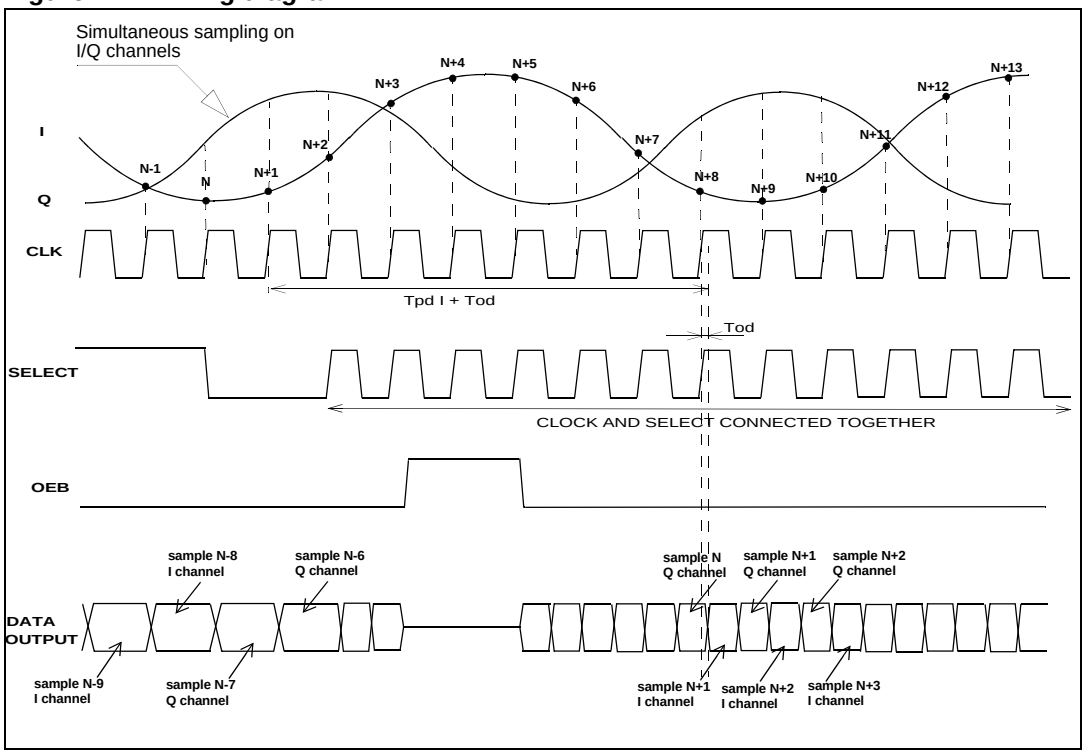


Figure 2. Timing diagram



2 Pin descriptions

Table 1. Pin descriptions (TQFP48 package)

Pin nb	Name	Description	Observation	Pin nb	Name	Description	Observation
1	AGND	Analog ground	0 V	25	GNDBE	Digital buffer ground	0 V
2	INI	I channel analog input		26	VCCBE	Digital buffer power supply	2.5 V/3.3 V
3	AGND	Analog ground	0 V	27	D11(MSB)	Most significant bit output	CMOS output (2.5 V/3.3 V)
4	INBI	I channel inverted analog input		28	D10	Digital output	CMOS output (2.5 V/3.3 V)
5	AGND	Analog ground	0 V	29	D9	Digital output	CMOS output (2.5 V/3.3 V)
6	IPOL	Analog bias current input		30	D8	Digital output	CMOS output (2.5 V/3.3 V)
7	AVCC	Analog power supply	2.5 V	31	D7	Digital output	CMOS output (2.5 V/3.3 V)
8	AGND	Analog ground	0 V	32	D6	Digital output	CMOS output (2.5 V/3.3 V)
9	INQ	Q channel analog input		33	D5	Digital output	CMOS output (2.5 V/3.3 V)
10	AGND	Analog ground	0 V	34	D4	Digital output	CMOS output (2.5 V/3.3 V)
11	INBQ	Q channel inverted analog input		35	D3	Digital output	CMOS output (2.5 V/3.3 V)
12	AGND	Analog ground	0 V	36	D2	Digital output	CMOS output (2.5 V/3.3 V)
13	REFPQ	Q channel top reference voltage		37	D1	Digital output	CMOS output (2.5 V/3.3 V)
14	REFMQ	Q channel bottom reference voltage	0 V	38	D0(LSB)	Least significant bit output	CMOS output (2.5 V/3.3 V)
15	INCMQ	Q channel input common mode		39	VCCBE	Digital buffer power supply	2.5 V/3.3 V - see *Table 14*.
16	AGND	Analog ground	0 V	40	GNDBE	Digital buffer ground	0 V
17	AVCC	Analog power supply	2.5 V	41	VCCBI	Digital buffer power supply	2.5 V
18	DVCC	Digital power supply	2.5 V	42	CLKD	Data clock input	Idle at high level 2.5 V or 3.3 V
19	DGND	Digital ground	0 V	43	OEB	Output enable input	2.5 V/3.3 V CMOS input
20	CLK	Clock input	2.5 V CMOS input	44	AVCC	Analog power supply	2.5 V
21	SELECT	Channel selection	2.5 V CMOS input	45	AVCC	Analog power supply	2.5 V
22	DGND	Digital ground	0 V	46	INCMI	I channel input common mode	
23	DVCC	Digital power supply	2.5 V	47	REFMI	I channel bottom reference voltage	0 V
24	GNDBI	Digital buffer ground	0 V	48	REFPI	I channel top reference voltage	

3 Dynamic characteristics

Dynamic characteristics are measured under the following conditions, unless otherwise specified: AV_{CC} = DV_{CC} = V_{CCB} = 2.5 V, F_S = 40 Msps, F_{in}=10.13 MHz, V_{in}@ -1 dBFS, V_{REFP}=0.8 V, V_{REFM}=0 V, T_{amb} = 25° C.

Table 2. Dynamic characteristics

Symbol	Parameter	Min	Typ	Max	Unit
SFDR	Spurious free dynamic range		-75	-59.5	dBc
SNR	Signal to noise ratio	60.7	67		dB
THD	Total harmonics distortion		-73	-58	dBc
SINAD	Signal to noise and distortion ratio	56.5	66		dB
ENOB	Effective number of bits	9.1	10.8		bits

4 Timing characteristics

Timing characteristics are measured under the following conditions, unless otherwise specified: AV_{CC} = DV_{CC} = V_{CCB} = 2.5 V, F_S = 40 Msps, F_{in}=10.13 MHz, V_{in}@ -1 dBFS, V_{REFP}=0.8 V, V_{REFM}=0 V, T_{amb} = 25° C.

Table 3. Timing characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_S	Sampling frequency		0.5		40	MHz
DC	Clock duty cycle		45	50	55	%
TC1	Clock pulse width (high)		22.5	25		ns
TC2	Clock pulse width (low)		22.5	25		ns
T_{od}	Data output delay (clock edge to data valid)	10 pF load capacitance		9		ns
T_{pd} I	Data pipeline delay for I channel			7		cycles
T_{pd} Q	Data pipeline delay for Q channel			7.5		cycles
T_{on}	Falling edge of OEB to digital output valid data			1		ns
T_{off}	Rising edge of OEB to digital output tri-state			1		ns

5 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage (1)	0 to 3.3	V
DV_{CC}	Digital supply voltage (1)	0 to 3.3	V
V_{CCBE}	Digital buffer supply voltage (1)	0 to 3.6	V
V_{CCBI}	Digital buffer supply voltage (1)	0 to 3.3	V
ID_{out}	Digital output current	-100 to 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
ESD	HBM: human body model(2)	2	kV
	CDM: charged device model(3)	1.5	
Latch-up	Class(4)	A	

1. All voltage values, except differential voltage, are with respect to network ground terminal. The magnitude of input and output voltages must not exceed -0.3 V or V_{CC}.
2. Electrostatic discharge pulse (ESD pulse) simulating a human body discharge of 100 pF through 1.5 kΩ.
3. Discharge to ground of a device that has been previously charged.
4. ST Microelectronics corporate procedure number 0018695.

6 Operating conditions

Table 5. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
AV_{CC}	Analog supply voltage	2.25	2.5	2.7	V
DV_{CC}	Digital supply voltage	2.25	2.5	2.7	V
V_{CCBE}	External digital buffer supply voltage	2.25	2.5	3.5	V
V_{CCBI}	Internal digital buffer supply voltage	2.25	2.5	2.7	V
V_{REFP} I V_{REFP} Q	Forced top voltage reference	0.94		1.5	V
V_{REFM} I V_{REFM} Q	Forced bottom reference voltage	0		0.4	V
V_{INCM} I V_{INCM} Q	Forced input common mode voltage	0.2		1	V

7 Electrical characteristics

Electrical characteristics, unless otherwise specified, are measured at AV_{CC} = DV_{CC} = V_{CCB} = 2.5 V, F_S = 40 Msps, R_{pol} = 18 kΩ, F_{in} = 2 MHz, V_{in}@ -1 dBFS, V_{REFP}=0.8 V, V_{REFM}=0 V, and T_{amb} = 25° C.

Table 6. Analog inputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN}-V_{INB}	Full scale reference voltage	Differential inputs mandatory	1.1	2.0	2.8	Vpp
C_{in}	Input capacitance			7.0		pF
R_{eq}	Equivalent input resistor			10		kΩ
BW	Analog input bandwidth	V_{in}@full scale, F_S=40 Msps		1000		MHz
ERB	Effective resolution bandwidth			70		MHz

Table 7. Digital inputs and outputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock and Select inputs						
V_{IL}	Logic "0" voltage			0	0.8	V
V_{IH}	Logic "1" voltage		2.0	2.5		V
OEB input						
V_{IL}	Logic "0" voltage			0	0.25 x V_{CCBE}	V
V_{IH}	Logic "1" voltage		0.75 x V_{CCBE}	V_{CCBE}		V
Digital outputs						
V_{OL}	Logic "0" voltage	I_{OL}=10 µA		0	0.1 x V_{CCBE}	V
V_{OH}	Logic "1" voltage	I_{OH}=10 µA	0.9 x V_{CCBE}	V_{CCBE}		V
I_{OZ}	High impedance leakage current	OEB set to V_{IH}	-1.67	0	1.67	µA
C_L	Output load capacitance				15	pF

Table 8. Reference voltage

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFP} I V_{REFP} Q	Top internal reference voltage	0.81	0.88	0.94	V
V_{INCM} I V_{INCM} Q	Input common mode voltage	0.41	0.46	0.50	V

Table 9. Power consumption

Symbol	Parameter	Min	Typ	Max	Unit
I_{CCA}	Analog supply current		76	96.5	mA
I_{CCD}	Digital supply current		3.5	4.9	mA
I_{CCBE}	Digital buffer supply current (10 pF load)		6	9.4	mA
I_{CCBI}	Digital buffer supply current		100	440	µA
P_d	Power consumption in normal operation mode		215	271	mW
R_{thja}	Thermal resistance (TQFP48)		80		°C/W

Table 10. Accuracy

Symbol	Parameter	Min	Typ	Max	Unit
OE	Offset error		2.97		LSB
GE	Gain error		0.1		%
DNL	Differential non linearity		±0.52		LSB
INL	Integral non linearity		±3		LSB
-	Monotonicity and no missing codes	Guaranteed			

Table 11. Matching between channels

Symbol	Parameter	Min	Typ	Max	Unit
GM	Gain match		0.04	1	%
OM	Offset match		0.88		LSB
PHM	Phase match		1		dg
XTLK	Crosstalk rejection		85		dB

Figure 3. Static parameter: integral non linearity[a]
F_S = 40 Msps, I_{CCA} = 60 mA, F_{in} = 2 MHz

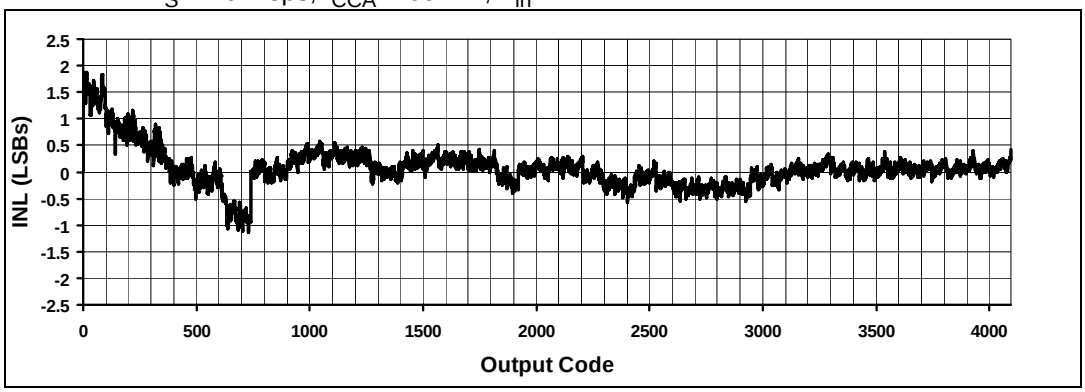
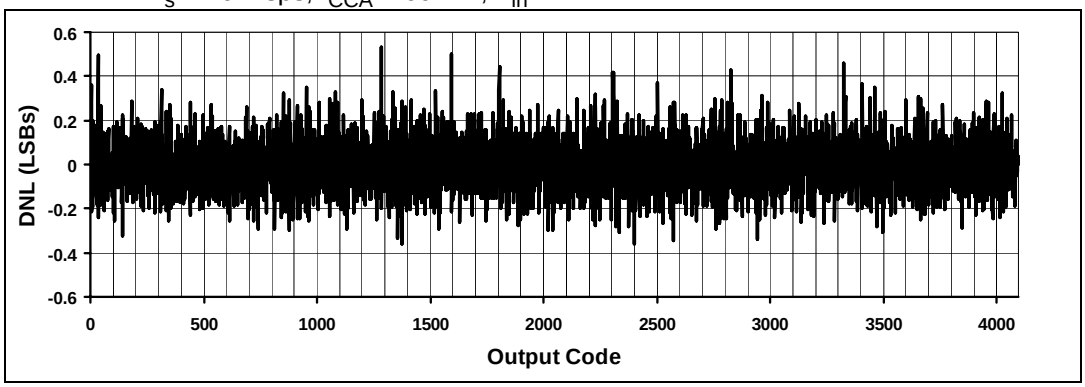


Figure 4. Static parameter: differential non linearity[a]
F_s = 40 Msps, I_{CCA} = 60 mA, F_{in} = 2 MH



a. For parameter definitions, see *Section 10: Definitions of specified parameters on page 25*.

Figure 5. Linearity vs. F_S
F_{in} = 5MHz

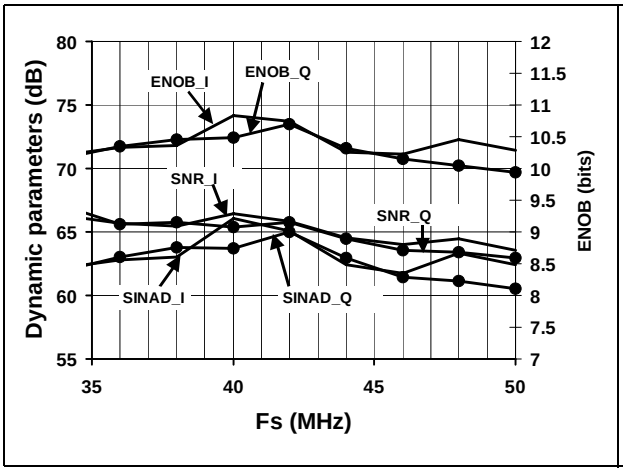


Figure 6. Distortion vs. F_S
F_{in} = 5MHz

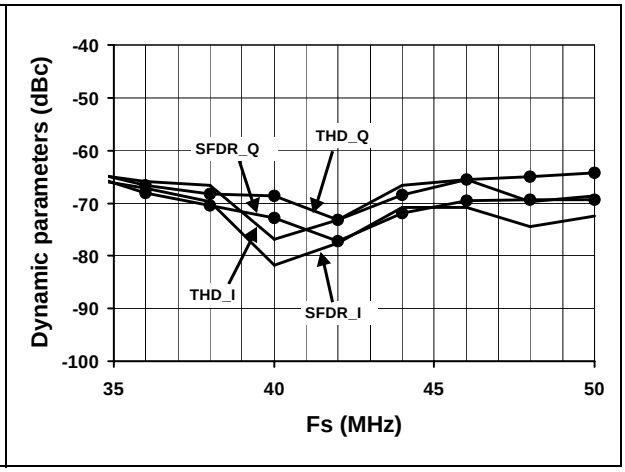


Figure 7. Linearity vs. F_{in}
F_S= 40MHz, I_{CCA} = 60mA

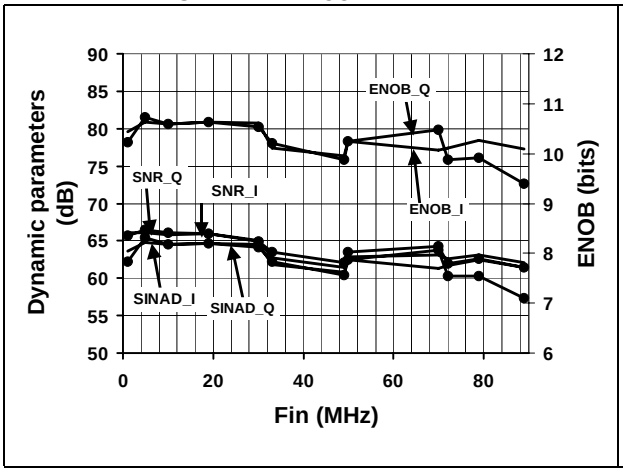


Figure 8. Distortion vs. F_{in}
F_S= 40MHz, I_{CCA} = 60mA

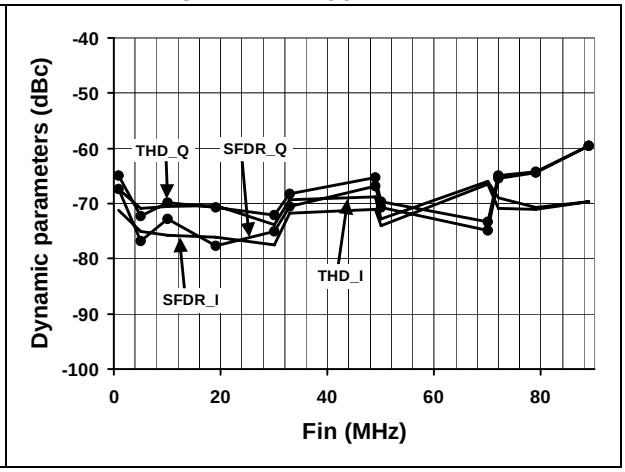


Figure 9. Linearity vs. temperature
F_S=40MHz, I_{CCA}=60mA, F_{in}=2MHz

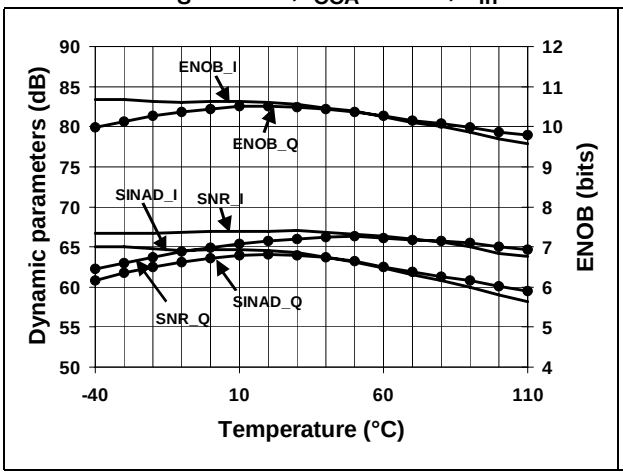


Figure 10. Distortion vs. temperature
F_S=40Msps, I_{CCA}=60mA, F_{in}=2MHz

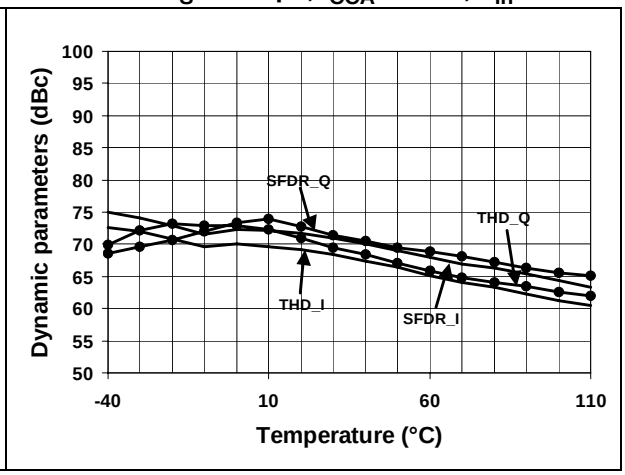


Figure 11. Linearity vs. AV_{CC}
F_S=40Msps, I_{CCA}=60mA, F_{in}=10MHz

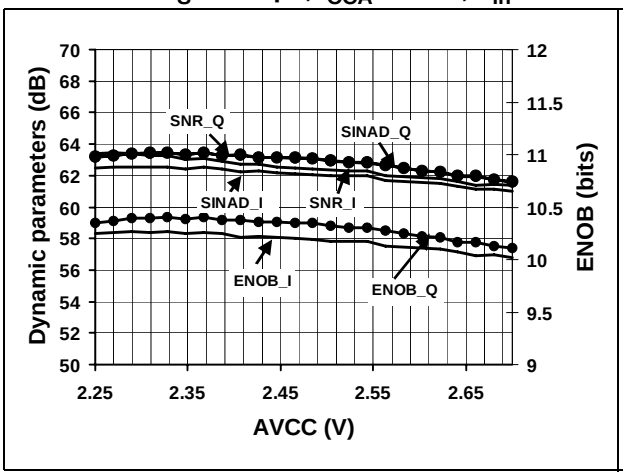


Figure 12. Distortion vs. AV_{CC}
F_S=40Msps, I_{CCA}=60mA, F_{in}=10MHz

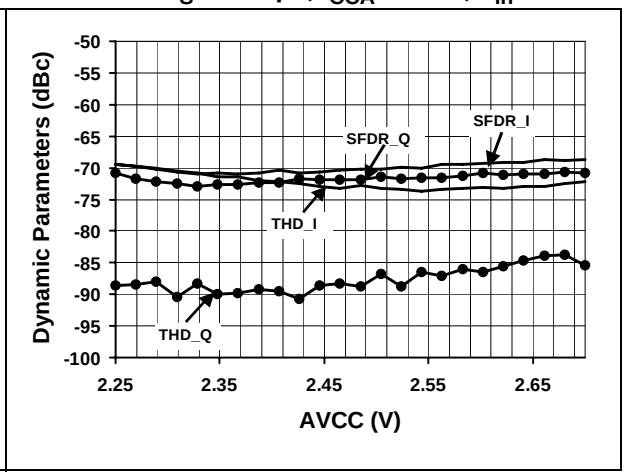


Figure 13. Linearity vs. DV_{CC}
F_S=40Msps, I_{CCA}=60mA, F_{in}=10MHz

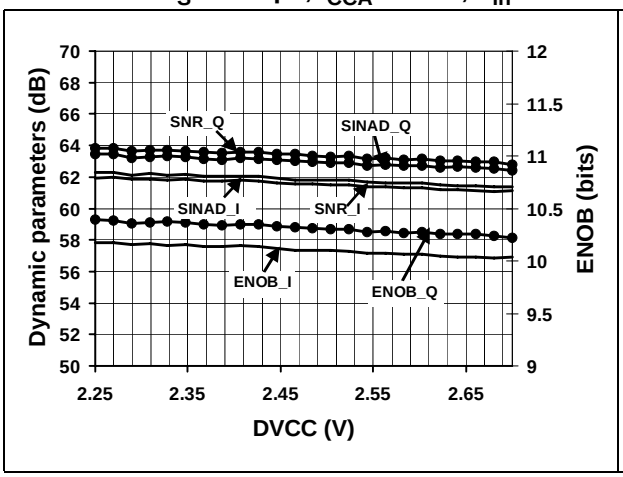


Figure 14. Distortion vs. DV_{CC}
F_S=40Msps, I_{CCA}=60mA, F_{in}=10MHz

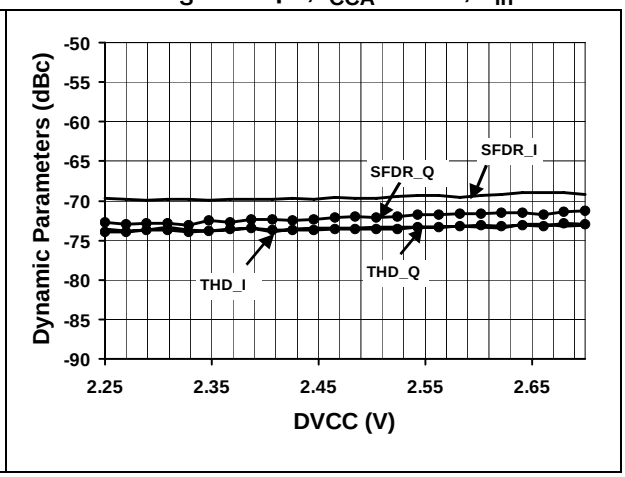


Figure 15. Linearity vs. V_{CCBI}
F_S=40Msps, I_{CCA}=60mA, F_{in}=10MHz

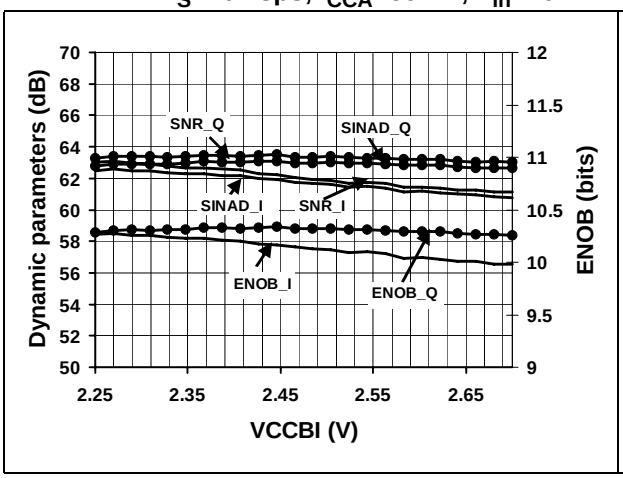


Figure 16. Distortion vs.V_{CCBI}
F_S=40Msps, I_{CCA}=60mA, F_{in}=10MHz

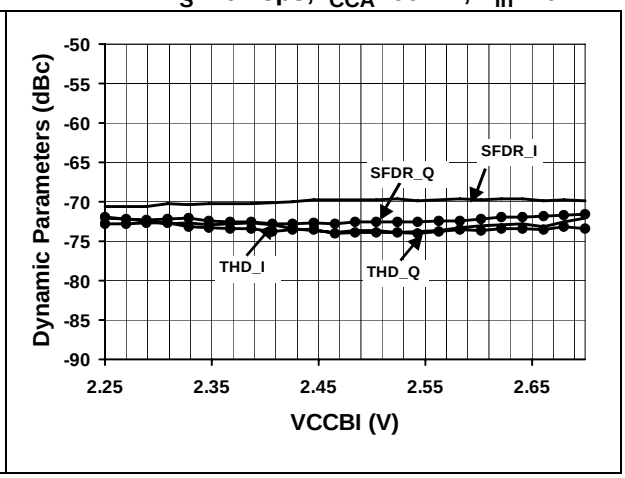


Figure 17. Linearity vs. V_{CCBE}
F_S=40Msps, I_{CCA}=60mA, F_{in}=5MHz

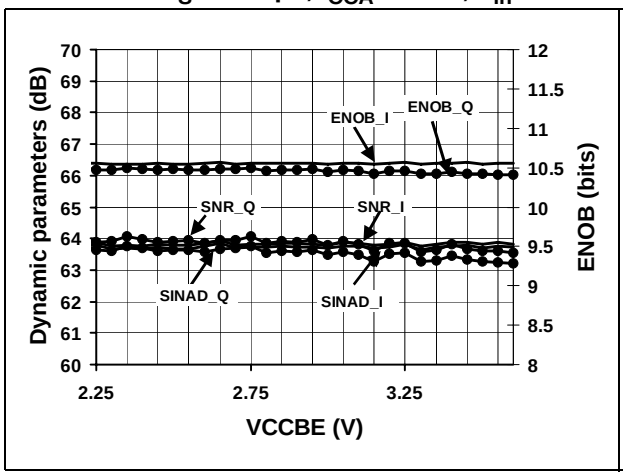


Figure 18. Distortion vs. V_{CCBE}
F_S=40Msps, I_{CCA}=60mA, F_{in}=5MHz

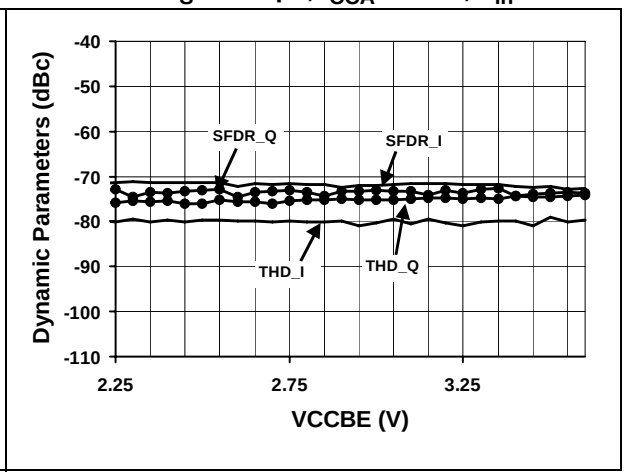


Figure 19. Linearity vs. duty cycle
F_S=40MHz, I_{CCA}=60mA, F_{in}=5MHz

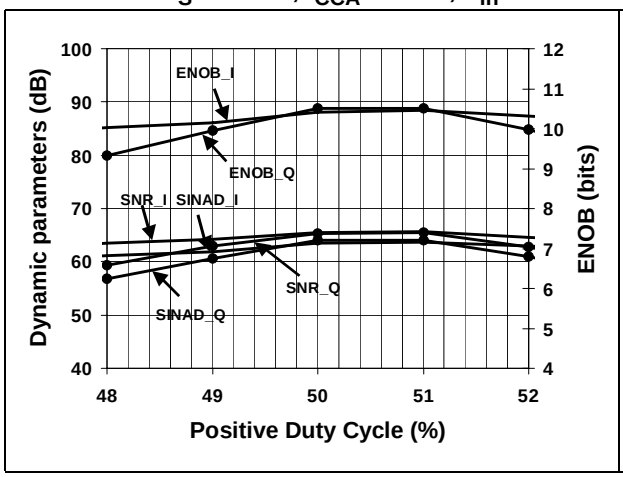


Figure 20. Distortion vs. duty cycle
F_S=40MHz, I_{CCA}=60mA, F_{in}=5MHz

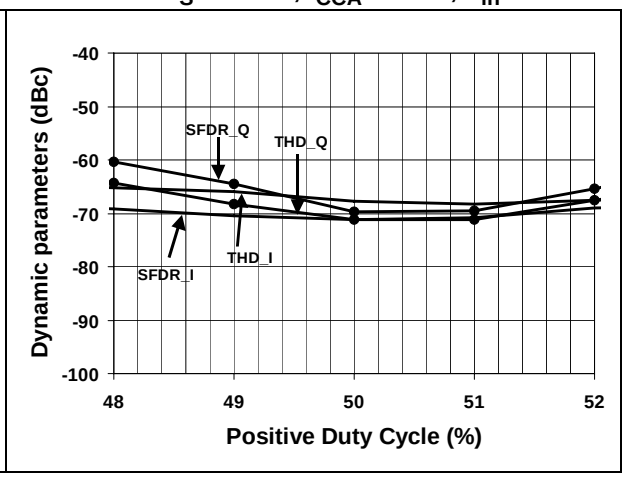


Figure 21. Single-tone 8K FFT at 40 Msps - Channel Q
F_{in} = 5MHz, I_{CCA} = 60mA, V_{in}@-1dBFS

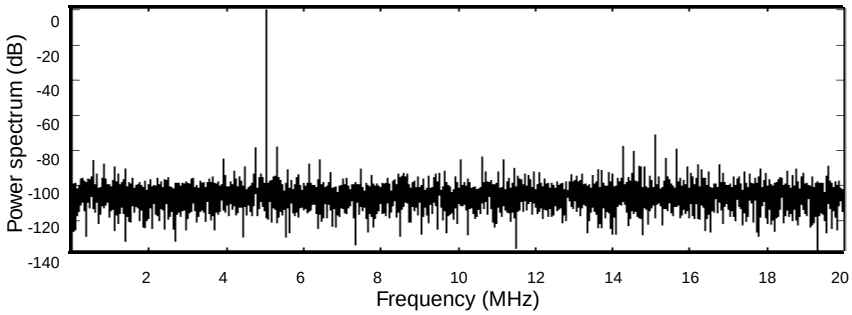
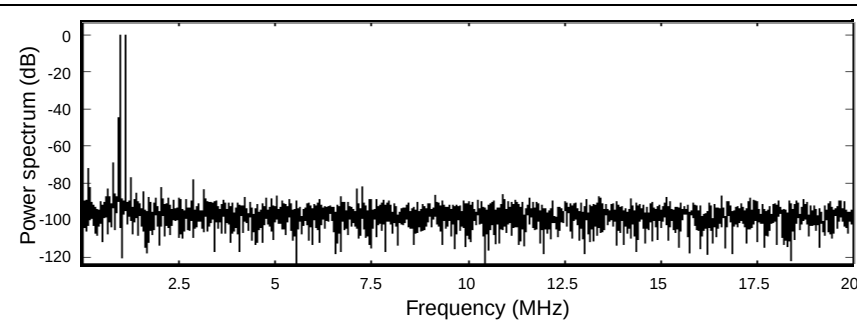


Figure 22. Dual-tone 8K FFT at 40Msps - Channel Q
F_{in1} = 0.93MHz, F_{in2} = 1.11MHz, I_{CCA} = 70mA, V_{in1}@-7dBFS, V_{in2}@-7dBFS, IMD = -69dBc



8 Application information

The TSA1203 is a dual-channel, 12-bit resolution high speed analog-to-digital converter based on a pipeline structure and deep sub-micron CMOS process to achieve the best performance in terms of linearity and power consumption.

Each channel achieves 12-bit resolution through the pipeline structure which consists of 12 internal conversion stages in which the analog signal is fed and sequentially converted into digital data. A latency time of 7 clock periods is necessary to obtain the digitized data on the output bus.

The input signals are simultaneously sampled, for both channels, on the rising edge of the clock. The output data is delivered on the rising edge of the clock for channel I, and on the falling edge of the clock for channel Q, as shown in *Figure 2: Timing diagram on page 4*. The digital data produced at the various stages must be time-delayed according to the order of conversion. Finally, a digital data correction completes the processing and ensures the validity of the ending codes on the output bus.

The TSA1203 is pin-to-pin compatible with the dual 10 bits/20 Msps TSA1005-20, the dual 10 bits /40 Msps TSA1005-40 and the dual 12 bits/ 20 Msps TSA1204.

8.1 Additional functions

To simplify the application board as much as possible, the following operating modes are provided:

- Output enable (OEB) mode
- Select mode

8.1.1 Output enable mode (OEB)

When set to low level (V_{IL}), all digital outputs remain active and are in low impedance state. When set to high level (V_{IH}), all digital output buffers are in high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data arrives on the output with a very short T_{on} delay. This mechanism allows the chip select of the device.

Figure 2: Timing diagram on page 4 summarizes this functionality.

If you do not want to use OEB mode, the OEB pin should be grounded through a low value resistor.

8.1.2 Select mode (SELECT)

The digital data output from each of the ADC cores is multiplexed to share the same output bus. This prevents an increase in the number of pins and allows to use the same package as for a single-channel ADC like the TSA1201.

The information channel is selected with the "SELECT" pin. When set to high level (V_{IH}), the channel I data is present on the D0-D11 output bus. When set to low level (V_{IL}), the channel Q data is delivered on D0-D11.

By connecting SELECT to CLK, channel I and channel Q are simultaneously present on D0-D11, channel I on the rising edge of the clock and channel Q on the falling edge of the clock. (refer to *Figure 2: Timing diagram on page 4*).

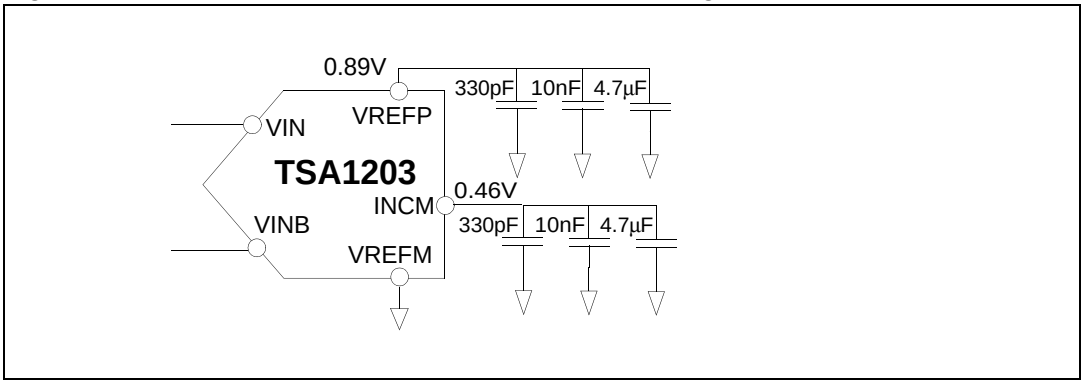
8.2 References and common mode connection

VREFM must always be connected directly to ground externally for most applications.

8.2.1 Internal reference and common mode

In the default configuration, the ADC operates with its own reference and common mode voltages generated by its internal bandgap. It is recommended to decouple the VREFP and INCM pins in order to minimize low and high frequency noise (see *Figure 23*).

Figure 23. Internal reference and common mode setting



8.2.2 External reference and common mode

Each of the voltages V_{REFP}, V_{REFM} and INCM can be fixed externally to better fit the application needs (refer to *Table 5: Operating conditions on page 7* for min/max values). It is possible to use an external reference voltage device for specific applications requiring even better linearity, accuracy or enhanced temperature behavior.

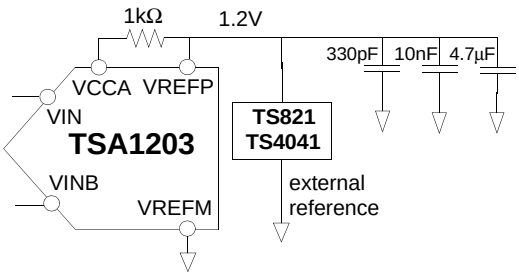
The V_{REFP} and V_{REFM} voltages set the analog dynamic range at the input of the converter that has a full scale amplitude of $2*(V_{REFP}-V_{REFM})$.

The INCM voltage is half the value of $V_{REFP}-V_{REFM}$.

The best signal-to-noise performance is achieved with a dynamic range at its maximum value. To obtain this, V_{REFM} can be connected to GND, and V_{REFP} can be set up to 1.5 V maximum. However, signal to noise performance is a trade-off with the THD, with a possibility of degraded THD under these conditions.

To obtain the highest performance from the TSA1203 device, we recommend implementing the configuration shown in *Figure 24* with the STMicroelectronics TS821 or TS4041-1.2 Vref.

Figure 24. External reference setting



8.3 Driving the differential analog inputs

The TSA1203 is designed to deliver optimum performance when driven on differential inputs. An RF transformer is an efficient way of achieving this high performance.

Figure 25 describes the schematics. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs. The common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set to 0.46V. It determines the DC component of the analog signal. Being a high-impedance input, it acts as an I/O and can be externally driven to adjust this DC component. The INCM is decoupled to maintain a low noise level on this node. Our evaluation board is mounted with a 1:1 ADT1-1WT transformer from Mini circuits. You might also use a higher impedance ratio (1:2 or 1:4) to reduce the driving requirement on the analog source.

Each analog input can drive a 1.4 V_{pp} amplitude input signal, so the resulting differential amplitude is 2.8 V_{pp}.

Figure 25. Differential input configuration with transformer

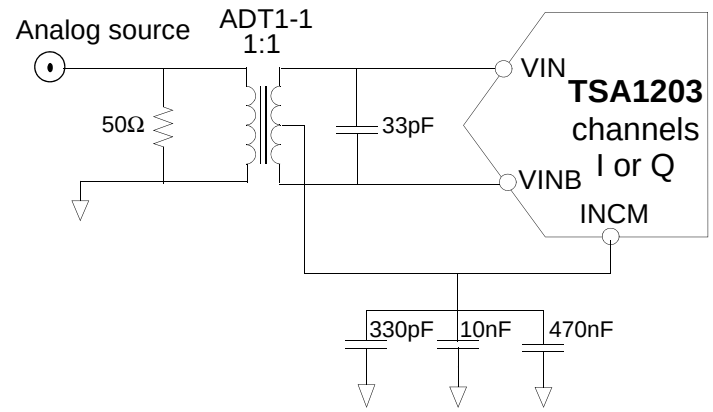


Figure 26. AC-coupled differential input

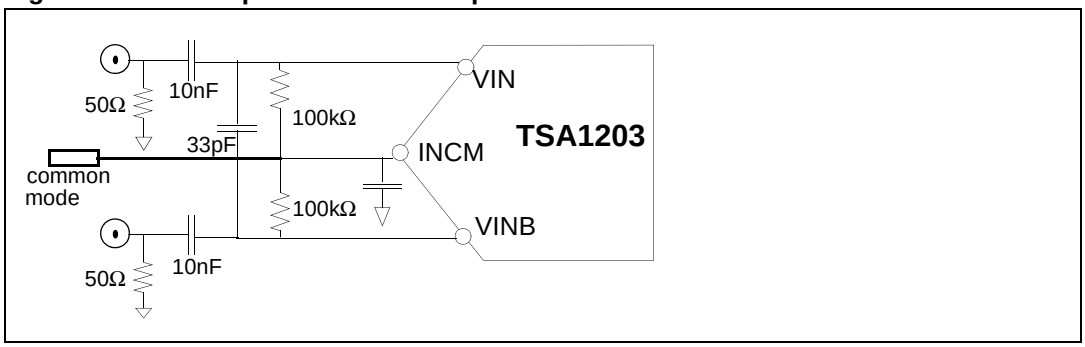


Figure 26 represents the biasing of a differential input signal in an AC-coupled differential input configuration. Both inputs V_{IN} and V_{INB} are centered around the common mode voltage, which can be left internal, or fixed externally.

Figure 27. DC-coupled 2 V_{pp} differential analog input

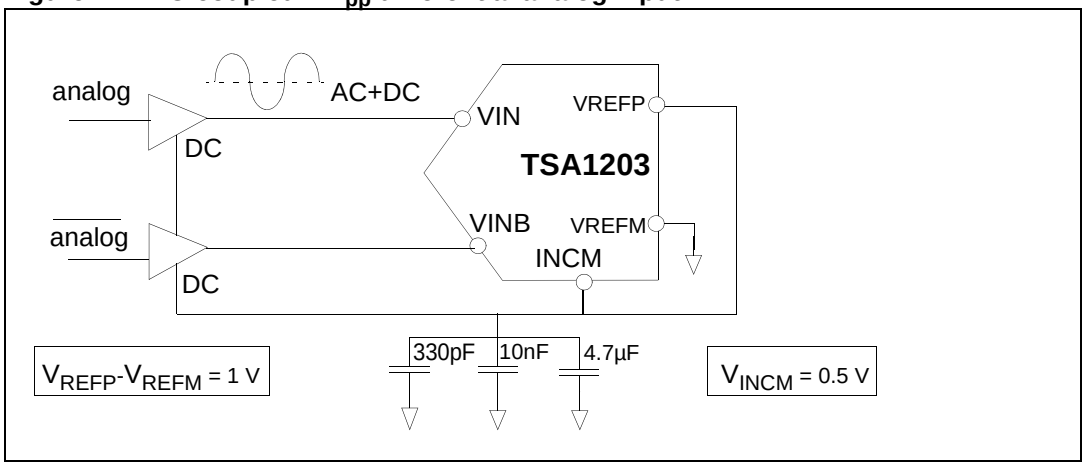


Figure 27 shows a DC-coupled configuration with forced VREFP and INCM to the 1V DC analog input while VREFM is connected to ground; the differential amplitude obtained is 2 V_{pp}.

8.4 Clock input

The quality of your TSA1203 converter is very dependent on your clock input accuracy, in terms of aperture jitter; the use of a low jitter crystal controlled oscillator is recommended.

Further points to consider in your implementation are:

- The duty cycle must be between 45% and 55%.
- The clock power supplies must be independent from the ADC output supplies to avoid digital noise modulation on the output.
- When powered-on, the circuit needs several clock periods to reach its normal operating conditions. Therefore, it is recommended to keep the circuit clocked to avoid random states before applying the supply voltages.

8.5 Power consumption optimization

The internal architecture of the TSA1203 makes it possible to optimize power consumption according to the sampling frequency of the application. For this purpose, an external resistor is placed between IPOL and the analog ground pins. Therefore, the total dissipation can be optimized over the full sampling range (0.5 Msps to 40 Msps).

The TSA1203 combines the highest performance with the lowest consumption at 40 Msps when R_{pol} is equal to 18 kΩ This value is nevertheless dependent on the application and the environment.

In the lower sampling frequency range, this value of resistor may be adjusted in order to decrease the analog current without any degradation of dynamic performance.

Table 12 gives some values to illustrate this.

Table 12. Total power consumption optimization depending on R_{pol} value

F_S (Msps)	30	35	40
R_{pol} (kΩ)	38	28	18
Optimized power (mW)	145	180	215

8.6 Layout precautions

To use the ADC circuits most efficiently at high frequencies, some precautions have to be taken for power supplies:

- The implementation of 4 proper separate supplies and ground planes (analog, digital, internal and external buffer ones) on the PCB is mandatory for high speed circuit applications to provide low inductance and low resistance common return.

  The separation of the analog signal from the digital output part is essential to prevent noise from coupling onto the input signal. The best compromise is to connect AGND, DGND, GNDBI in a common point whereas GNDBE must be isolated. Similarly, the AVCC, DVCC and VCCBI power supplies must be separate from the VCCBE power supply.
- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.
- All inputs and outputs must be properly terminated with output termination resistors; thus, the amplifier load is resistive only and the stability of the amplifier is improved. All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.
- To keep the capacitive loading as low as possible at digital outputs, short lead lengths of routing are essential to minimize currents when the output changes. To minimize this output capacitance, use buffers or latches close to the output pins.
- Choose component sizes as small as possible (SMD).

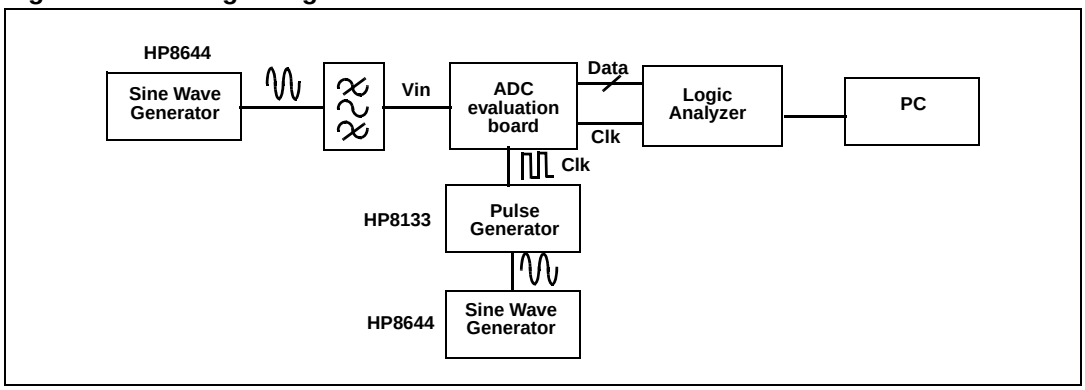
8.7 EVAL1203/BA evaluation board

The EVAL1203/BA is a 4-layer board with high decoupling and grounding level. The schematic of the board is shown in *Figure 30* and its top overlay view in *Figure 29*. The board has been characterized with a fully devoted ADC test bench as shown in *Figure 28*.

All characterization measurements are made with:

- SFSR=1 dB for static parameters,
- SFSR=-1 dB for dynamic parameters.

Figure 28. Analog to digital converter characterization bench



Note: The analog input signal must be filtered to be very pure. The dataready signal is the acquisition clock of the logic analyzer. The ADC digital outputs are latched by the octal buffers 74LCX573.

Figure 29. Evaluation board printed circuit

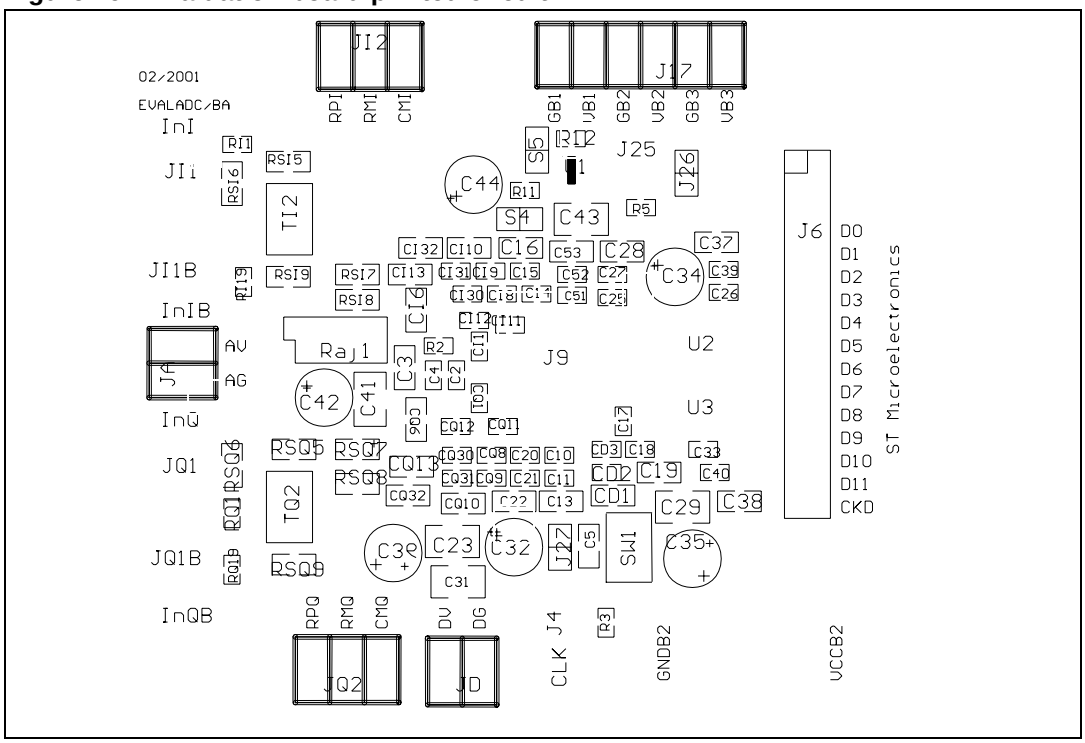


Figure 30. TSA1203 evaluation board schematic

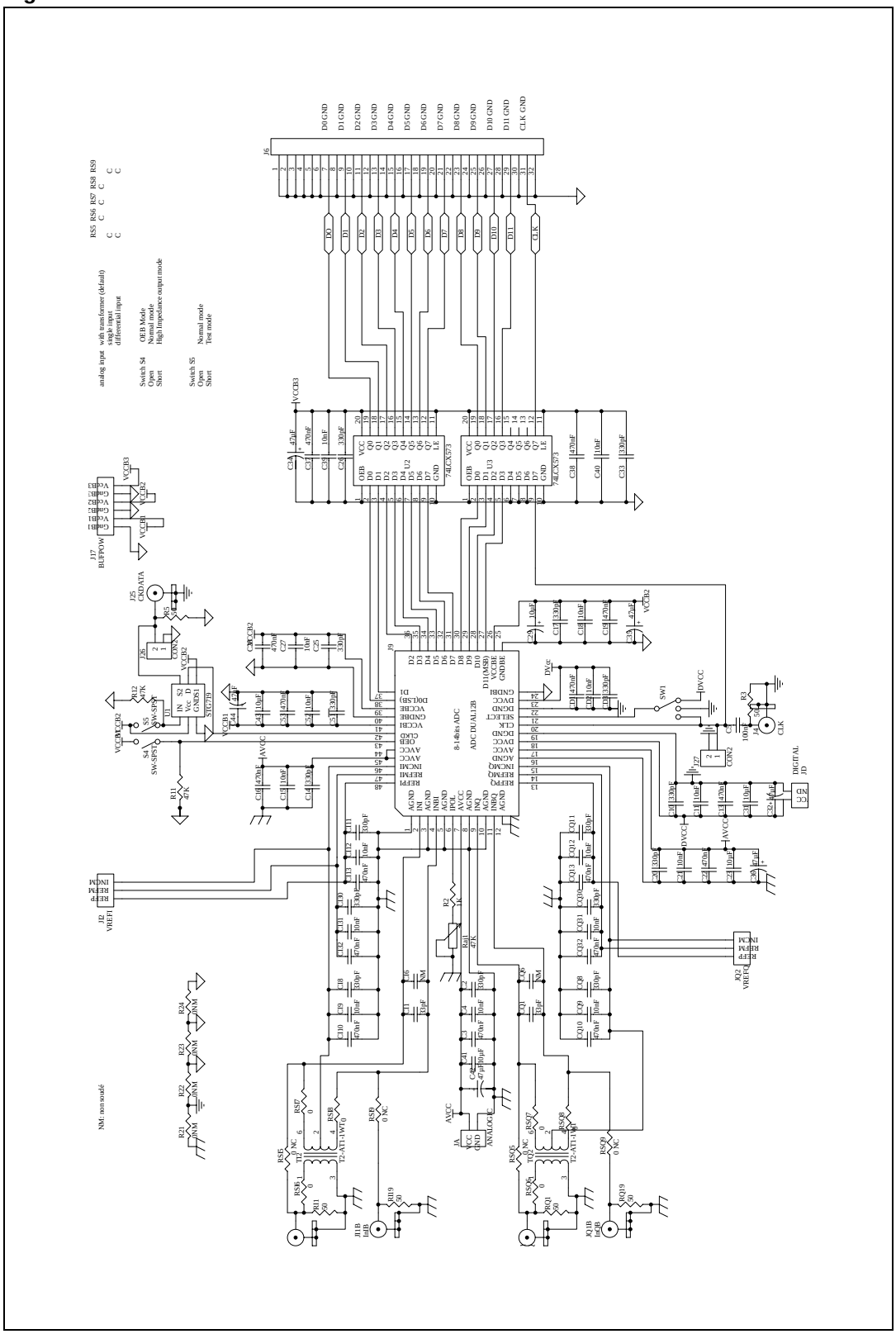


Table 13. Printed circuit board — list of components

Name	Part Type	Footprint	Name	Part Type	Footprint	Name	Part Type	Footprint	Name	Part Type	Footprint
RSQ6	0	805	CD2	10nF	603	C26	330pF	603	CQ6	NC	805
RSQ7	0	805	C40	10nF	603	C20	330pF	603	CI6	NC	805
RSQ8	0	805	C39	10nF	603	C33	330pF	603	U2	74LCX573	TSSOP20
RSI6	0	805	CQ12	10nF	603	C25	330pF	603	U3	74LCX573	TSSOP20
RSI7	0	805	CQ9	10nF	603	CI1	33pF	603	U1	STG719	SOT23-6
RSI8	0	805	C52	10nF	603	CQ1	33pF	603	JA	ANALOGIC	connector
R3	47	603	C18	10nF	603	C34	47µF	RB.1	J17	BUFPOW	connector
R5	47	603	C21	10nF	603	C42	47µF	RB.1	J25	CKDATA	SMA
RQ19	47	603	C4	10nF	603	C35	47µF	RB.1	J4	CLK	SMA
RI1	47	603	C15	10nF	603	C44	47µF	RB.1	J27	CON2	SIP2
RQ1	47	603	C27	10nF	603	C36	47µF	RB.1	J26	CON2	SIP2
RI19	47	603	C11	10nF	603	C32	47µF	RB.1	JD	DIGITAL	connector
RSI9	0NC	805	CI9	10nF	603	C37	470nF	805	JI1	InI	SMA
RSQ5	0NC	805	CI12	10nF	603	CQ10	470nF	805	JI1B	InIB	SMA
RSQ9	0NC	805	CI31	10nF	603	C28	470nF	805	JQ1	InQ	SMA
RSI5	0NC	805	CQ31	10nF	603	CI10	470nF	805	JQ1B	InQB	SMA
R24	0NC	805	CQ30	330pF	603	CQ32	470nF	805	SW1	SWITCH	connector
R23	0NC	805	CI11	330pF	603	CQ13	470nF	805	S5	SW-SPST	connector
R21	0NC	805	C51	330pF	603	CI32	470nF	805	S4	SW-SPST	connector
R22	0NC	805	C2	330pF	603	C13	470nF	805	TI2	T2-AT1-1WT	ADT
R2	1K	603	C17	330pF	603	C53	470nF	805	TQ2	T2-AT1-1WT	ADT
R12	47K	603	CD3	330pF	603	C16	470nF	805	JI2	VREFI	connector
R11	47K	603	C10	330pF	603	C3	470nF	805	JQ2	VREFQ	connector
Raj1	200K	VR5	CQ8	330pF	603	C22	470nF	805	J6	32Pin	IDC-32
		trimmer	CQ11	330pF	603	CI13	470nF	805			connector
C23	10µF	1210	CI8	330pF	603	C38	470nF	805			
C41	10µF	1210	C14	330pF	603	CD1	470nF	805		NC: non soldered	
C29	10µF	1210	CI30	330pF	603	C19	470nF	805			

8.7.1 Evaluation board operating conditions

Table 14. Board connections for power supplies and other pins

Board marking	Connection	Internal voltage (V)	External voltage (V)
AV	AVCC		2.5
AG	AGND		0
RPI	REFPI	0.89	<1.4
RMI	REFMI		<0.4
CMI	INCMI	0.46	<1
RPQ	REFPQ	0.89	<1.4
RMQ	REFMQ		<0.4
CMQ	INCMQ	0.46	<1
DV	DVCC		2.5
DG	DGND		0
GB1	GNDBI		0
VB1	VCCBI		2.5
GB2	GNDBE		0

Table 14. Board connections for power supplies and other pins (continued)

Board marking	Connection	Internal voltage (V)	External voltage (V)
VB2	VCCBE		2.5/3.3
GB3	GNDB3		0
VB3	VCCB3		2.5

Caution: Do not use the VB3 power supply (5 V) dedicated to the 74LCX573 external buffers to supply the VB2 of the TSA1203 which cannot exceed 3.3 V.

8.7.2 Consumption adjustment

Before beginning characterization tests, make sure to adjust the R_{pol} (Raj1), and therefore I_{pol} value, according to your sampling frequency.

8.7.3 Single and differential inputs

The test board can be driven on a single analog input, or on differential inputs. With a single analog input, you must use the ADT1-1WT transformer to generate a differential signal. In this configuration, the resistors RSI6, RSI7, RSI8 for channel I (respectively RSQ6, RSQ7, RSQ8 for channel Q) are connected as short-circuits whereas RSI5, RSI9 (respectively RSQ5, RSQ9 for channel Q) are open circuits.

Alternatively, you can use the JI1 and JI1B differential inputs. In this case, the resistances RSI5, RSI9 for channel I (respectively RSQ5, RSQ9 for channel Q) are connected as short-circuits whereas RSI6, RSI7, RSI8 (respectively RSQ6, RSQ7, RSQ8 for channel Q) are open circuits.

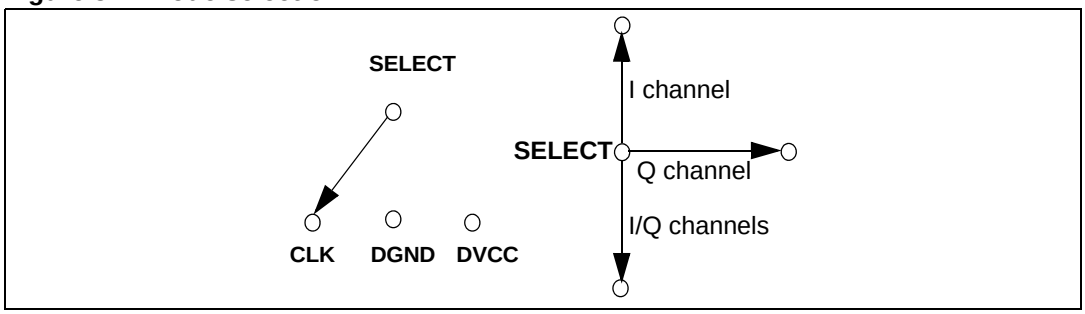
8.7.4 Mode selection

In order to select the channel you want to evaluate, you must set a jumper on the board in the relevant position for the SELECT pin (see *Figure 31*).

The channels selected depend on the position of the jumper:

- With the jumper connected to the upper connectors, channel I at the output is selected.
- With the jumper connected horizontally, channel Q at the output is selected.
- With the jumper connected to the lower connectors, both channels are selected, relative to the clock edge.

Figure 31. Mode selection



9 Practical application examples

9.1 Digital interface applications

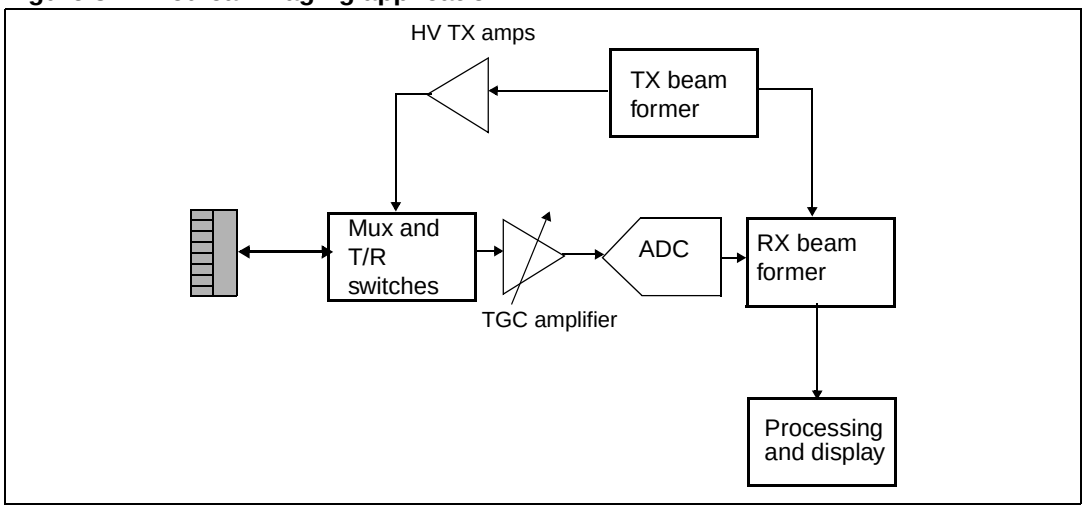
The wide external buffer power supply range of the TSA1203 makes it a perfect choice for plugging into 2.5 V or 3.3 V low voltage DSPs or digital interfaces.

9.2 Medical imaging applications

Driven by the increasing demand for applications requiring either portability or a high degree of parallelism (or both), this product satisfies the requirements of medical imaging and telecom infrastructures.

The typical system diagram in *Figure 32*, shows how a narrow input beam of acoustic energy is sent into a living body via the transducer, and how the energy reflected back is analyzed.

Figure 32. Medical imaging application



The transducer is a piezoelectric ceramic such as zirconium titanate. The whole array can reach up to 512 channels. The TX beam former, amplified by the HV TX amps, delivers up to 100 V amplitude excitation pulses with phase and amplitude shifts. The mux and T/R switch is a two way input signal transmitter/ output receiver.

To compensate for skin and tissues attenuation effects, the time gain compensation (TGC) amplifier is an exponential amplifier that amplifies low voltage signals to the ADC input range. A differential output structure with low noise and very high linearity are essential factors.

These applications need high speed, low power and high performance ADCs. 10-12 bit resolution is necessary to lower the quantification noise. As multiple channels are used, a dual converter is a must for room saving issues.

The input signal is in the range of 2 to 20 MHz (mainly 2 to 7 MHz) and the application uses mostly a 4 over-sampling ratio for spurious free dynamic range (SFDR) optimization.

The next RX beam former and processing blocks enable the analysis of the output channels versus the input beam.

10 Definitions of specified parameters

Static parameters

Static measurements are performed using the histograms method on a 2 MHz input signal, sampled at 50 Msps, which is high enough to fully characterize the test frequency response. The input level is +1 dBFS to saturate the signal.

Differential non linearity (DNL)

The average deviation of any output code width from the ideal code width of 1 LSB.

Integral non linearity (INL)

An ideal converter exhibits a transfer function which is a straight line from the starting code to the ending code. The INL is the deviation from this ideal line for each transition.

Dynamic parameters

Dynamic measurements are performed by spectral analysis, applied to an input sine wave of various frequencies sampled at 40 Msps.

The input level is -1dBFS to measure the linear behavior of the converter. All the parameters are given without correction for the full scale amplitude performance except the calculated ENOB parameter.

Spurious free dynamic range (SFDR)

The ratio between the power of the worst spurious signal (not always an harmonic) and the amplitude of fundamental tone (signal power) over the full Nyquist band. It is expressed in dBc.

Total harmonic distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to noise ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_S/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to noise and distortion ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). It is expressed in dB.

The effective number of bits (ENOB) is easily deduced from the SINAD, using the formula:

SINAD= 6.02 $\times$ ENOB + 1.76 dB.

When the applied signal is not full scale (FS), but has an A_0 amplitude, the SINAD expression becomes:

$SINAD_{2Ao}=SINAD_{Full\ Scale}+ 20\ log\ (2A_0/FS)$

$SINAD_{2A_0}=6.02 \times ENOB + 1.76\ dB + 20\ log\ (2A_0/FS)$

The ENOB is expressed in bits.

Analog input bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3 dB. Higher values can be achieved with smaller input levels.

Effective resolution bandwidth (ERB)

The band of input signal frequencies that the ADC is intended to convert without loosing linearity i.e. the maximum analog input frequency at which the SINAD is decreased by 3dB or the ENOB by 1/2 bit.

Pipeline delay

Delay between the initial sample of the analog input and the availability of the corresponding digital data output, on the output bus. Also called data latency. It is expressed as a number of clock cycles.

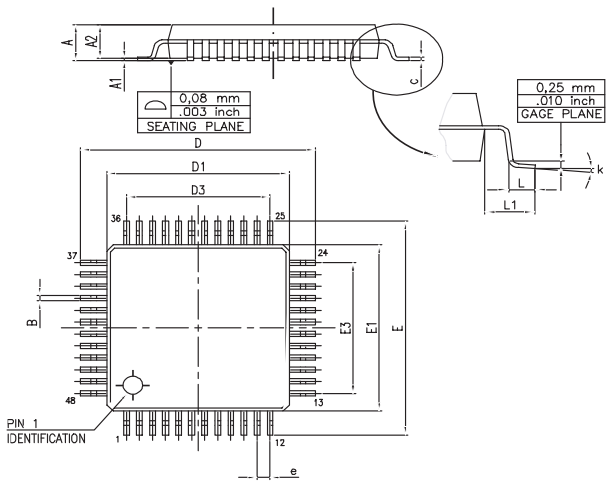
11 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

11.1 TQFP48 package

TQFP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.6			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.0035		0.0079
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.020	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°	3.5°	7°	0°	3.5°	7°



0110596/C

12 Ordering information

Part number	Temperature range	Package	Packing	Marking
TSA1203IFT-E	-40° C to +85° C	TQFP48	Tape & reel	SA1203I
TSA1203IF	-40° C to +85° C	TQFP48	Tray	SA1203I
EVAL1203/BA	Evaluation board			

13 Revision history

Date	Revision	Changes
1-Feb-2003	1	Initial release.
2-Jan-2006	2	Update of dynamic performance measurements in *Table 2 on page 6*.
26-Sep-2006	3	Editorial updates. Reorganized document structure. No technical changes.
12-Dec-2006	4	Pin 42 renamed to CLKD.

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