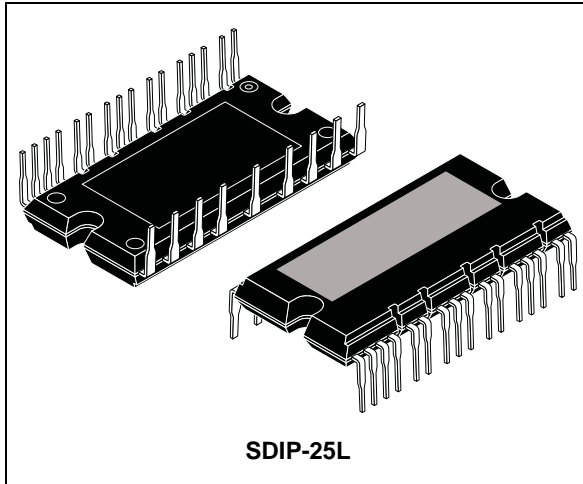


## SLLIMM™ small low-loss intelligent molded module IPM, 3-phase inverter, 14 A, 600 V short-circuit rugged IGBT

Datasheet - production data



### Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners and sewing machines

### Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

### Features

- IPM 14 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$  negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down / pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Shutdown function
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 Vrms/min
- 4.7 kΩ NTC for temperature control
- UL recognized: UL1557 file E81734

**Table 1. Device summary**

| Order code     | Marking      | Package  | Packing |
|----------------|--------------|----------|---------|
| STGIPS14K60T-H | GIPS14K60T-H | SDIP-25L | Tube    |

# Contents

- 1 Internal block diagram and pin configuration ..... 3**
- 2 Electrical ratings ..... 5**
  - 2.1 Absolute maximum ratings ..... 5
  - 2.2 Thermal data ..... 6
- 3 Electrical characteristics ..... 7**
  - 3.1 Control part ..... 9
    - 3.1.1 NTC thermistor ..... 11
  - 3.2 Waveform definitions ..... 12
- 4 Applications information ..... 13**
  - 4.1 Recommendations ..... 14
- 5 Package information ..... 15**
  - 5.1 SDIP-25L package information ..... 15
  - 5.2 Packing information ..... 17
- 6 Revision history ..... 18**

# 1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

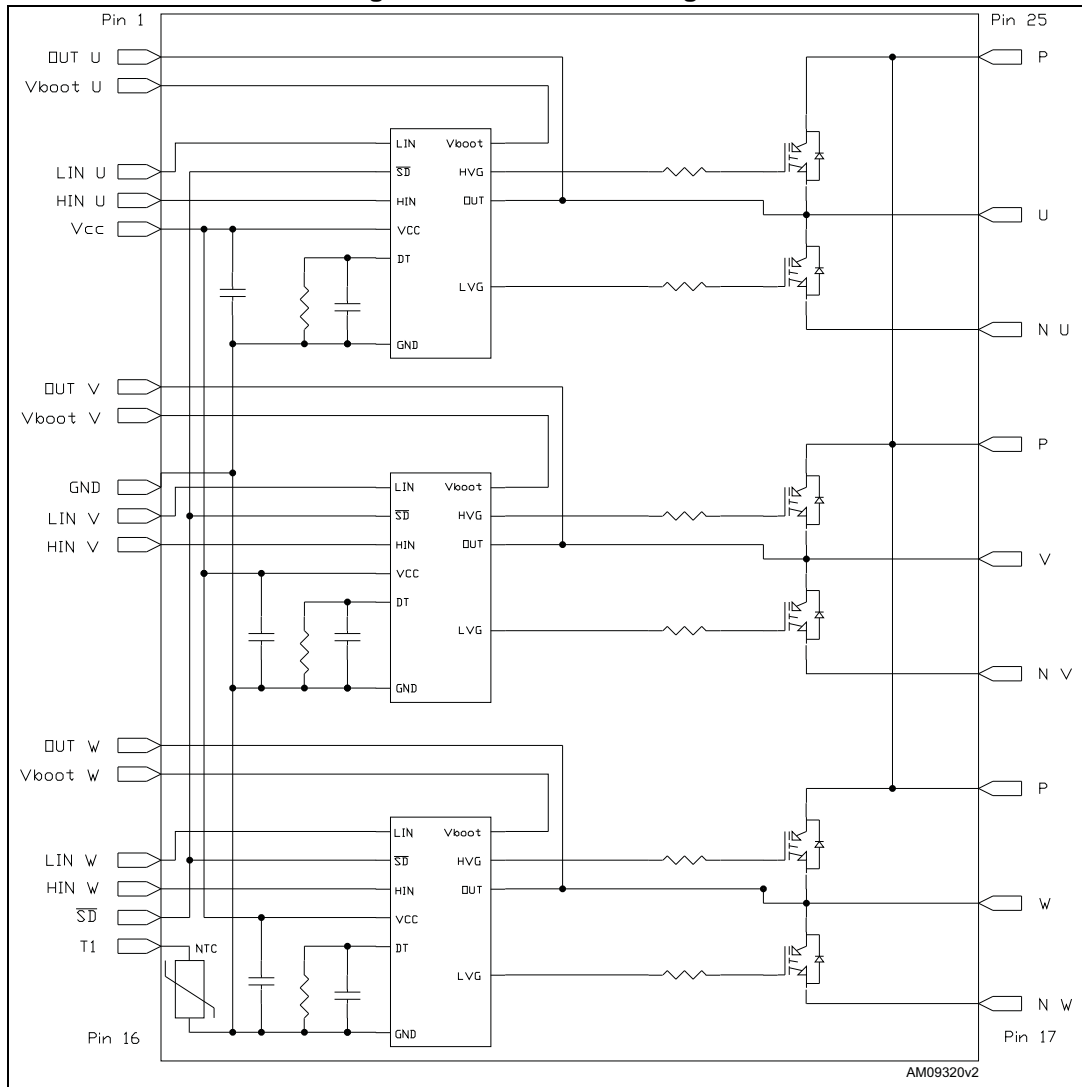
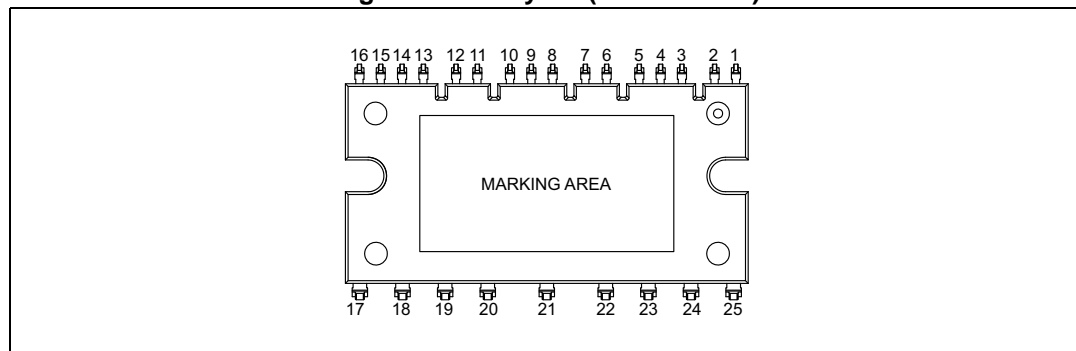


Table 2. Pin description

| Pin n° | Symbol              | Description                            |
|--------|---------------------|--|
| 1      | OUT <sub>U</sub>    | High side reference output for U phase |
| 2      | V <sub>boot U</sub> | Bootstrap voltage for U phase          |
| 3      | LIN <sub>U</sub>    | Low side logic input for U phase       |
| 4      | HIN <sub>U</sub>    | High side logic input for U phase      |
| 5      | V <sub>CC</sub>     | Low voltage power supply               |
| 6      | OUT <sub>V</sub>    | High side reference output for V phase |
| 7      | V <sub>boot V</sub> | Bootstrap voltage for V phase          |
| 8      | GND                 | Ground                                 |
| 9      | LIN <sub>V</sub>    | Low side logic input for V phase       |
| 10     | HIN <sub>V</sub>    | High side logic input for V phase      |
| 11     | OUT <sub>W</sub>    | High side reference output for W phase |
| 12     | V <sub>boot W</sub> | Bootstrap voltage for W phase          |
| 13     | LIN <sub>W</sub>    | Low side logic input for W phase       |
| 14     | HIN <sub>W</sub>    | High side logic input for W phase      |
| 15     | SD                  | Shut down logic input (active low)     |
| 16     | T1                  | NTC thermistor terminal                |
| 17     | N <sub>W</sub>      | Negative DC input for W phase          |
| 18     | W                   | W phase output                         |
| 19     | P                   | Positive DC input                      |
| 20     | N <sub>V</sub>      | Negative DC input for V phase          |
| 21     | V                   | V phase output                         |
| 22     | P                   | Positive DC input                      |
| 23     | N <sub>U</sub>      | Negative DC input for U phase          |
| 24     | U                   | U phase output                         |
| 25     | P                   | Positive DC input                      |

Figure 2. Pin layout (bottom view)



## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Table 3. Inverter part

| Symbol             | Parameter  | Value | Unit          |
|--------------------|--|-------|---------------|
| $V_{PN}$           | Supply voltage applied between P - $N_U$ , $N_V$ , $N_W$   | 450   | V             |
| $V_{PN(surge)}$    | Supply voltage (surge) applied between P - $N_U$ , $N_V$ , $N_W$   | 500   | V             |
| $V_{CES}$          | Each IGBT collector emitter voltage ( $V_{IN}^{(1)} = 0$ )   | 600   | V             |
| $\pm I_C^{(2)}$    | Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$   | 14    | A             |
| $\pm I_{CP}^{(3)}$ | Each IGBT pulsed collector current   | 30    | A             |
| $P_{TOT}$          | Each IGBT total dissipation at $T_C = 25^\circ\text{C}$  | 42    | W             |
| $t_{scw}$          | Short-circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$<br>$T_j = 125^\circ\text{C}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN(1)} = 5\text{ V}$ | 5     | $\mu\text{s}$ |

1. Applied between  $HIN_i$ ,  $LIN_i$  and  $G_{ND}$  for  $i = U, V, W$ .
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature.

Table 4. Control part

| Symbol        | Parameter  | Min.            | Max.             | Unit |
|---------------|--|-----------------|------------------|------|
| $V_{OUT}$     | Output voltage applied between $OUT_U$ , $OUT_V$ , $OUT_W$ - GND | $V_{boot} - 21$ | $V_{boot} + 0.3$ | V    |
| $V_{CC}$      | Low voltage power supply   | - 0.3           | 21               | V    |
| $V_{boot}$    | Bootstrap voltage  | - 0.3           | 620              | V    |
| $V_{IN}$      | Logic input voltage applied between $HIN$ , $LIN$ and GND        | - 0.3           | 15               | V    |
| $V_{SD}$      | Open drain voltage   | - 0.3           | 15               | V    |
| $dV_{OUT}/dt$ | Allowed output slew rate   |                 | 50               | V/ns |

Table 5. Total system

| Symbol    | Parameter   | Value      | Unit             |
|-----------|---|------------|------------------|
| $V_{ISO}$ | Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$ ) | 2500       | V                |
| $T_C$     | Module case operation temperature   | -40 to 125 | $^\circ\text{C}$ |
| $T_J$     | Power chips operating junction temperature  | -40 to 150 | $^\circ\text{C}$ |

## 2.2 Thermal data

**Table 6. Thermal data**

| Symbol     | Parameter  | Value | Unit |
|------------|--|-------|------|
| $R_{thJC}$ | Thermal resistance junction-case single IGBT max.  | 3.0   | °C/W |
|            | Thermal resistance junction-case single diode max. | 5.5   | °C/W |

### 3 Electrical characteristics

T<sub>J</sub> = 25 °C unless otherwise specified.

Table 7. Inverter part

| Symbol  | Parameter  | Test conditions   | Value |      |      | Unit |
|---|--|---|-------|------|------|------|
|   |  |   | Min.  | Typ. | Max. |      |
| V <sub>CE(sat)</sub>                            | Collector-emitter saturation voltage   | V <sub>CC</sub> = V <sub>boot</sub> = 15 V,<br>V <sub>IN</sub> <sup>(1)</sup> = 5 V,<br>I <sub>C</sub> = 7 A  | -     | 2.1  | 2.5  | V    |
|   |  | V <sub>CC</sub> = V <sub>boot</sub> = 15 V,<br>V <sub>IN</sub> <sup>(1)</sup> = 5 V,<br>I <sub>C</sub> = 7 A, T <sub>J</sub> = 125 °C                                       | -     | 1.8  |      |      |
| I <sub>CES</sub>                                | Collector-cut off current (V <sub>IN</sub> <sup>(1)</sup> = 0 "logic state") | V <sub>CE</sub> = 550 V<br>V <sub>CC</sub> = V <sub>boot</sub> = 15 V   | -     |      | 150  | µA   |
| V <sub>F</sub>                                  | Diode forward voltage  | (V <sub>IN</sub> <sup>(1)</sup> = 0 "logic state"),<br>I <sub>C</sub> = 7 A   | -     |      | 2.1  | V    |
| <b>Inductive load switching time and energy</b> |  |   |       |      |      |      |
| t <sub>on</sub>                                 | Turn-on time   | V <sub>DD</sub> = 300 V,<br>V <sub>CC</sub> = V <sub>boot</sub> = 15 V,<br>V <sub>IN</sub> <sup>(1)</sup> = 0 ÷ 5 V<br>I <sub>C</sub> = 7 A (see <a href="#">Figure 4</a> ) | -     | 270  | -    | ns   |
| t <sub>c(on)</sub>                              | Crossover time (on)  |   | -     | 130  | -    |      |
| t <sub>off</sub>                                | Turn-off time  |   | -     | 520  | -    |      |
| t <sub>c(off)</sub>                             | Crossover time (off)   |   | -     | 140  | -    |      |
| t <sub>rr</sub>                                 | Reverse recovery time  |   | -     | 130  | -    |      |
| E <sub>on</sub>                                 | Turn-on switching losses   |   | -     | 150  | -    | µJ   |
| E <sub>off</sub>                                | Turn-off switching losses  |   | -     | 110  | -    |      |

1. Applied between HIN<sub>i</sub>, LIN<sub>i</sub> and GND for i = U, V, W.

Note: t<sub>ON</sub> and t<sub>OFF</sub> include the propagation delay time of the internal drive. t<sub>C(ON)</sub> and t<sub>C(OFF)</sub> are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

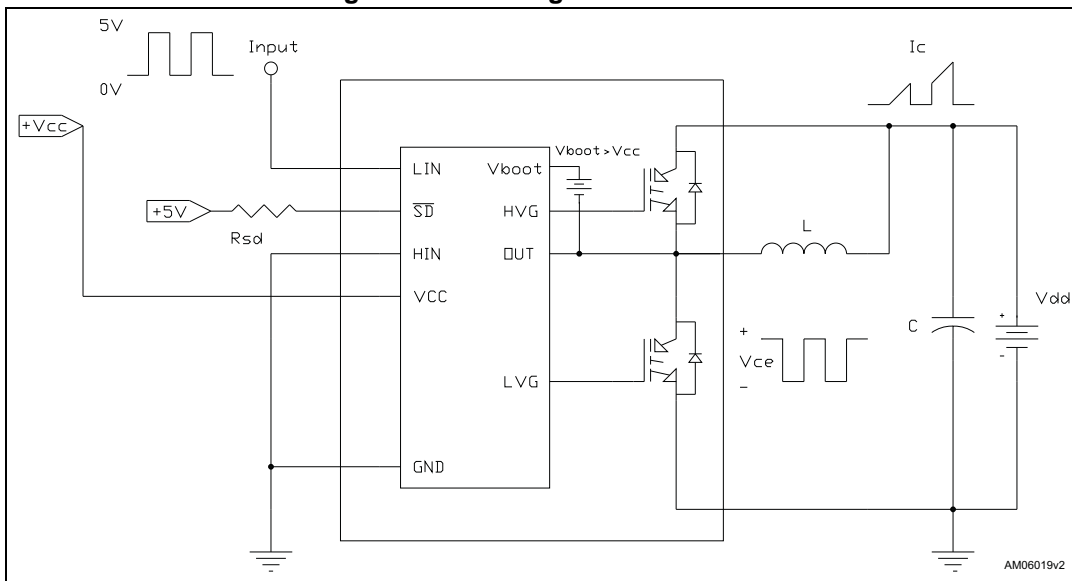
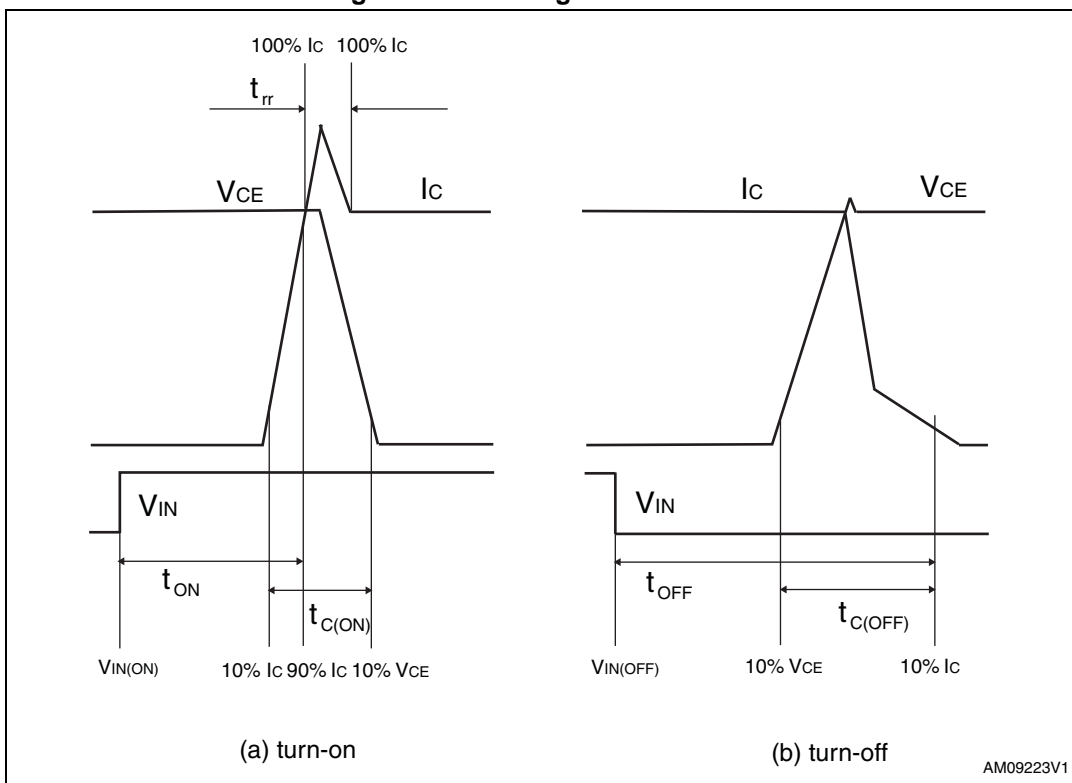


Figure 4. Switching time definition



Note: Figure 4 "Switching time definition" refers to HIN, LIN inputs (active high).



### 3.1 Control part

**Table 8. Low voltage power supply ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

| Symbol          | Parameter                             | Test conditions   | Min. | Typ. | Max. | Unit          |
|-----------------|---------------------------------------|---|------|------|------|---------------|
| $V_{CC\_hys}$   | $V_{CC}$ UV hysteresis                |   | 1.2  | 1.5  | 1.8  | V             |
| $V_{CC\_thON}$  | $V_{CC}$ UV turn ON threshold         |   | 11.5 | 12   | 12.5 | V             |
| $V_{CC\_thOFF}$ | $V_{CC}$ UV turn OFF threshold        |   | 10   | 10.5 | 11   | V             |
| $I_{qccu}$      | Undervoltage quiescent supply current | $V_{CC} = 10\text{ V}$<br>$\overline{SD} = 5\text{ V}$ ; LIN = 0 V;<br>$H_{IN} = 0$ |      |      | 450  | $\mu\text{A}$ |
| $I_{qcc}$       | Quiescent current                     | $V_{CC} = 15\text{ V}$<br>$\overline{SD} = 5\text{ V}$ ; LIN = 0 V<br>$H_{IN} = 0$  |      |      | 3.5  | mA            |

**Table 9. Bootstrapped voltage ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

| Symbol          | Parameter                               | Test conditions   | Min. | Typ. | Max. | Unit          |
|-----------------|---|---|------|------|------|---------------|
| $V_{BS\_hys}$   | $V_{BS}$ UV hysteresis                  |   | 1.2  | 1.5  | 1.8  | V             |
| $V_{BS\_thON}$  | $V_{BS}$ UV turn ON threshold           |   | 11.1 | 11.5 | 12.1 | V             |
| $V_{BS\_thOFF}$ | $V_{BS}$ UV turn OFF threshold          |   | 9.8  | 10   | 10.6 | V             |
| $I_{QBSU}$      | Undervoltage $V_{BS}$ quiescent current | $V_{BS} = 9\text{ V}$<br>$\overline{SD} = 5\text{ V}$ ; LIN = 0<br>$H_{IN} = 5\text{ V}$  |      | 70   | 110  | $\mu\text{A}$ |
| $I_{QBS}$       | $V_{BS}$ quiescent current              | $V_{BS} = 15\text{ V}$<br>$\overline{SD} = 5\text{ V}$ ; LIN = 0<br>$H_{IN} = 5\text{ V}$ |      | 200  | 300  | $\mu\text{A}$ |
| $R_{DS(on)}$    | Bootstrap driver on resistance          | LVG ON  |      | 120  |      | $\Omega$      |

**Table 10. Logic inputs ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

| Symbol     | Parameter                                    | Test conditions               | Min. | Typ. | Max. | Unit          |
|------------|--|-------------------------------|------|------|------|---------------|
| $V_{il}$   | Low logic level voltage                      |                               | 0.8  |      | 1.1  | V             |
| $V_{ih}$   | High logic level voltage                     |                               | 1.9  |      | 2.25 | V             |
| $I_{HINh}$ | HIN logic "1" input bias current             | HIN = 15 V                    | 20   | 40   | 100  | $\mu\text{A}$ |
| $I_{HINI}$ | HIN logic "0" input bias current             | HIN = 0 V                     |      |      | 1    | $\mu\text{A}$ |
| $I_{LINh}$ | LIN logic "1" input bias current             | LIN = 15 V                    | 20   | 40   | 100  | $\mu\text{A}$ |
| $I_{LINI}$ | LIN logic "0" input bias current             | LIN = 0 V                     |      |      | 1    | $\mu\text{A}$ |
| $I_{SDh}$  | $\overline{SD}$ logic "0" input bias current | $\overline{SD} = 15\text{ V}$ | 30   | 120  | 300  | $\mu\text{A}$ |
| $I_{SDI}$  | $\overline{SD}$ logic "1" input bias current | $\overline{SD} = 0\text{ V}$  |      |      | 3    | $\mu\text{A}$ |
| Dt         | Dead time                                    | see <a href="#">Figure 9</a>  |      | 600  |      | ns            |

Table 11. Shut down characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)

| Symbol   | Parameter   | Test conditions                                       | Min. | Typ. | Max. | Unit |
|----------|---|---|------|------|------|------|
| $t_{sd}$ | Shut down to high / low side driver propagation delay | $V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0$ to 3.3 V | 50   | 125  | 200  | ns   |

Table 12. Truth table

| Condition                                | Logic input ( $V_I$ ) |     |     | Output |     |
|--|-----------------------|-----|-----|--------|-----|
|  | SD                    | LIN | HIN | LVG    | HVG |
| Shutdown enable half-bridge tri-state    | L                     | X   | X   | L      | L   |
| Interlocking half-bridge tri-state       | H                     | H   | H   | L      | L   |
| 0 "logic state" half-bridge tri-state    | H                     | L   | L   | L      | L   |
| 1 "logic state" low side direct driving  | H                     | H   | L   | H      | L   |
| 1 "logic state" high side direct driving | H                     | L   | H   | L      | H   |

Note: X: don't care

Figure 5. Maximum  $I_{C(RMS)}$  current vs. switching frequency (1)

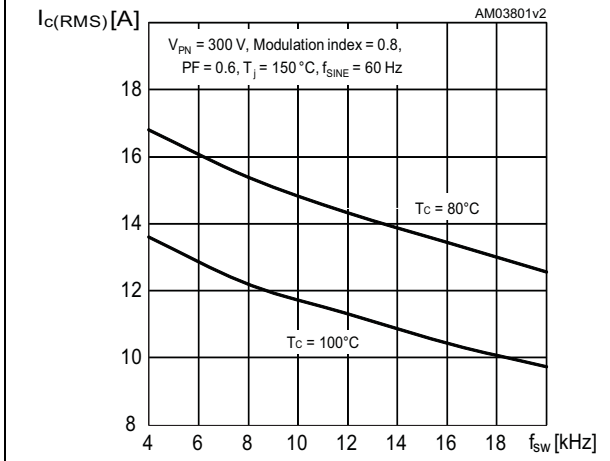
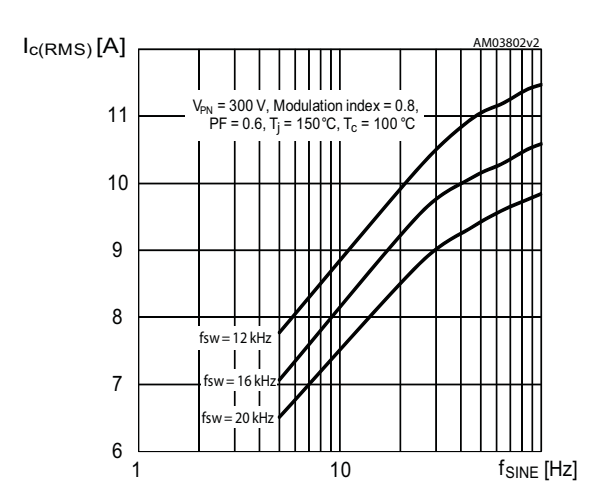


Figure 6. Maximum  $I_{C(RMS)}$  current vs.  $f_{SINE}$  (1)



1. Simulated curves refer to typical IGBT parameters and maximum  $R_{thJC}$ .

3.1.1 NTC thermistor

Table 13. NTC thermistor

| Symbol           | Parameter             | Test conditions  | Min. | Typ. | Max. | Unit. |
|------------------|-----------------------|------------------|------|------|------|-------|
| R <sub>25</sub>  | Resistance            | T = 25°C         |      | 4.7  |      | kΩ    |
| R <sub>125</sub> | Resistance            | T = 125°C        |      | 160  |      | Ω     |
| B                | B-constant            | T = 25°C to 85°C |      | 3950 |      | K     |
| T                | Operating temperature |                  | -40  |      | 150  | °C    |

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B \left( \frac{1}{T} - \frac{1}{298} \right)}$$

Where T are temperatures in Kelvins

Figure 7. NTC resistance vs. temperature

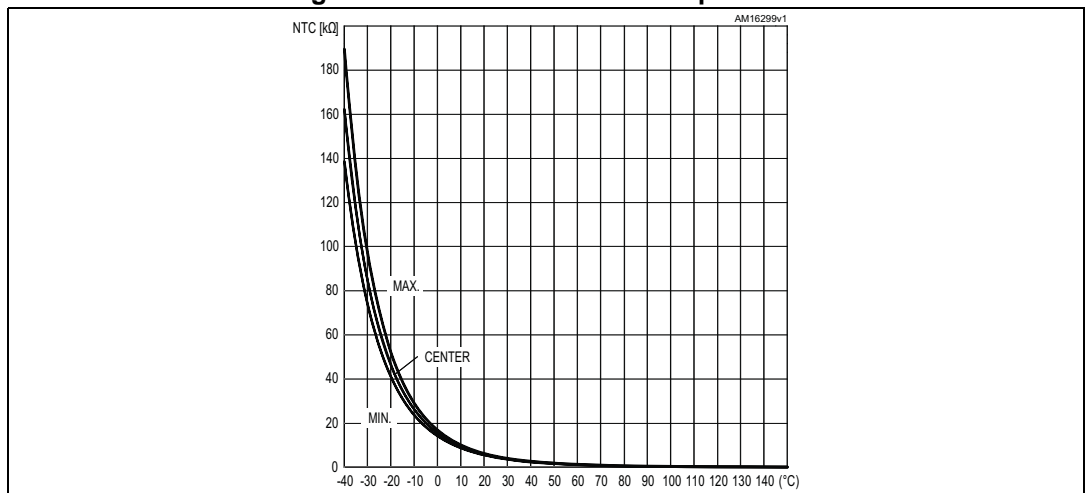
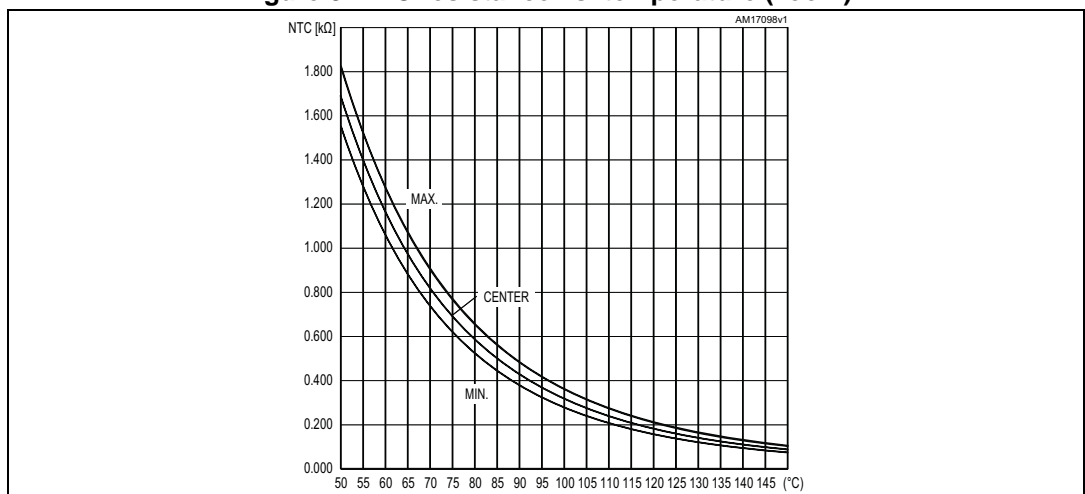
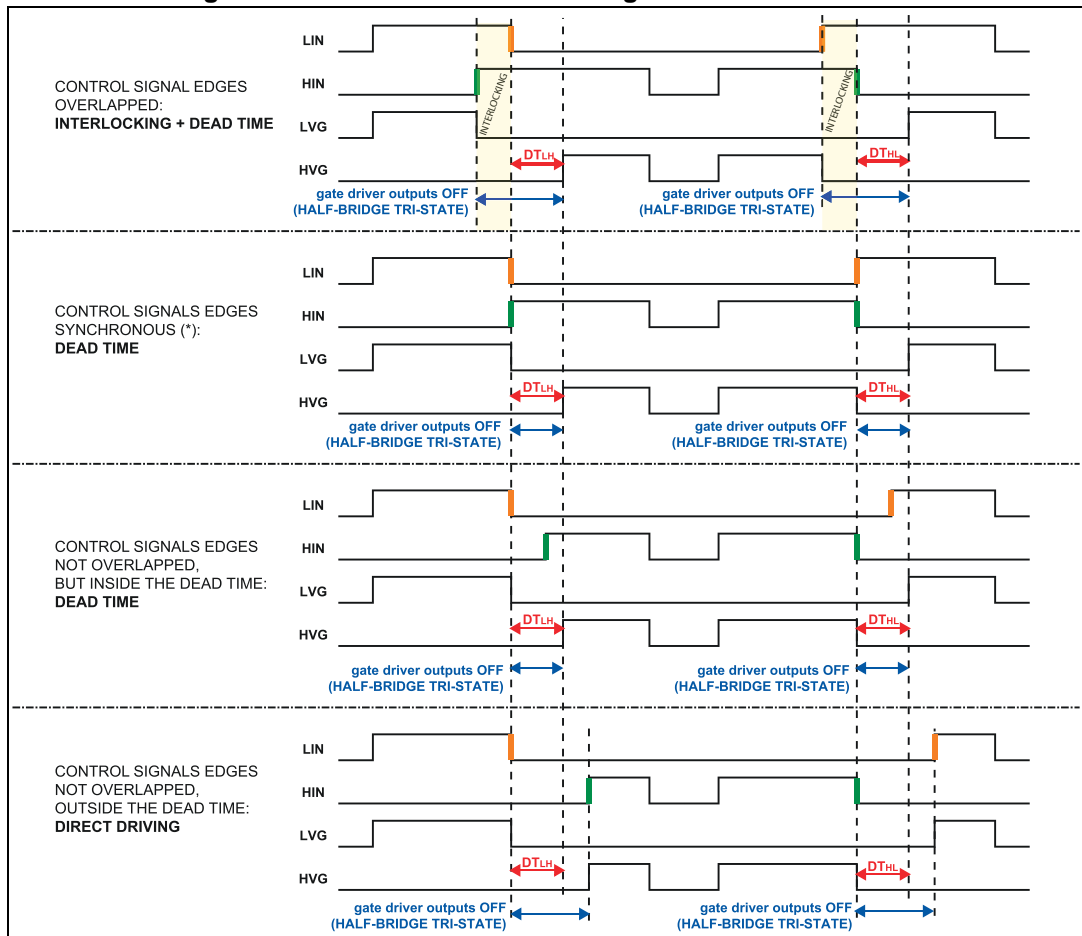


Figure 8. NTC resistance vs. temperature (zoom)



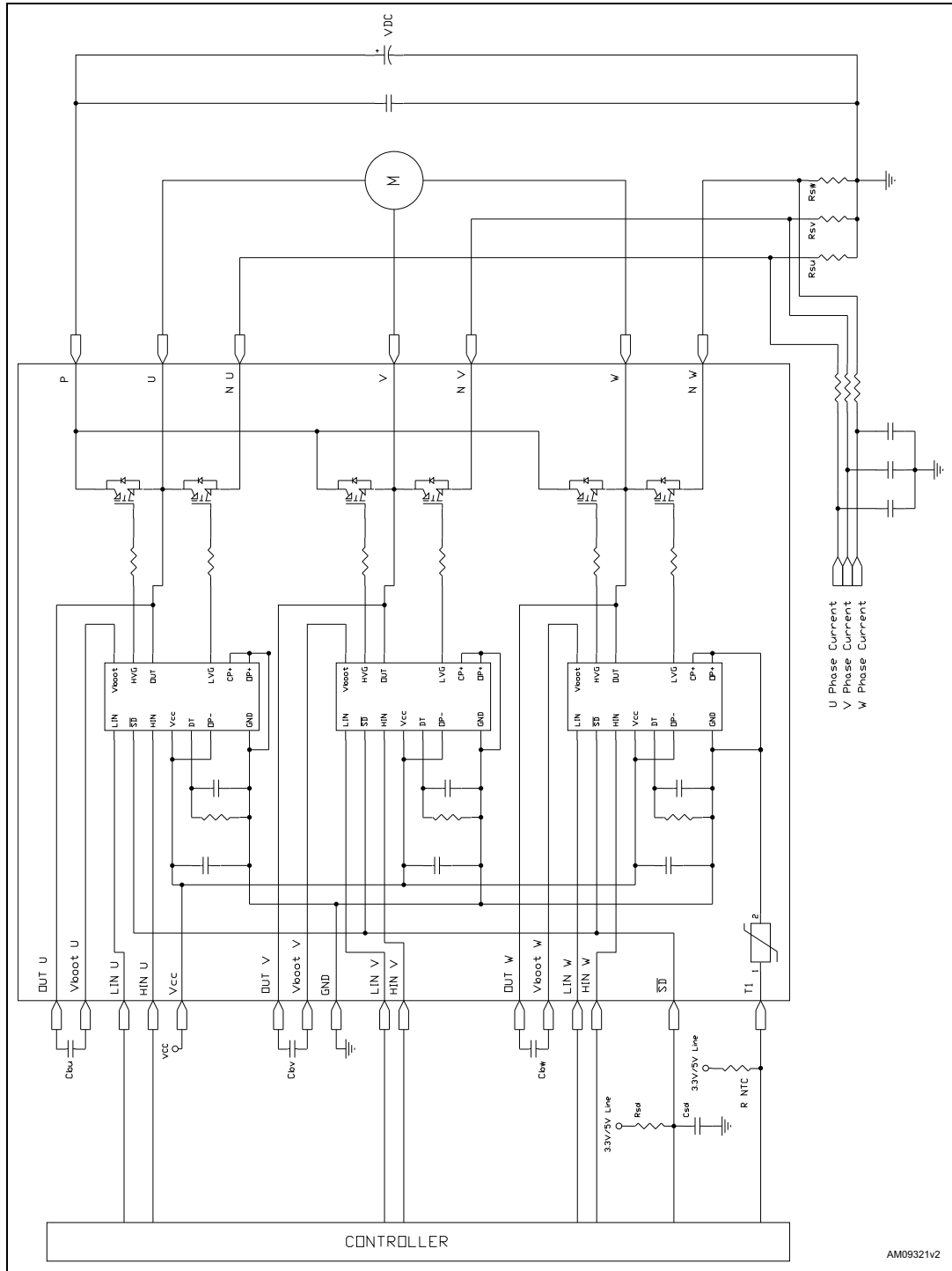
### 3.2 Waveform definitions

Figure 9. Dead time and interlocking waveform definitions



# 4 Applications information

Figure 10. Typical application circuit



## 4.1 Recommendations

- Input signals HIN, LIN are active high logic. A 375 k $\Omega$  (typ.) pull down resistor is built-in for each input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The  $\overline{\text{SD}}$  signal should be pulled up to 5 V / 3.3 V with an external resistor.

**Table 14. Recommended operating conditions**

| Symbol     | Parameter                          | Conditions  | Value |      |      | Unit          |
|------------|------------------------------------|---|-------|------|------|---------------|
|            |                                    |   | Min.  | Typ. | Max. |               |
| $V_{PN}$   | Supply voltage                     | Applied between P-Nu, Nv, Nw                            |       | 300  | 400  | V             |
| $V_{CC}$   | Control supply voltage             | Applied between $V_{CC}$ -GND                           | 13.5  | 15   | 18   | V             |
| $V_{BS}$   | High side bias voltage             | Applied between $V_{BOOTi}$ - $OUT_i$ for $i = U, V, W$ | 13    |      | 18   | V             |
| $t_{dead}$ | Blanking time to prevent arm-short | For each input signal                                   | 1     |      |      | $\mu\text{s}$ |
| $f_{PWM}$  | Pwm input signal                   | -40°C < $T_c$ < 100°C<br>-40°C < $T_j$ < 125°C          |       |      | 20   | kHz           |
| $T_c$      | Case operation temperature         |   |       |      | 100  | °C            |

For further details refer to AN3338.

## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

### 5.1 SDIP-25L package information

Figure 11. SDIP-25L package outline

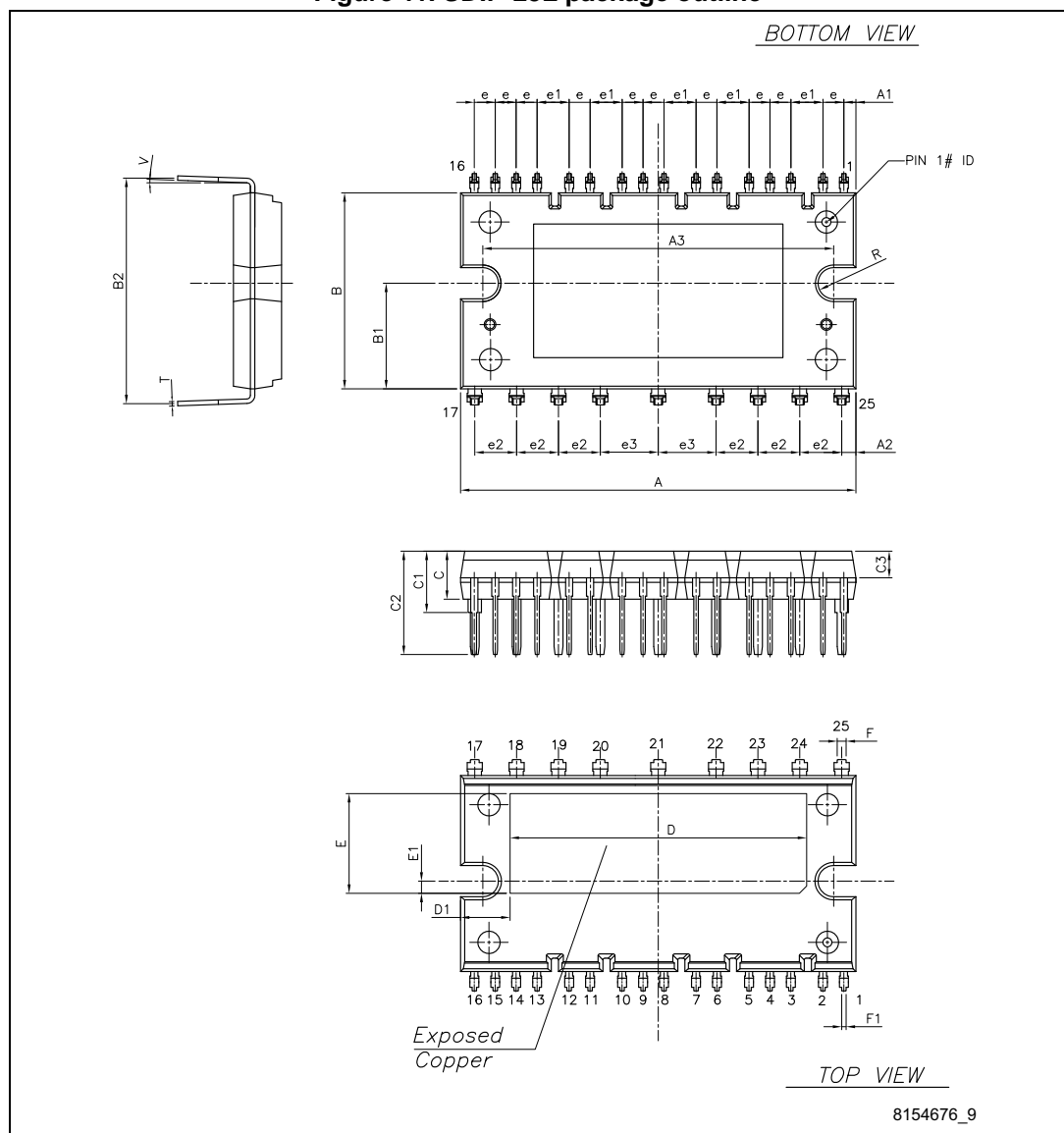


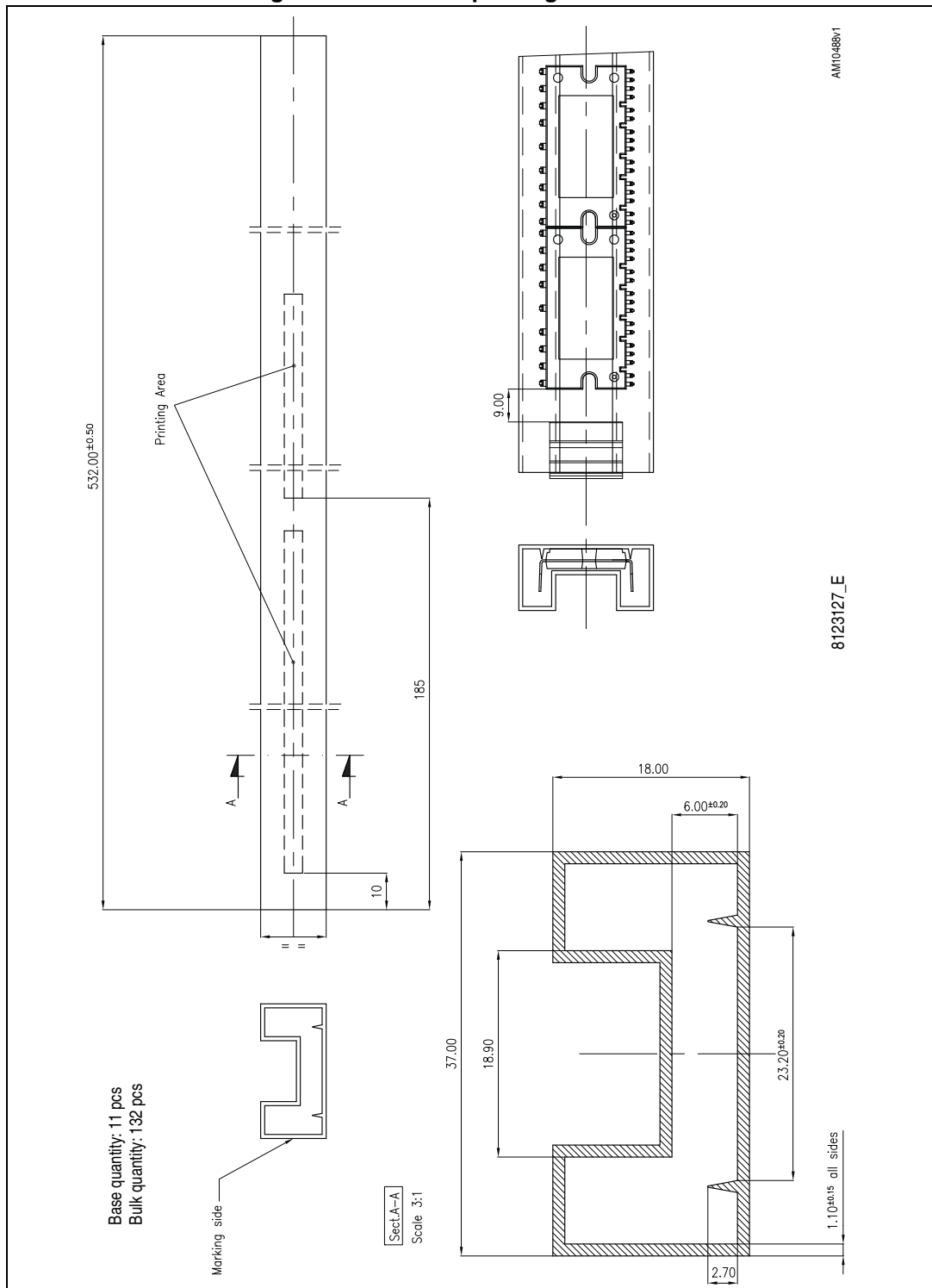
Table 15. SDIP-25L mechanical data

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 43.90 | 44.40 | 44.90 |
| A1   | 1.15  | 1.35  | 1.55  |
| A2   | 1.40  | 1.60  | 1.80  |
| A3   | 38.90 | 39.40 | 39.90 |
| B    | 21.50 | 22.00 | 22.50 |
| B1   | 11.25 | 11.85 | 12.45 |
| B2   | 24.83 | 25.23 | 25.63 |
| C    | 5.00  | 5.40  | 6.00  |
| C1   | 6.50  | 7.00  | 7.50  |
| C2   | 11.20 | 11.70 | 12.20 |
| C3   | 2.90  | 3.00  | 3.10  |
| e    | 2.15  | 2.35  | 2.55  |
| e1   | 3.40  | 3.60  | 3.80  |
| e2   | 4.50  | 4.70  | 4.90  |
| e3   | 6.30  | 6.50  | 6.70  |
| D    |       | 33.30 |       |
| D1   |       | 5.55  |       |
| E    |       | 11.20 |       |
| E1   |       | 1.40  |       |
| F    | 0.85  | 1.00  | 1.15  |
| F1   | 0.35  | 0.50  | 0.65  |
| R    | 1.55  | 1.75  | 1.95  |
| T    | 0.45  | 0.55  | 0.65  |
| V    | 0°    |       | 6°    |



## 5.2 Packing information

Figure 12. SDIP-25L packing information



## 6 Revision history

**Table 16. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 08-Apr-2013 | 1        | Initial release.  |
| 15-Apr-2014 | 2        | Document status promoted from preliminary to production data.<br>Updated <a href="#">Figure 2: Pin layout (bottom view)</a> .   |
| 15-Apr-2015 | 3        | Text edits and formatting changes throughout document<br>Updated <a href="#">Figure 2: Pin layout (bottom view)</a><br>Updated <a href="#">Section 5: Package information</a> |

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