



STGP10NC60H

N-channel 10A - 600V - TO-220
Very fast PowerMESH™ IGBT

Features

Type	V _{CES}	V _{CE(sat)} (Max)@ 25°C	I _C @ 100°C
STGP10NC60H	600V	< 2.5V	10A

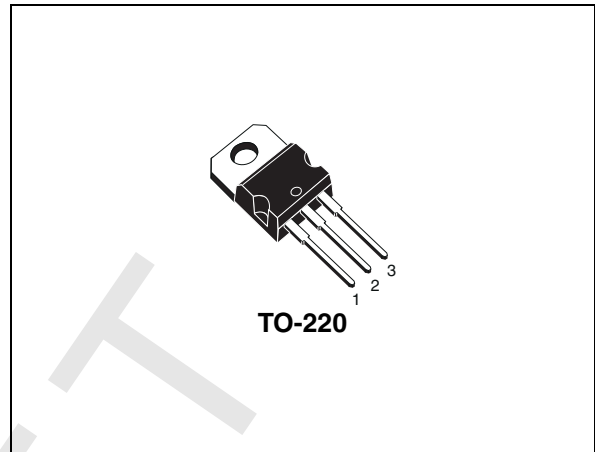
- Low on-voltage drop (V_{cesat})
- Low C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)

Description

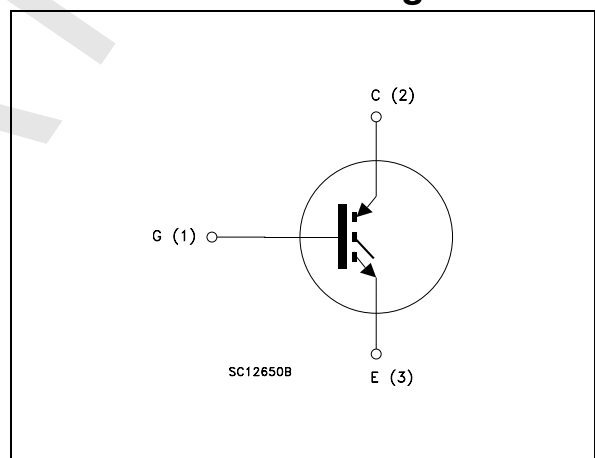
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "H" identifies a family optimized for high frequency applications in order to achieve very high switching performances (reduced t_{fall}) maintaining a low voltage drop.

Applications

- High frequency motor controls
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STGP10NC60H	GP10NC60H	TO-220	Tube

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 9

4 **Package mechanical data** 10

5 **Revision history** 12

DRAFT

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	20	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	10	A
$I_{CL}^{(2)}$	Collector current (pulsed)	40	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
T_j	Operating junction temperature	- 55 to 150	$^\circ\text{C}$

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. $V_{clamp}=480\text{V}$, $T_j=150^\circ\text{C}$, $R_G=10\Omega$, $V_{GE}=15\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.08	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$, $V_{GE} = 0$	600			V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = \text{Max rating}$, $T_C = 25^{\circ}\text{C}$ $V_{CE} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			150 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}$, $V_{CE} = 0$			± 100	nA
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 250\text{ }\mu\text{A}$	3.75		5.75	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$, $I_C = 5\text{A}$ $V_{GE} = 15\text{V}$, $I_C = 5\text{A}$, $T_C = 125^{\circ}\text{C}$		1.9 1.7	2.5	V V
g_{fs}	Forward transconductance	$V_{CE} = 15\text{V}$, $I_C = 5\text{A}$		3.5		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GE} = 0$		365		pF
C_{oes}	Output capacitance			43		pF
C_{res}	Reverse transfer capacitance			8.3		pF
Q_g	Total gate charge	$V_{CE} = 390\text{V}$, $I_C = 5\text{A}$, $V_{GE} = 15\text{V}$, (see Figure 16)		19.2		nC
Q_{ge}	Gate-emitter charge			4.5		nC
Q_{gc}	Gate-collector charge			7		nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V$, $I_C = 5A$ $R_G = 10\Omega$, $V_{GE} = 15V$, <i>Figure 15. and Figure 17.</i>		14.2 5 1000		ns ns A/ μs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V$, $I_C = 5A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_j = 125^\circ C$ <i>Figure 15. and Figure 17.</i>		14 5 920		ns ns A/ μs
$t_r(V_{off})$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V$, $I_C = 5A$, $R_{GE} = 10\Omega$, $V_{GE} = 15V$, <i>Figure 15. and Figure 17.</i>		27 72 85		ns ns ns
$t_r(V_{off})$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V$, $I_C = 5A$, $R_{GE} = 10\Omega$, $V_{GE} = 15V$, $T_j = 125^\circ C$ <i>Figure 15. and Figure 17.</i>		50 108 139		ns ns ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on} $E_{off}^{(1)}$ E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V$, $I_C = 5A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_j = 25^\circ C$ <i>(see Figure 17)</i>		31.8 95 126.8		μJ μJ μJ
E_{on} $E_{off}^{(1)}$ E_{ts}	Turn-on switching losses Turn-off switching Losses Total switching losses	$V_{CC} = 390V$, $I_C = 5A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_j = 125^\circ C$ <i>(see Figure 17)</i>		61.8 173 234.8		μJ μJ μJ

1. Turn-off losses include also the tail of the collector current

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

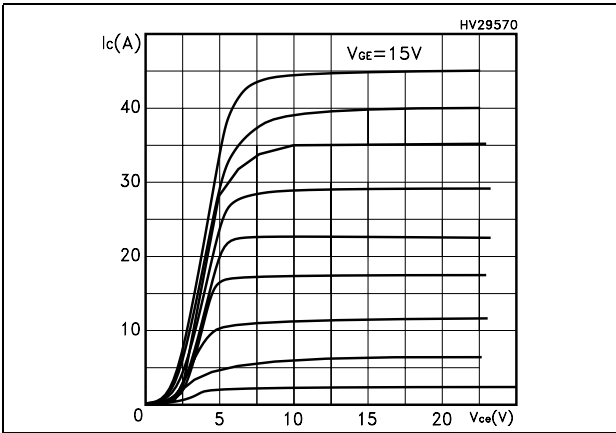


Figure 2. Transfer characteristics

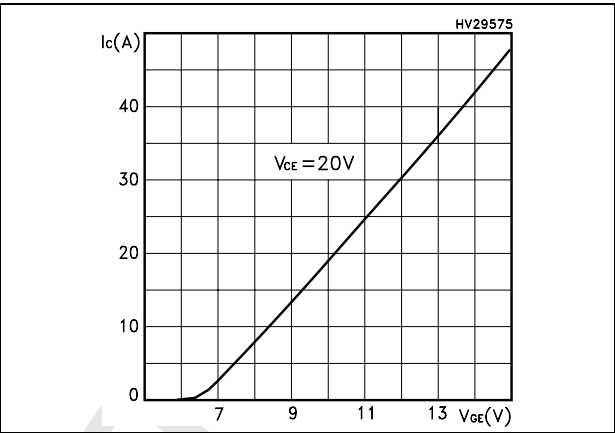


Figure 3. Transconductance

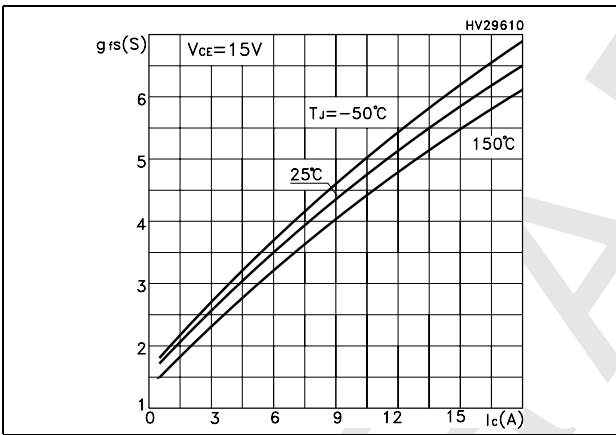


Figure 4. Collector-emitter on voltage vs temperature

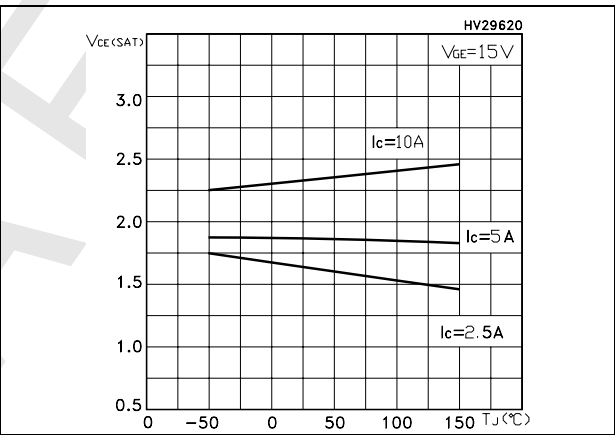


Figure 5. Gate charge vs gate-source voltage

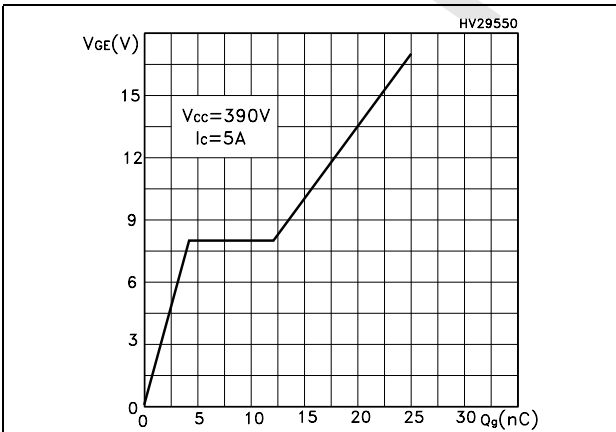


Figure 6. Capacitance variations

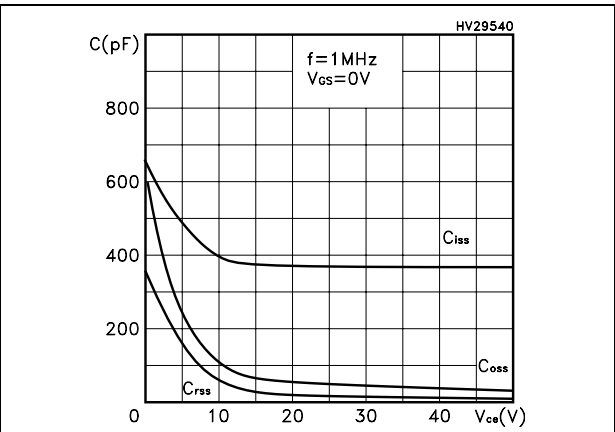


Figure 7. Normalized gate threshold voltage vs temperature

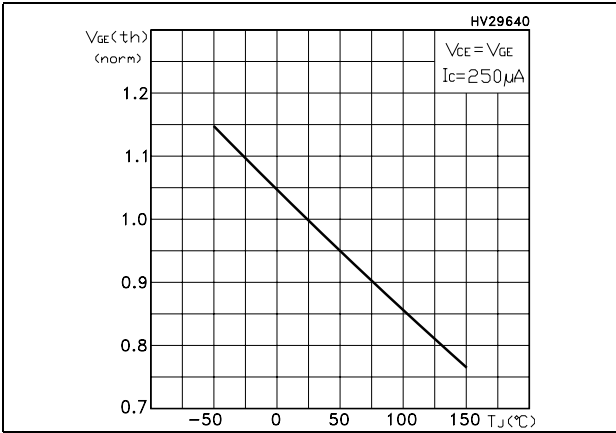


Figure 8. Collector-emitter on voltage vs collector current

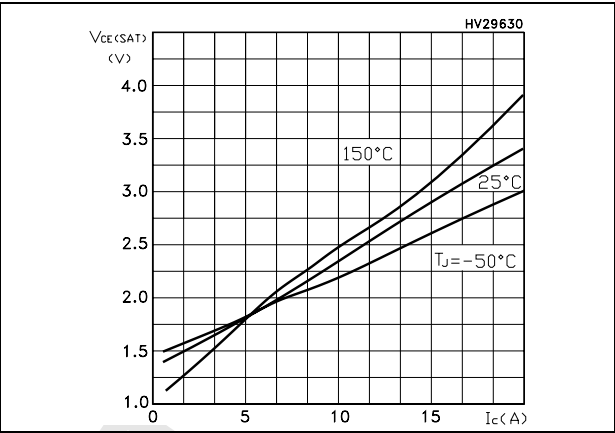


Figure 9. Normalized breakdown voltage vs temperature

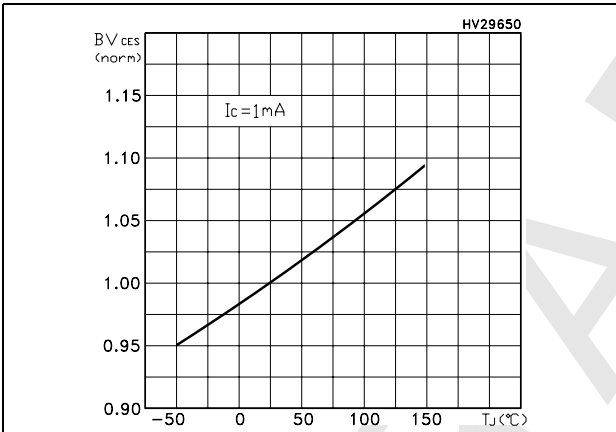


Figure 10. Switching losses vs temperature

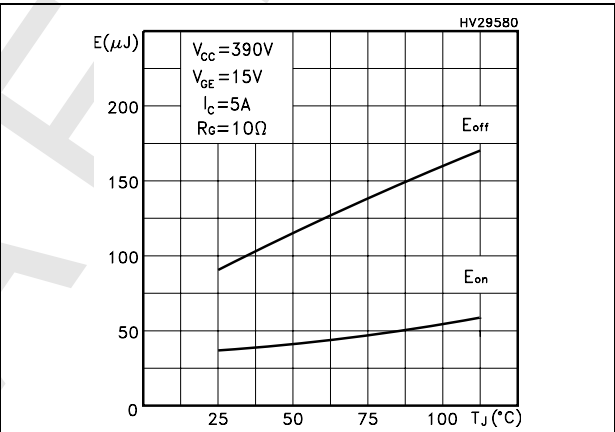


Figure 11. Switching losses vs gate resistance

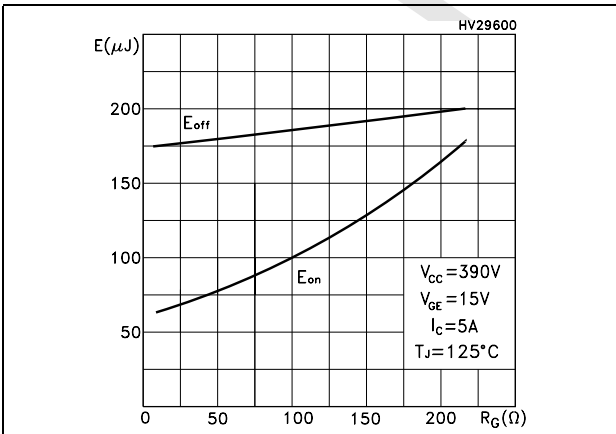


Figure 12. Switching losses vs collector current

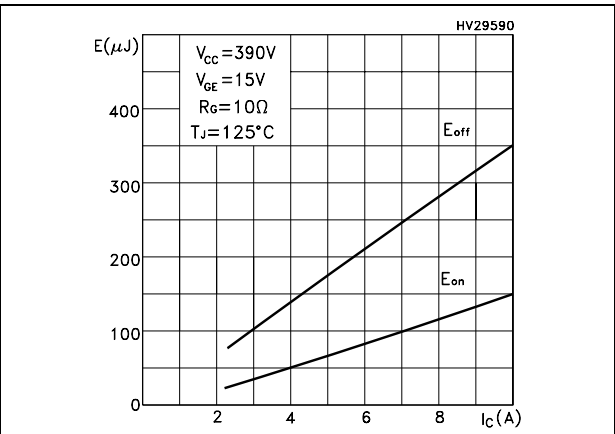


Figure 13. Thermal Impedance

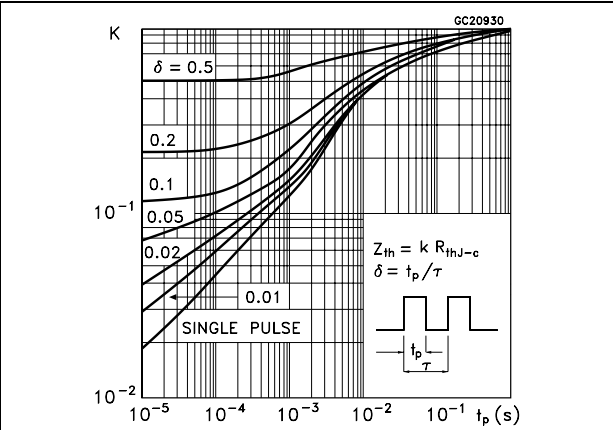
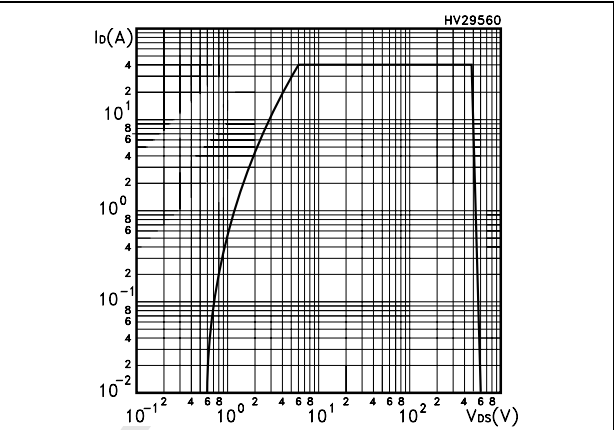


Figure 14. Turn-off SOA



3 Test circuits

Figure 15. Test circuit for inductive load switching

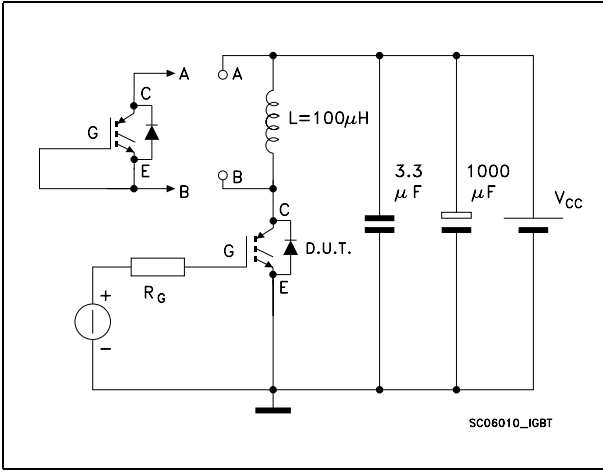


Figure 16. Gate charge test circuit

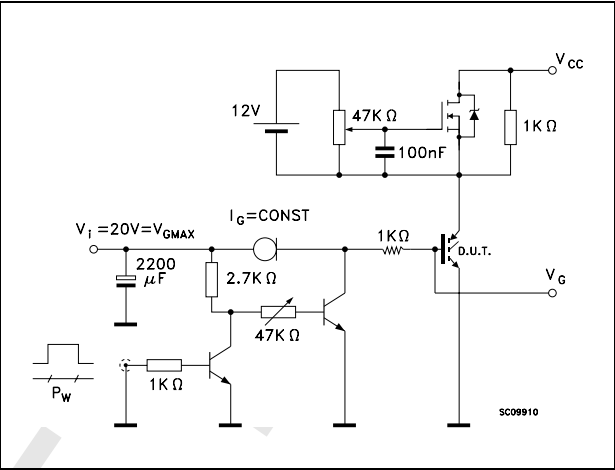
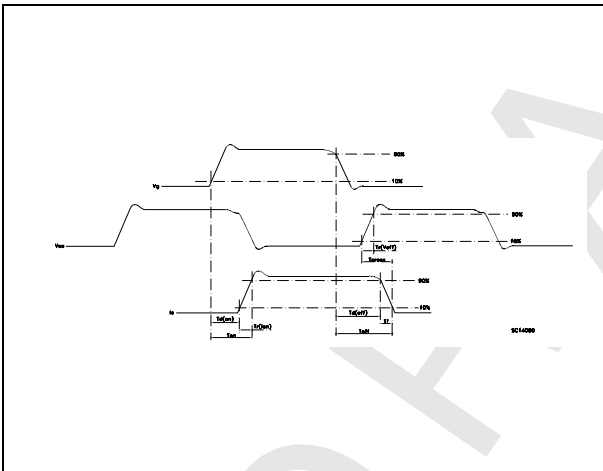


Figure 17. Switching waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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5 Revision history

Table 7. Revision history

Date	Revision	Changes
18-Nov-2005	1	Initial release.
12-Oct-2006	2	The document has been reformatted
02-Apr-2007	3	Corrected value on Table 3 .

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