

## 4-line ESD protection for high speed lines

Datasheet – production data

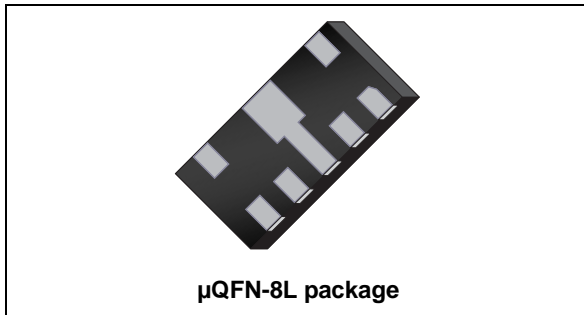
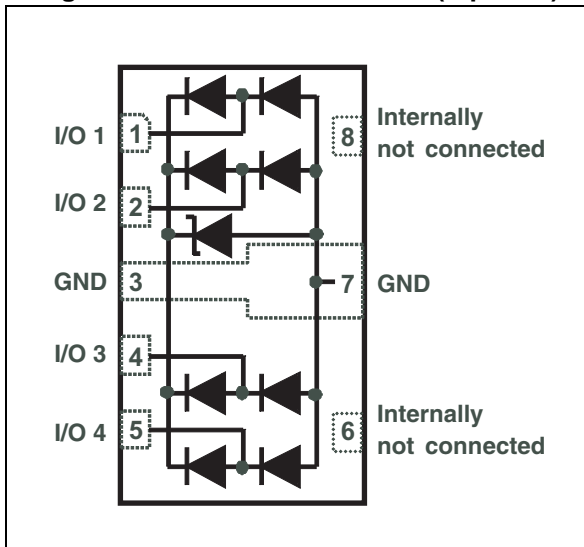


Figure 1. Functional schematic (top view)



### Features

- Flow-through routing to keep signal integrity
- Ultralarge bandwidth: 6 GHz
- Ultralow capacitance: 0.6 pF
- Low time domain reflection
- Low leakage current: 100 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- Package size in mm: 2 x 1 x 0.5
- RoHS compliant

### Benefits

- High ESD robustness of the equipment
- Suitable for high density boards

### Complies with following standards

- MIL-STD 883G Method 3015-7 Class 3B:
  - 8 kV
- IEC 61000-4-2 level 4:
  - 8 kV (contact discharge)
  - 15 kV (air discharge)

### Applications

The HSP061-4NY8 is designed to protect against electrostatic discharge on sub micron technology circuits driving:

- HDMI 1.3 and 1.4
- Digital Video Interface
- Display Port
- USB 3.0
- Serial ATA

### Description

The HSP061-4NY8 is a 4-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The ultra-low variation of the capacitance ensures very low influence on signal-skew. The large bandwidth and the low reflection make it compatible with 5 Gbps.

The device is packaged in μQFN-8L with a 400 μm pitch, which minimizes the PCB area.

# 1 Characteristics

**Table 1. Absolute maximum ratings  $T_{amb} = 25\text{ }^{\circ}\text{C}$**

Symbol	Parameter	Value	Unit
$V_{PP}$	Peak pulse voltage	IEC 61000-4-2 contact discharge	8
		IEC 61000-4-2 air discharge	20
$I_{pp}$	Repetitive peak pulse current (8/20 $\mu\text{s}$ )	3	A
$T_j$	Operating junction temperature range	-40 to +150	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Maximum lead temperature for soldering during 10 s	260	$^{\circ}\text{C}$

**Table 2. Electrical characteristics  $T_{amb} = 25\text{ }^{\circ}\text{C}$**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR}$	Breakdown voltage	$I_R = 1\text{ mA}$	6			V
$I_{RM}$	Leakage current	$V_{RM} = 3\text{ V}$			100	nA
$V_{CL}$	Clamping voltage	IEC 61000-4-2, +8 kV contact ( $I_{PP} = 30\text{ A}$ ), measured at 30 ns		18		V
$C_{I/O - GND}$	Capacitance (input/output to ground)	$V_{I/O} = 0\text{ V}$ , $F = (200\text{ MHz} - 3000\text{ MHz})$ , $V_{OSC} = 30\text{ mV}$		0.5	0.6	pF
$\Delta C_{I/O - GND}$	Capacitance variation (input/output to ground)	$V_{I/O} = 0\text{ V}$ $F = 1\text{ MHz}$ , $V_{OSC} = 30\text{ mV}$		0.03	0.05	pF
$f_C$	Cut-off frequency	-3dB		6		GHz
$Z_{Diff}$	Differential impedance	$t_r = 200\text{ ps}$ (10 - 90%) <sup>(1)</sup> $Z_{0\text{ Diff}} = 100\text{ }\Omega$	85	100	115	$\Omega$

1. HDMI specification conditions. This information can be provided for other applications. Please contact your local ST office.

Figure 2. Leakage current versus junction temperature (typical values)

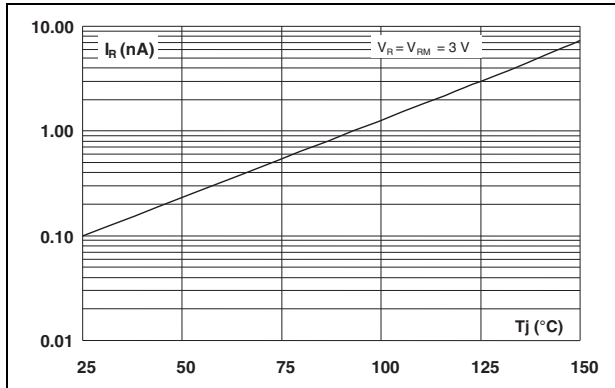


Figure 3. S21 attenuation measurement

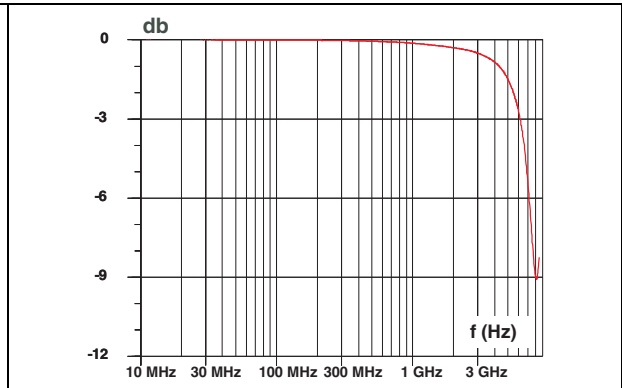


Figure 4. Differential impedance ( $Z_{diff}$ )<sup>(1)</sup>

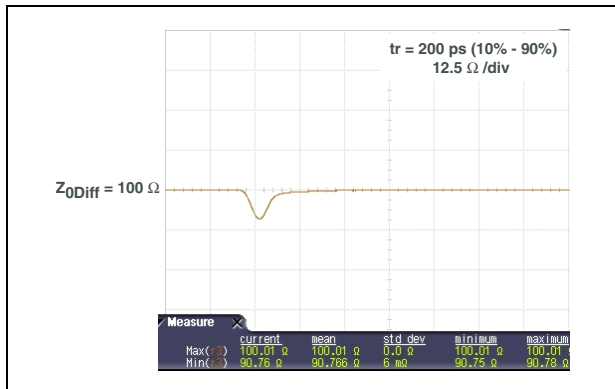
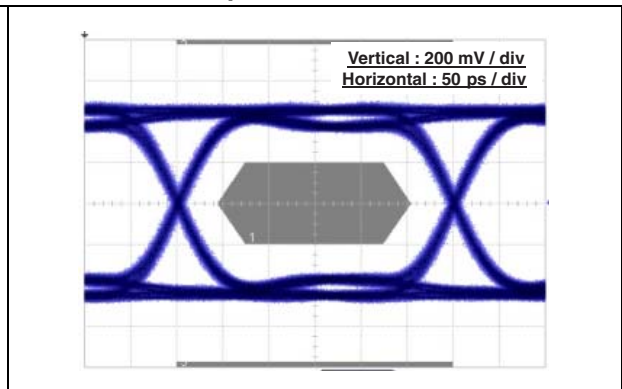


Figure 5. Eye diagram - HDMI mask at 3.4 Gbps per channel<sup>(1)</sup>



1. HDMI specification conditions. This information can be provided for other applications. Please contact your local ST office.

Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

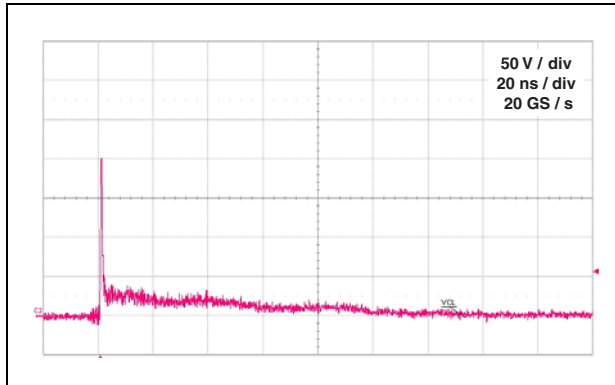
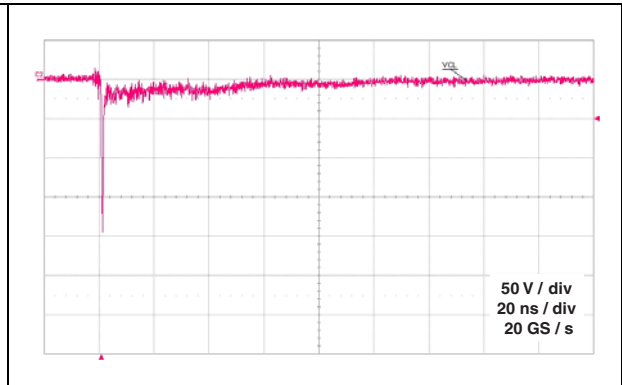


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



## 2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Figure 8. μQFN-8L dimension definitions

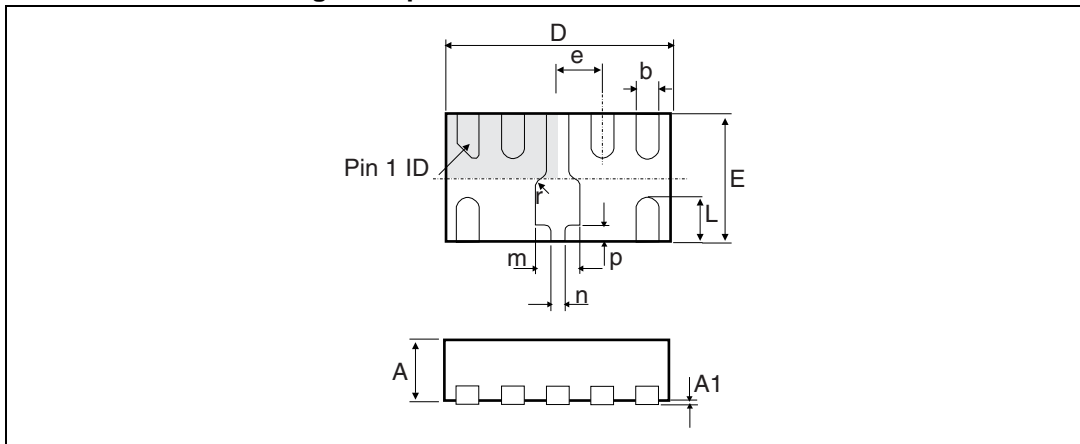
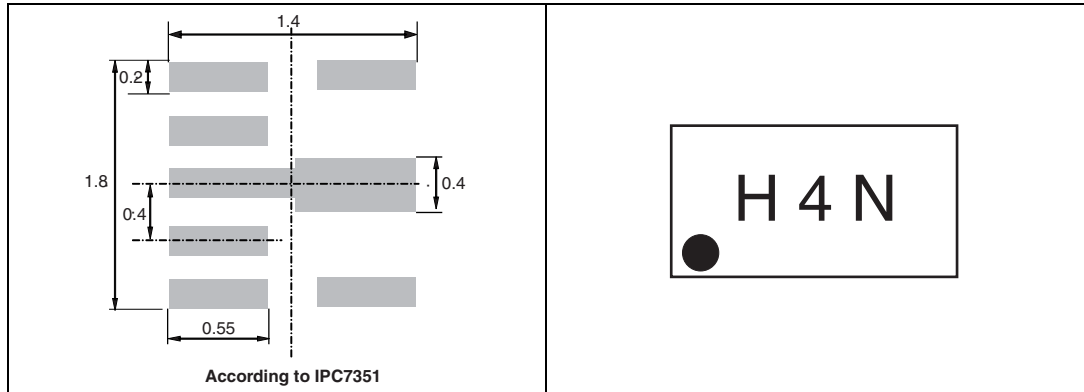


Table 3. μQFN-8L dimensions

Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.00	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.95	2.00	2.05	0.077	0.079	0.081
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.35	0.40	0.45	0.014	0.016	0.018
L	0.25	0.35	0.45	0.010	0.014	0.018
m		0.40			0.016	
n		0.15			0.006	
p		0.11			0.004	
r		0.05			0.002	

**Figure 9. Footprint recommendations (dimensions in mm)**

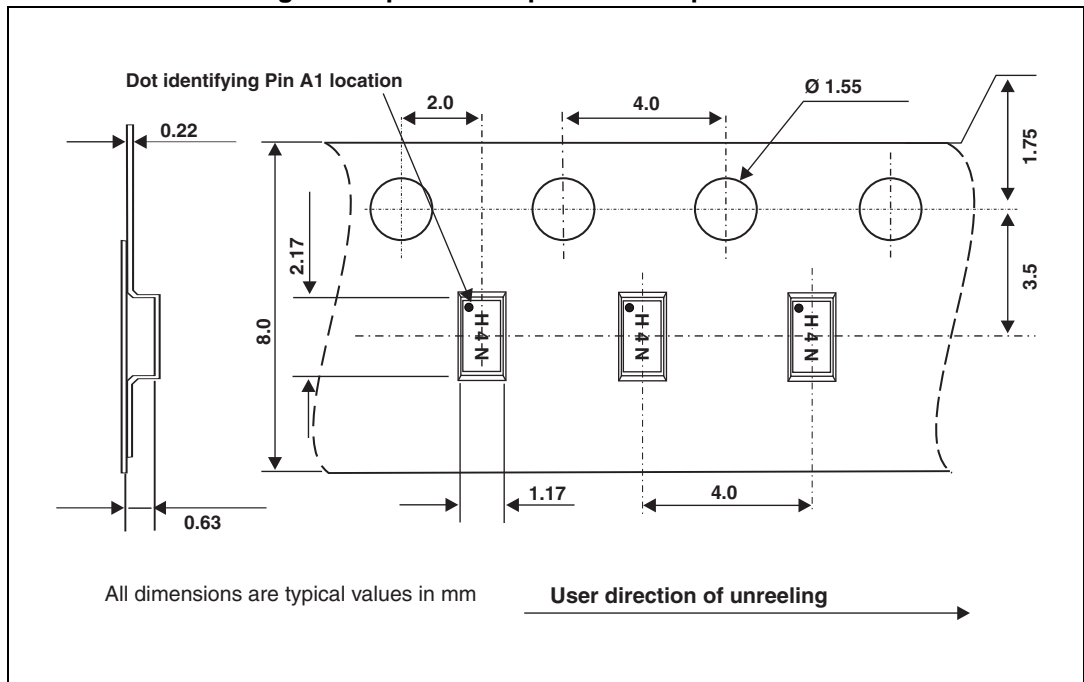


**Figure 10. Marking**



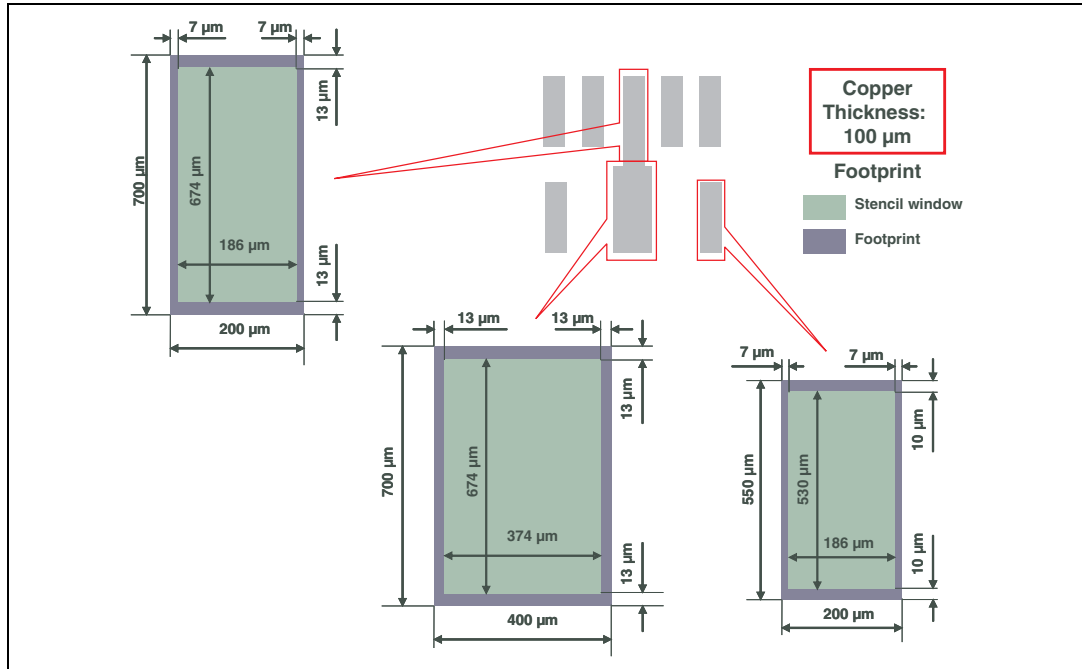
*Note:* Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

**Figure 11. μQFN-8L tape and reel specification**



### 3 Recommendation on PCB assembly

Figure 12. Recommended stencil window position



#### 3.1 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

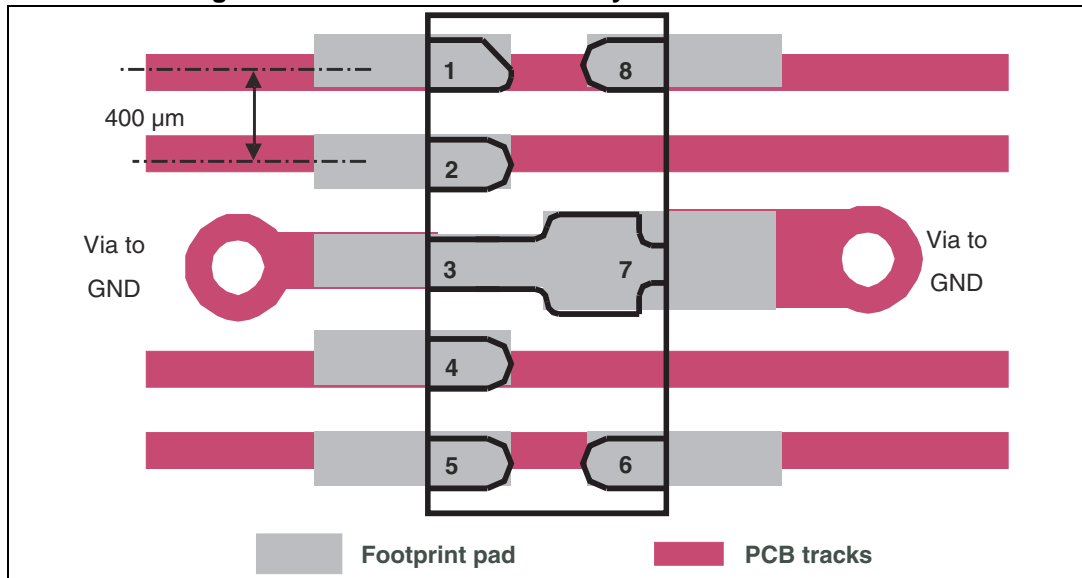
#### 3.2 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.3 PCB design

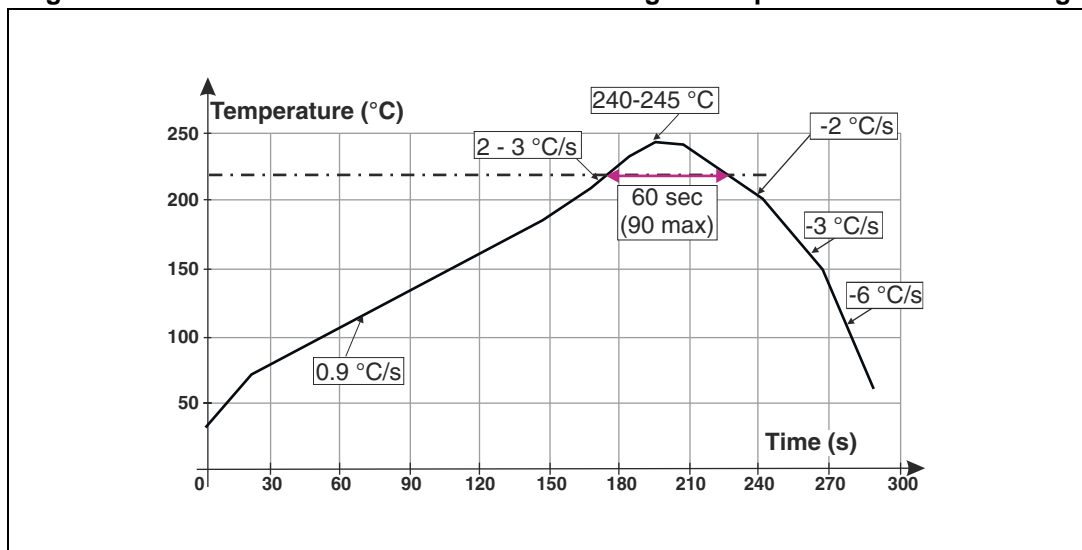
1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

Figure 13. Printed circuit board layout recommendations



### 3.4 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

## 4 Ordering information

Figure 15. Ordering information scheme

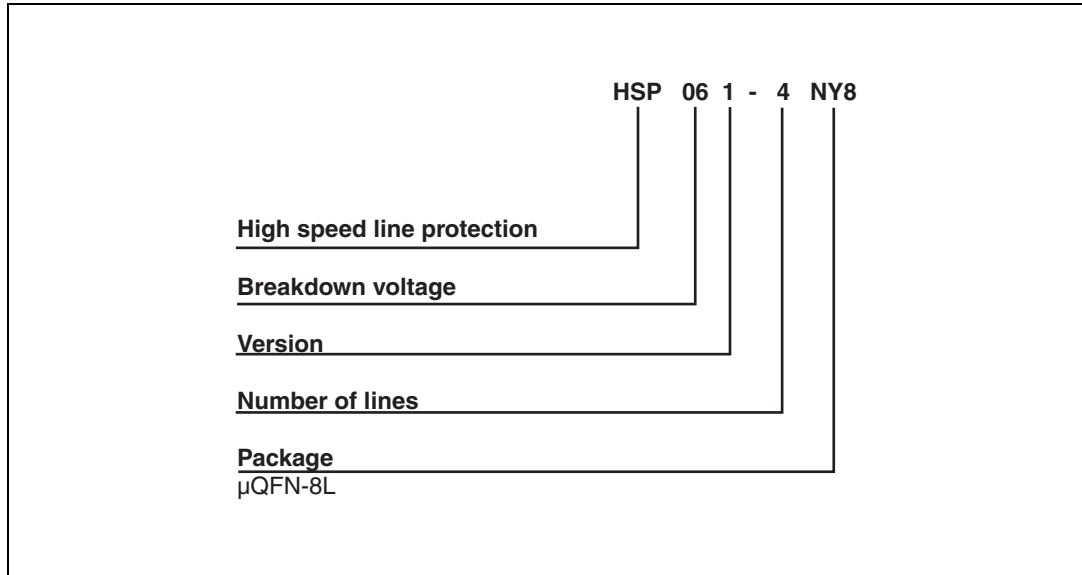


Table 4. Ordering information

Order code	Marking <sup>(1)</sup>	Package	Weight	Base qty	Delivery mode
HSP061-4YN8	H4N	μQFN-8L	2.77 mg	6000	Tape and reel (7")

1. The marking can be rotated by multiples of 90° to differentiate assembly location

## 5 Revision history

Table 5. Document revision history

Date	Revision	Changes
20-Apr-2010	1	Initial release.
15-Oct-2010	2	Updated values for $\Delta C_{I/O - GND}$ in <a href="#">Table 2</a> . Updated <a href="#">Figure 13</a> . Updated package name.
29-Mar-2012	3	Updated <a href="#">Table 2</a> . Updated weight value in <a href="#">Table 4</a> .
19-Oct-2012	4	Added IEC 61000-4-2 air discharge parameter in <a href="#">Table 1</a> . Added grid to <a href="#">Figure 14</a> for easier reading of values.
27-Mar-2013	5	Added notes on marking rotation.

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