

# NTR4003N, NVR4003N

## Small Signal MOSFET 30 V, 0.56 A, Single N-Channel, SOT-23

### Features

- Low Gate Voltage Threshold ( $V_{GS(TH)}$ ) to Facilitate Drive Circuit Design
- Low Gate Charge for Fast Switching
- ESD Protected Gate
- SOT-23 Package Provides Excellent Thermal Performance
- Minimum Breakdown Voltage Rating of 30 V
- NVR Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Notebooks:
  - ◆ Level Shifters
  - ◆ Logic Switches
  - ◆ Low Side Load Switches
- Portable Applications

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	30	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	0.5	A
			$T_A = 85^\circ\text{C}$	0.37	
Power Dissipation (Note 1)	Steady State	$P_D$	0.69	W	
Continuous Drain Current (Note 1)	$t < 10$ s	$I_D$	$T_A = 25^\circ\text{C}$	0.56	A
			$T_A = 85^\circ\text{C}$	0.40	
Power Dissipation (Note 1)	$t < 5$ s	$P_D$	0.83	W	
Pulsed Drain Current	$t_p = 10$ $\mu\text{s}$	$I_{DM}$	1.7	A	
Operating Junction and Storage Temperature		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	1.0	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	180	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t < 10$ s (Note 1)	$R_{\theta JA}$	150	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	300	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size.

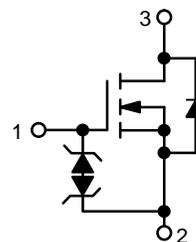


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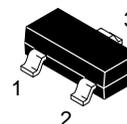
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
30 V	1.0 $\Omega$ @ 4.0 V	0.56 A
	1.5 $\Omega$ @ 2.5 V	

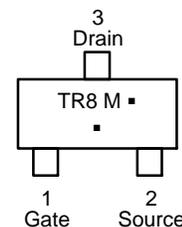
### N-Channel



### MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23  
CASE 318  
STYLE 21



TR8 = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTR4003NT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR4003NT3G	SOT-23 (Pb-Free)	10,000 / Tape & Reel
NVR4003NT3G	SOT-23 (Pb-Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			40		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$			1.0	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$			$\pm 1.0$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	0.8		1.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.0\text{ V}, I_D = 10\text{ mA}$		1.0	1.5	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 10\text{ mA}$		1.5	2.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 3.0\text{ V}, I_D = 10\text{ mA}$		0.33		S

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 5.0\text{ V}$		21	42	pF
Output Capacitance	$C_{oss}$			19.7	40	
Reverse Transfer Capacitance	$C_{rss}$			8.1	16	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 5.0\text{ V}, V_{DS} = 24\text{ V}, I_D = 0.1\text{ A}$		1.15		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.15		
Gate-to-Source Gate Charge	$Q_{GS}$			0.32		
Gate-to-Drain Charge	$Q_{GD}$			0.23		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 5.0\text{ V}, I_D = 0.1\text{ A}, R_G = 50\ \Omega$		16.7		ns
Rise Time	$t_r$			47.9		
Turn-Off Delay Time	$t_{d(off)}$			65.1		
Fall Time	$t_f$			64.2		

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 10\text{ mA}$	$T_J = 25^\circ\text{C}$	0.65	0.7	V
			$T_J = 125^\circ\text{C}$	0.45		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 8\text{ A}/\mu\text{s}, I_S = 10\text{ mA}$		14		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

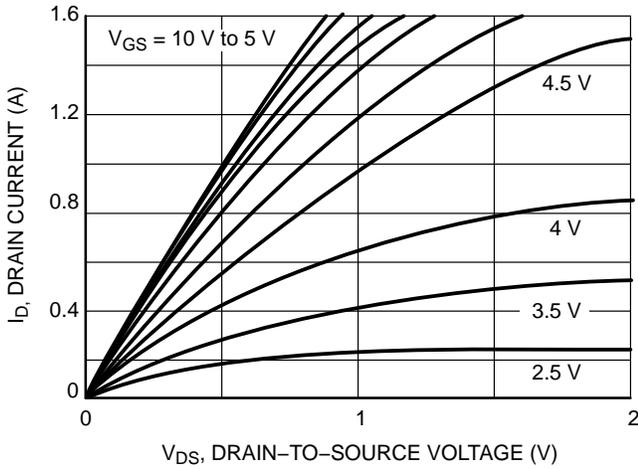


Figure 1. On-Region Characteristics

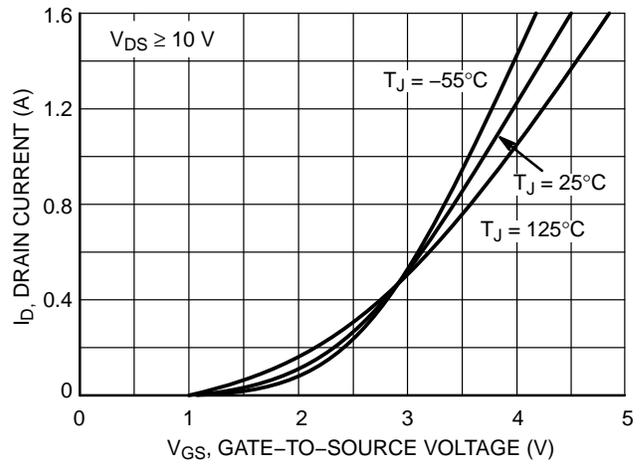


Figure 2. Transfer Characteristics

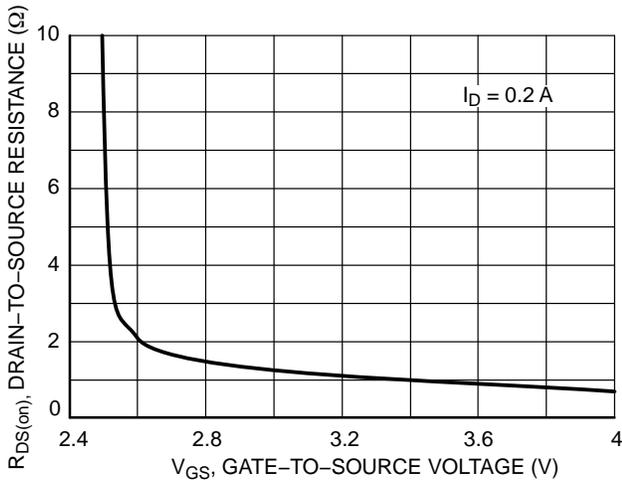


Figure 3. On-Resistance vs. Gate-to-Source Voltage

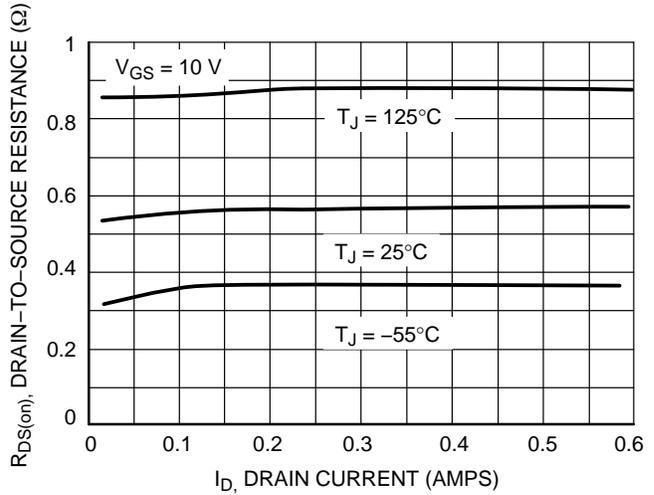


Figure 4. On-Resistance vs. Drain Current and Temperature

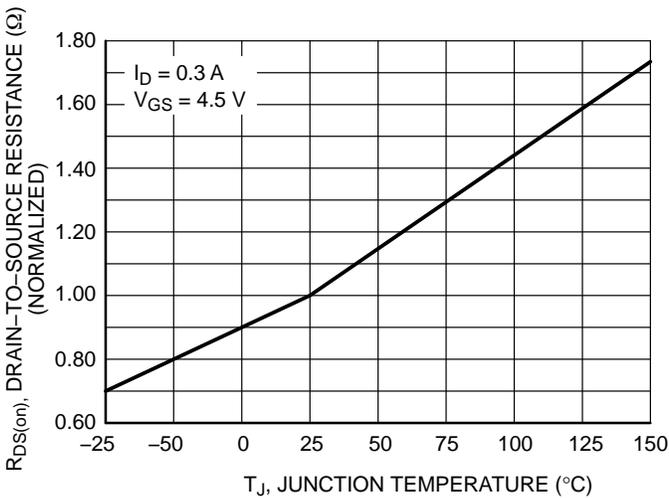


Figure 5. On-Resistance Variation with Temperature

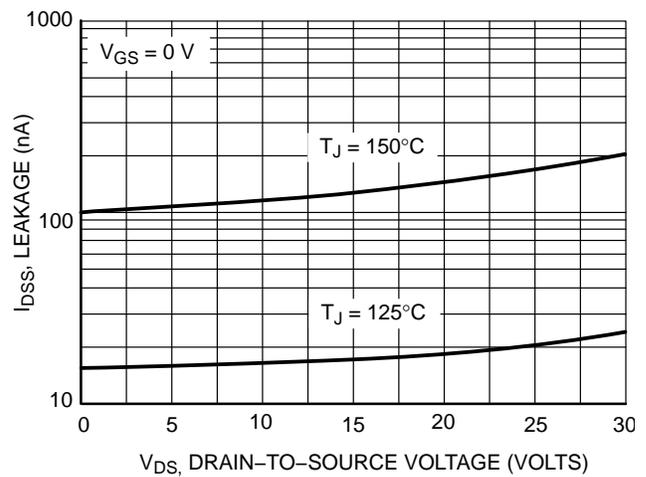


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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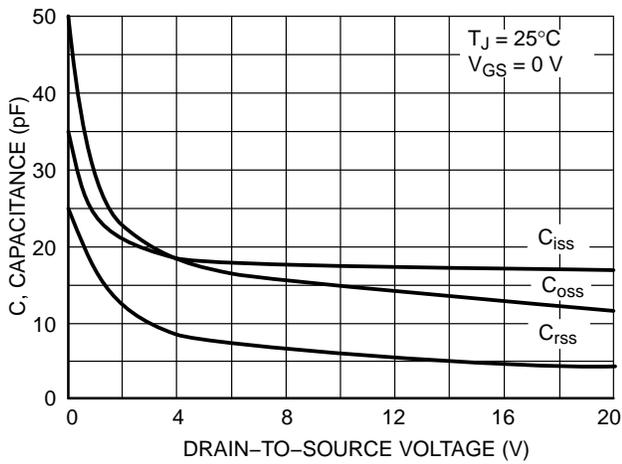


Figure 7. Capacitance Variation

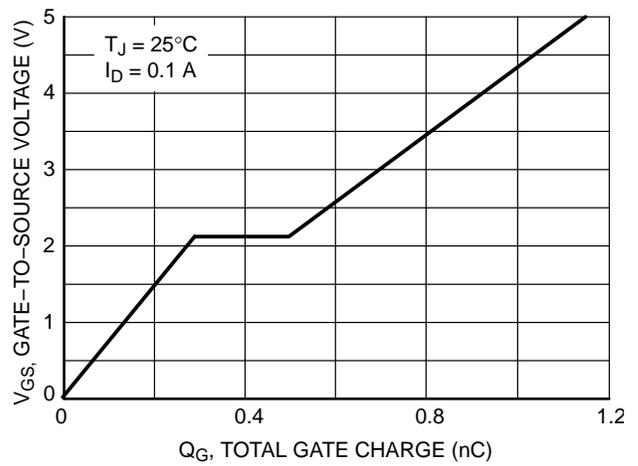


Figure 8. Gate-to-Source & Drain-to-Source Voltage vs. Total Charge

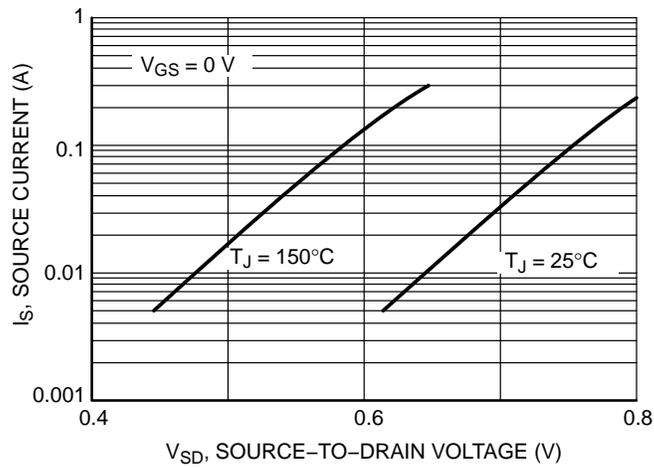
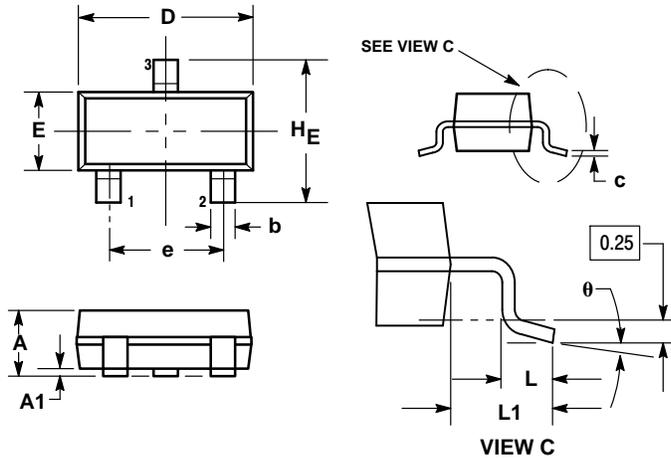


Figure 9. Diode Forward Voltage vs. Current

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## PACKAGE DIMENSIONS

### SOT-23 (TO-236) CASE 318-08 ISSUE AP

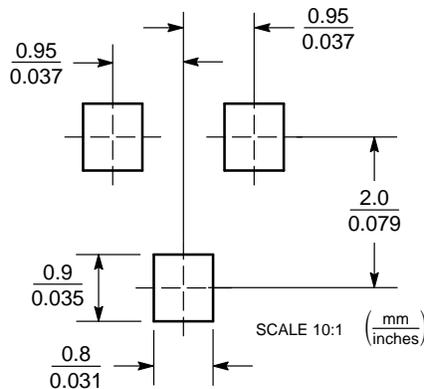


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

- STYLE 21:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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