



Quad SPST CMOS Analog Switch with Latches

FEATURES

- Accepts 150-ns Write Pulse Width
- 5-V On-Chip Regulator
- Latches Are Transparent with $\overline{WR}$ Low
- Low On-Resistance: 60 Ω

BENEFITS

- Compatible with Most μP Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Consumption
- Allows Flexibility of Design

APPLICATIONS

- μP Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems
- Medical Instrumentation
- Factory Automation

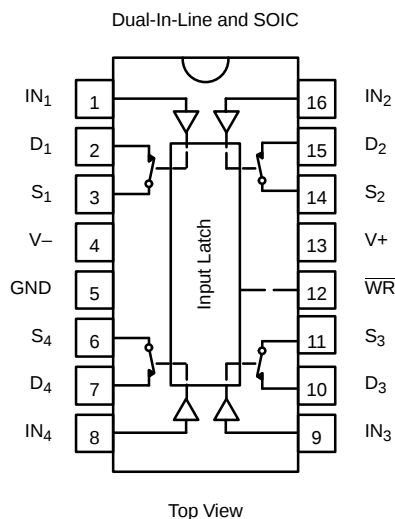
DESCRIPTION

The DG221B is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common $\overline{WR}$ pin, each DG221B can be memory mapped, and addressed as a single data byte for simultaneous switching.

The DG221B combines low power and low on-resistance (60 Ω typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four Latchable SPST Switches per Package

TRUTH TABLE		
IN_x	$\overline{WR}$	Switch
0	0	ON
1	0	OFF
X		Control data latched-in, switches on or off as selected by last IN_x
X	1	Maintains previous state

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40°C to 85°C	16-Pin Plastic DIP	DG221BDJ
	16-Pin Narrow SOIC	DG221BDY

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–	
V+	34 V
GND	25 V
Digital Inputs ^a , V _S , V _D	(V–) –2 V to (V+) +2 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed 1 ms, 10% duty cycle)	70 mA

Storage Temperature: (DJ and DY Suffix)	–65 to 125°C
Power Dissipation (Package) ^b	
16-Pin Plastic DIP ^c	470 mW
16-Pin SOIC ^d	600 mW

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 7.7 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

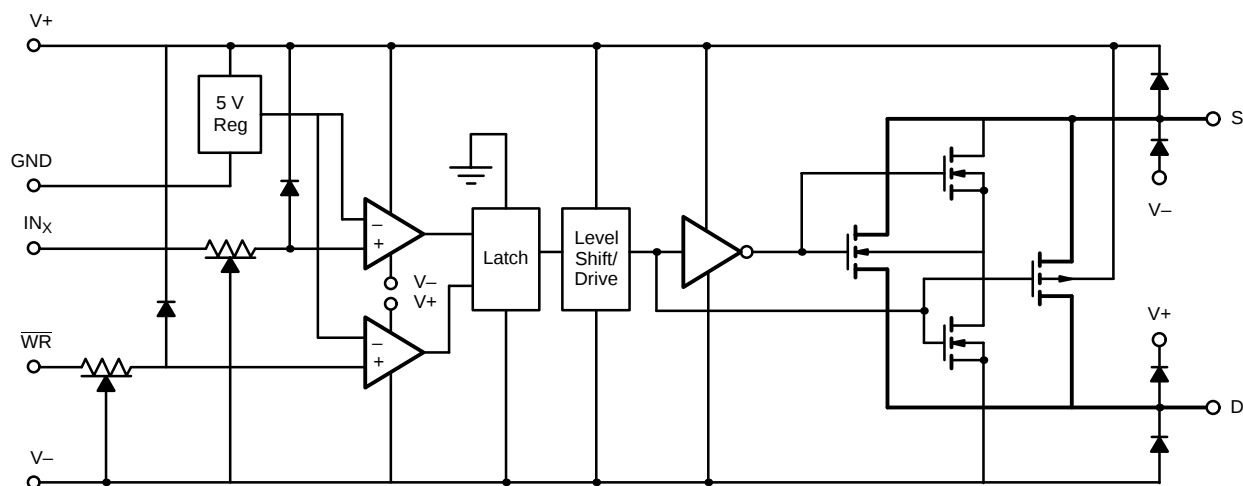


FIGURE 1.

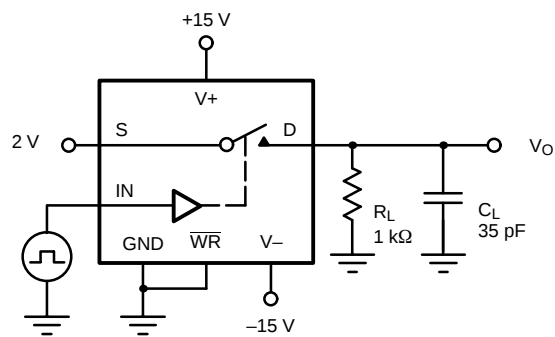


SPECIFICATIONS ^a							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V _– = –15 V V _{IN} = 2.4 V, 0.8 ^f V, $\overline{WR}$ = 0	Temp ^b	Limits –40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	V _{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	r _{DS(on)}	I _S = –10 mA, V _D = ±10 V	Room Full		60	90 135	Ω
Source Off Leakage Current	I _{S(off)}	V _S = ±14 V, V _D = ∓14 V	Room Full	–5 –100	±0.01	5 100	nA
Drain Off Leakage Current	I _{D(off)}		Room Full	–5 –100	±0.02	5 100	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ±14 V	Room Full	–5 –200	±0.01	5 200	
Digital Control							
Input Current	I _{INL} , I _{INH}	V _{IN} = 0 V or = 2.4 V	Room Full	–1 –10	–0.0004	1 10	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	See Figure 2	Room			550	ns
Turn-Off Time	t _{OFF}		Room			340	
Turn-On Time Write	t _{ON} , $\overline{WR}$	See Figure 3	Room			550	
Turn-Off Time Write	t _{OFF} , $\overline{WR}$		Room			340	
Write Pulse Width	t _W	See Figure 4	Room	150	120		
Input Setup Time	t _S		Room	180	130		
Input Hold Time	t _H		Room	20	18		
Charge Injection	Q	C _L = 1000 pF V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		20		pC
Source-Off Capacitance	C _{S(off)}	f = 1 MHz, V _S , V _D = 0 V	Room		8		pF
Drain-Off Capacitance	C _{D(off)}		Room		9		
Channel-On Capacitance	C _{D(on)}		Room		29		
Off Isolation	OIRR	V _S = 1 V _{p-p} , f = 100 kHz C _L = 15 pF, R _L = 1 kΩ	Room		70		dB
Interchannel Crosstalk	X _{TALK}		Room		90		
Power Supplies							
Positive Supply Current	I ₊	All Channels On or Off V _{IN} = 0 V or 2.4 V	Full		0.8	1.5	mA
Negative Supply Current	I _–		Room	–1	–0.4		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

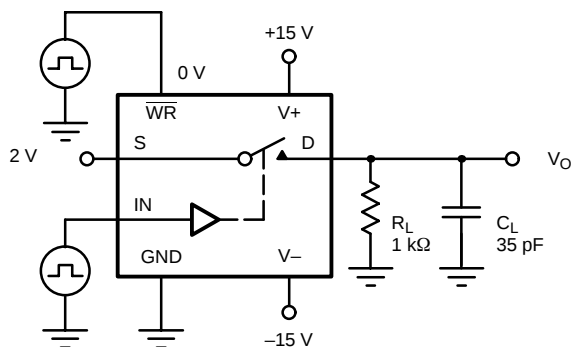
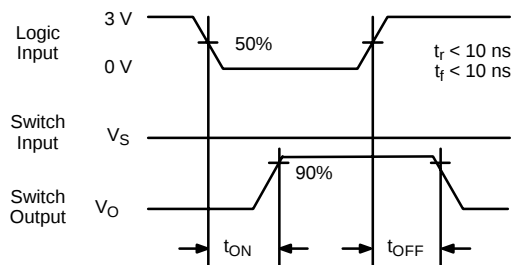
TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

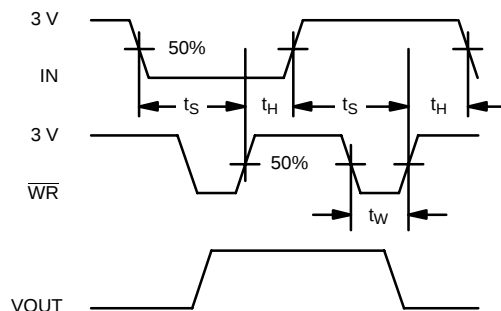
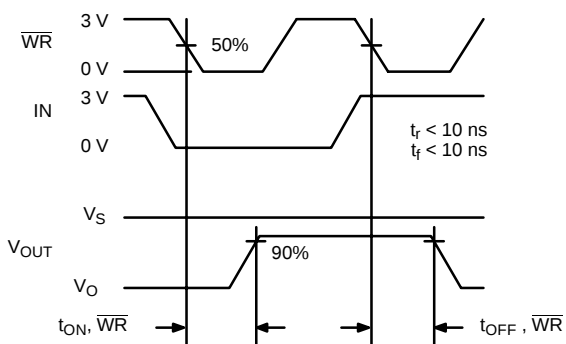
FIGURE 2. Switching Time



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

FIGURE 3. $\overline{WR}$ Switching Time

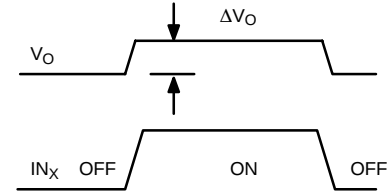
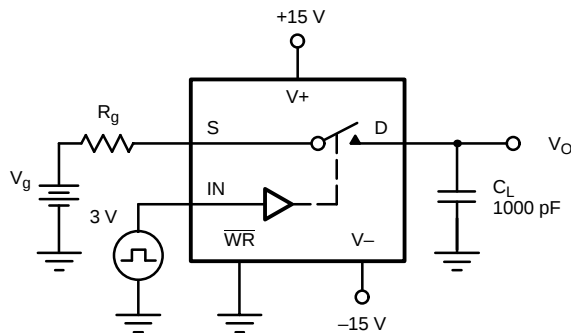


t_H = Hold Time
 t_S = Setup Time
 t_W = WR Pulse Width

The latches are level sensitive. When $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

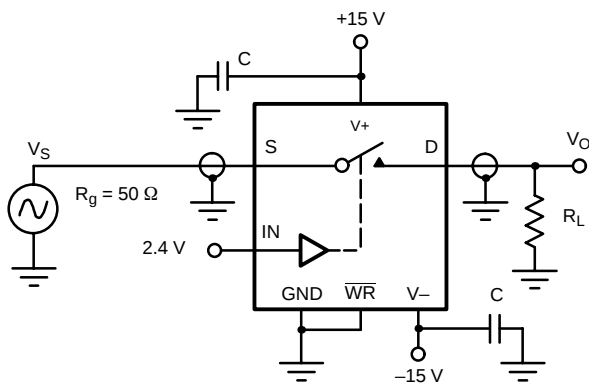
FIGURE 4. $\overline{WR}$ Setup Conditions

TEST CIRCUITS



ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

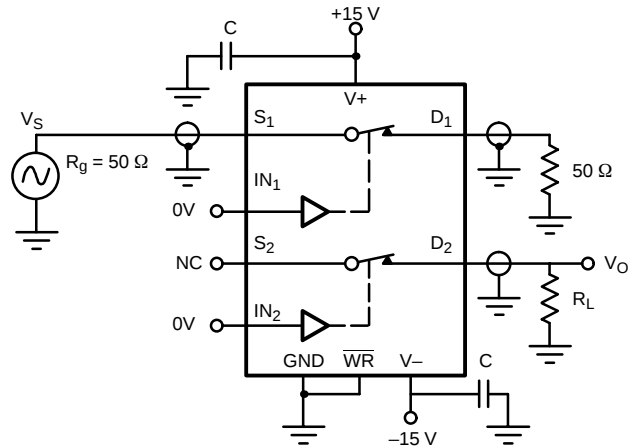
FIGURE 5. Charge Injection



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

FIGURE 6. Off Isolation



$$X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

FIGURE 7. Channel-to-Channel Crosstalk

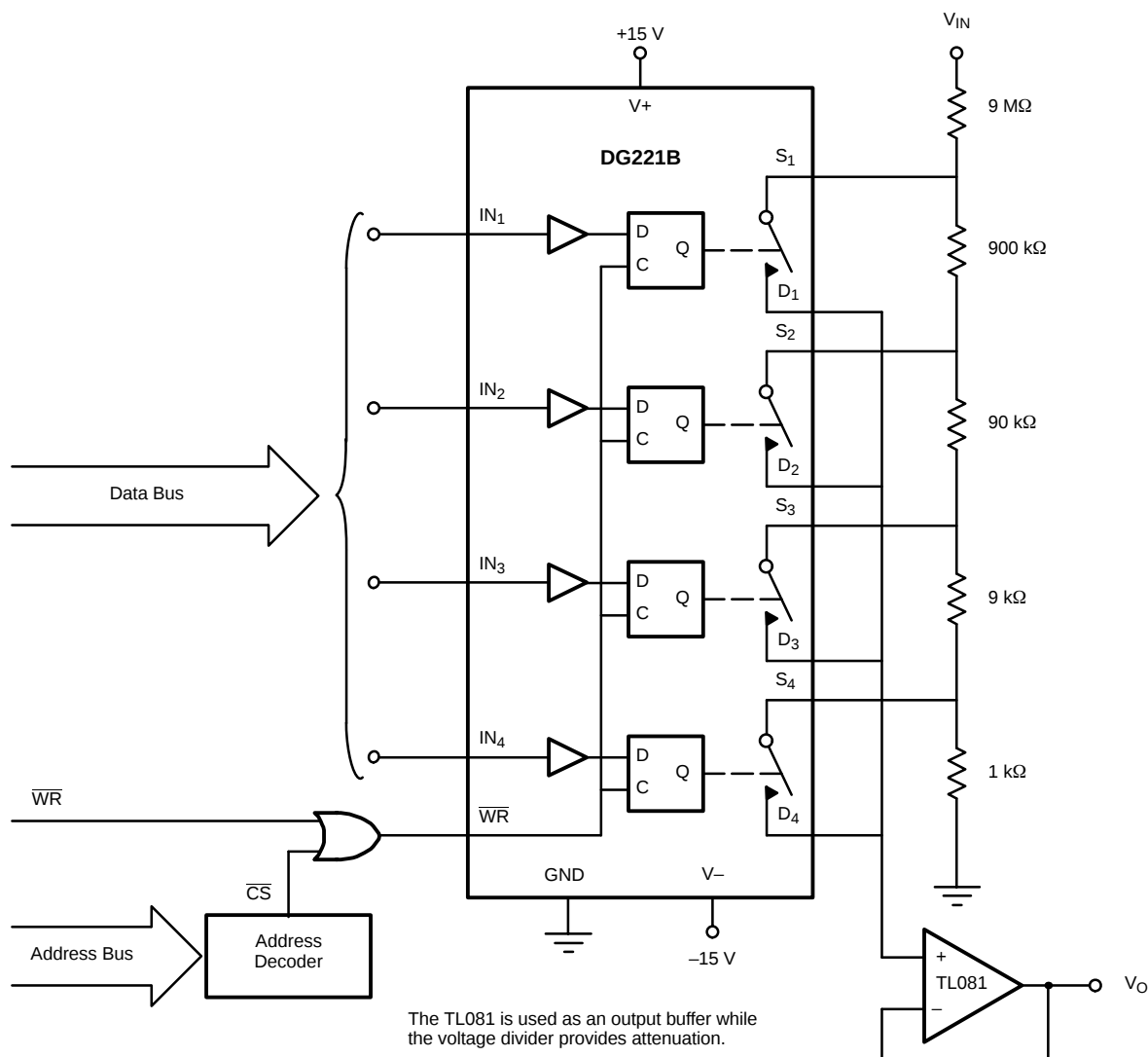
APPLICATION HINTS^a

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND (V)	$\overline{WR}$ (V)	V _{IN} Logic Input Voltage V _{INH(min)} /V _{INL(max)} (V)	V _S or V _D Analog Voltage Range (V)
15	-15	0	2.4/0.8	2.4/0.8	-15 to 15
10	-10	0	2.4/0.8	2.4/0.8	-10 to 10
10	-5	0	2.4/0.8	2.4/0.8	-5 to 10

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

FIGURE 8. μ P-Controlled Analog Signal Attenuator

TRUTH TABLE					
IN ₁	IN ₂	IN ₃	IN ₄	WR ^A	ON SWITCH
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

OUTPUT ATTENUATION FOR FIGURE 8					
WR	IN ₁	IN ₂	IN ₃	IN ₄	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

Notes:

a. WR may be held at "0" for temporary operation similar to DG201A/DG201B. With WR at "0" SW₁ will remain on as long as IN₁ is held at "0".



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