Kintex-7 FPGA KC705 Embedded Kit

Getting Started Guide

Vivado Design Suite 2013.2

UG913 (v4.1.1) March 7, 2014

XILINX

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/23/2012	1.0	Initial Xilinx release.
05/31/2012	1.0.1	Updated PDF document properties.
08/16/2012	1.1	Replaced ISE software with Xilinx Design Tools throughout. Added Vivado tools to KC705 Embedded Kit Contents, page 7. Updated URL for Kintex-7 FPGA embedded kit in What's Available Online, page 8. Updated Figure 1-1, Figure 1-4, Figure 1-5, Figure 1-7, and Figure 1-8. Updated steps in Running the Video Demonstration, page 11. Updated Next Steps, page 18. Updated Table 1-1. Added Documentation, page 19. Updated title of Appendix B, Installation and Licensing of Xilinx Design Tools.
10/31/2012	1.2	Removed mention of flash drives throughout. Added jumper settings to step of Video Demonstration Hardware Setup Instructions, page 10. In step 3 of Running the Video Demonstration, page 11, changed 14.1 to 14.x.
11/27/2012	1.2.1	Updated XPN number on the title page.
01/24/2013	2.0	Updated jumper settings in step of Video Demonstration Hardware Setup Instructions. Added "(ISE Design Suite 14.4)" to document title.
04/12/2013	2.0.1	Removed XPN number from the title page. No other changes.
04/12/2013	3.0	Updated for ISE® Design Suite 14.5. Two of the local cores, DVI2AXI and PERF_MONITOR, were replaced with EDK build IPs. Figure 1-1 was updated and different color codes are used to differentiate local and EDK IPs. Figure 1-5 was updated. Appendixes were re-sequenced and Appendix C was enhanced.
04/17/2013	3.0.1	Updated links for UG914 and UG915.
04/23/2013	3.0.2	Updated links for UG914 and UG915.

Date	Version	Revision
08/29/2013	4.0	Updated for Vivado Design Suite 2013.2. Updated Figure 1-1 and Figure 1-8. Updated Table 1-1.
12/20/2013	4.1	Updated disclaimer and copyright. Updated What's Inside the Box.
03/07/2014	4.1.1	Made typographical edits.

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Chapter 1

Getting Started with the Kintex-7 FPGA KC705 Embedded Kit

Introduction

The Kintex®-7 FPGA embedded kit conveniently delivers the key components of the Xilinx® Embedded Targeted Design Platform (TDP) required for developing embedded software and hardware in a wide range of applications in the broadcast, industrial, medical, and aerospace and defense markets. For software developers, a familiar Eclipse-based integrated development environment (IDE), GNU tools, operating systems, libraries, and a pre-verified reference design enables them to start programming right away. Similarly, hardware designers now have immediate access to a pre-integrated MicroBlaze™ processor subsystem that includes the most commonly used peripheral IP cores, enabling the designers to begin at once developing their custom logic.

This getting started guide identifies the steps required to set up the KC705 board and run the out-of-box video demonstration, which illustrates the flexibility and capability of a MicroBlaze processor subsystem for embedded design. If the Xilinx Design Tools have not already been installed, the user is directed through the steps to install the software, get updates, and generate a license.

KC705 Embedded Kit Contents

What's Inside the Box

- KC705 evaluation board featuring the XC7K325T-2FFG900C FPGA
- USB cables, Ethernet cable, and universal power supply
- SD card
- Xilinx Design Tools (node-locked, device-locked for the XC7K325T-2FFG900C FPGA), which includes:
  - Vivado® design tools
  - Software Development Kit (SDK)
- Documentation:
  - Kintex-7 FPGA Embedded Kit Targeted Reference Design Documentation Advisory
- Reference designs and demonstrations:
  - BIST - MicroBlaze processor subsystem
  - Web server-based multi video streams demonstration system

What's Available Online

- License for Vivado Design Suite:
  - Licensing Solution Center
  - Xilinx Licensing FAQ
- Embedded kit home page with documentation and reference designs:
  - Kintex-7 FPGA Embedded Kit
- Technical Support

Getting Started with the Video Demonstration

This Kintex-7 FPGA embedded kit comes with a video demonstration available on the embedded kit home page. This demonstration can be run before installing any additional tools to get an overview of the features of the KC705 evaluation board using a MicroBlaze processor subsystem in the Kintex-7 (XC7K325T-FF900-2) FPGA.

Processor System Used for the Video Demonstration

The provided video demonstration uses a pre-built Kintex-7 FPGA design (Figure 1-1) with these features:

- MicroBlaze processor
- External DDR3 SDRAM interface
- External flash memory interface
- On-chip memory (block RAM)
- Integrated Tri-Mode Ethernet MAC
- UART (connected from the KC705 board via the USB-UART connector)
- Interrupt controller (Intc) and timer
- GPIO (LCD, LEDs, buttons, switches, and rotary)
- Software-configurable XADC block

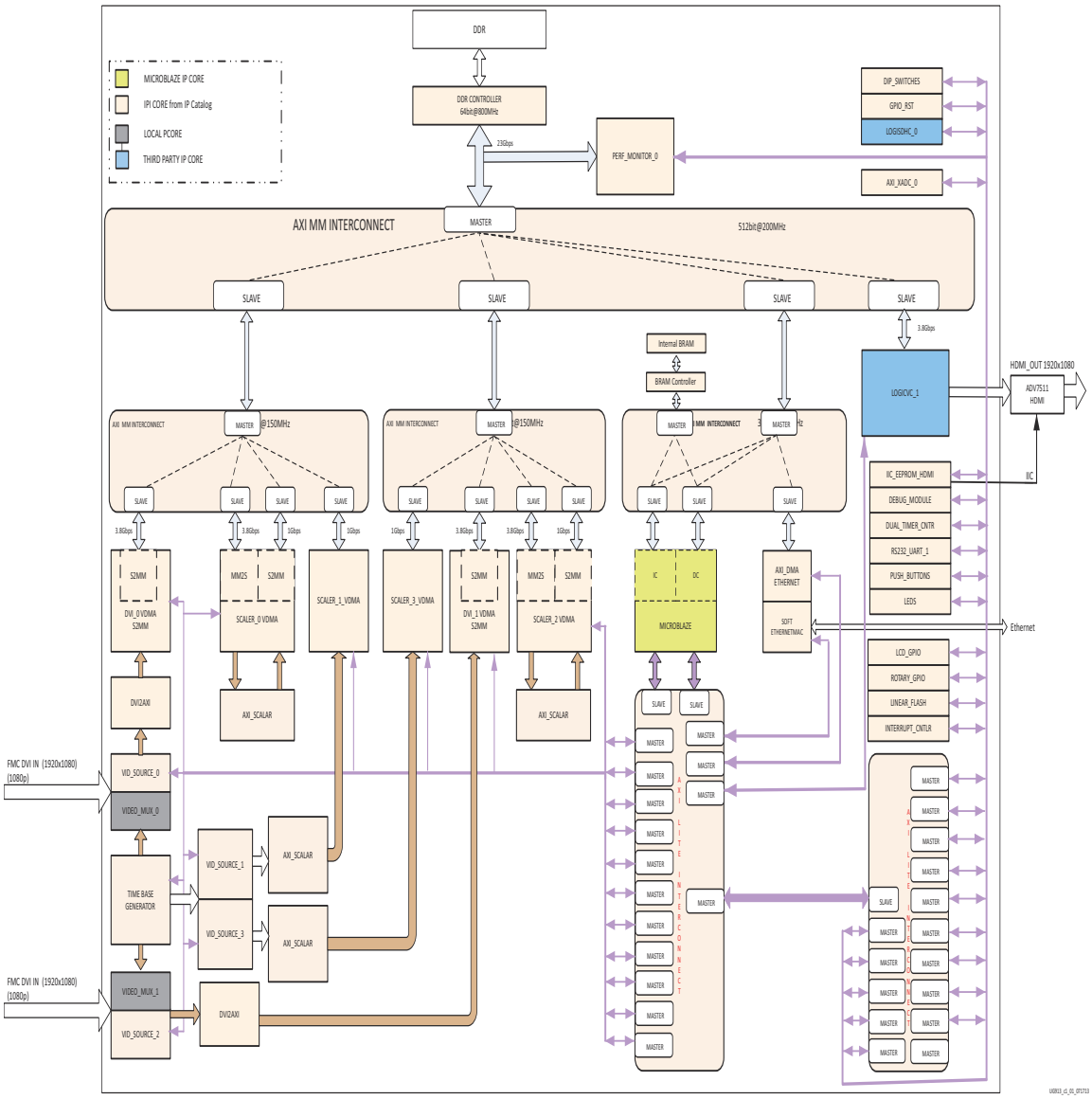


Figure 1-1: **Kintex-7 FPGA Video Demonstration System**

Video Demonstration Hardware

The following hardware is provided with the evaluation kit:

- KC705 evaluation board with the Kintex-7 XC7K325T-2FFG900C device
- USB-to-Mini-B cable (for UART)
- AC power adapter (12V DC)
- Digilent USB cable (for JTAG)

The following prerequisites are not provided with the evaluation kit:

- One external monitor capable of displaying 1080p video through high-definition multimedia interface (HDMI™) or digital visual interface (DVI)
- One HDMI-HDMI or HDMI-DVI cable

- A host PC with TeraTerm Pro terminal program
- Adobe SVG plug-in for Internet Explorer

Video Demonstration Hardware Setup Instructions

This demonstration requires default switch and jumper settings on the KC705 board. For more information on the default switch settings, see the *Hardware Test Board Setup Requirements* section of UG883, *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide (Vivado Design Suite)*. Ensure the following jumper settings for the video demonstration:

- Jumper 27: Short pins 2 and 3
- Jumper 28: Short pins 2 and 3
- Jumper 29: Short pins 1 and 2
- Jumper 30: Short pins 1 and 2
- Jumper 32: Short pins 5 and 6
- Jumper 47: Short pins 1 and 2
- Jumper 48: Short pins 2 and 3
- Jumper 69: Short pins 1 and 2
- Jumper 3: Short pins 1 and 2
- Jumper 4: Short pins 1 and 2
- Jumper 43: Short pins 1 and 2
- Jumper 65: Short pins 1 and 2
- Jumper 68: Short pins 1 and 2

1. Connect the KC705 board, HDMI cables, display monitor, Ethernet cable, and USB cables as shown in Figure 1-2.

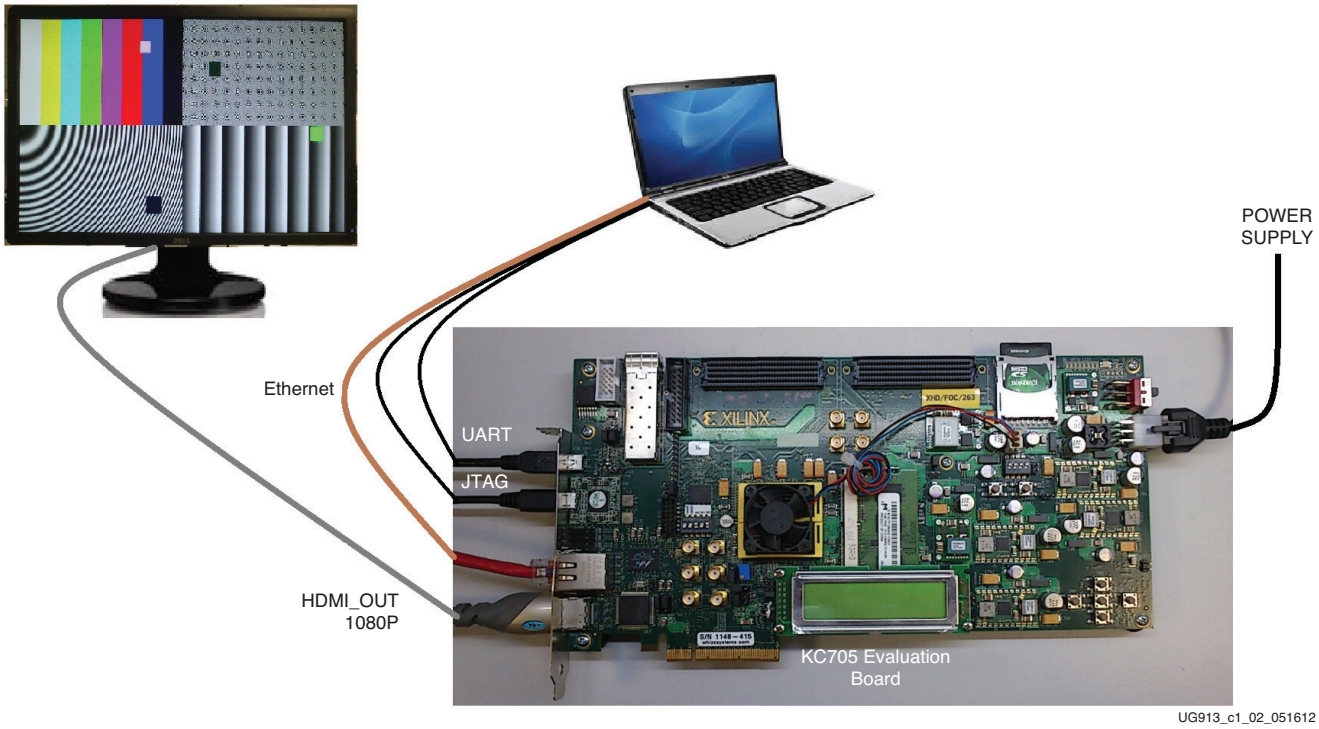


Figure 1-2: **Kintex-7 FPGA Video Demonstration Hardware Setup**

2. Set the IP address of the host PC to 192.168.1.100. Return the IP address of the PC back to its original setting after running the demonstration.

Note: The demonstration uses a hard-coded MAC address and a fixed IP address of 192.168.1.10 and does not connect to the regular LAN network using DHCP. Do not connect more than one board to the same network segment.

Running the Video Demonstration

To run the video demonstration, copy and unzip the demonstration package files from the Web to the host machine and use the following steps:

Note: Because the package has a deep hierarchy structure, unzip the package at a user location so that the overall path length is smaller.

1. If the KC705 board is not already powered on, plug in the power adapter to local AC power. Plug the 12V power cable into the board connector on J49. Turn on the power by switching the SW15 to the ON position.
2. Open and configure a serial communications terminal utility program with these settings:
   - Baud Rate: **9600**
   - Data: **8 bit**
   - Parity: **None**
   - Stop: **1 bit**
   - Flow Control: **None**

   Note: Refer to Appendix A, Communicating with the KC705 USB-UART for setting up the UART communication.

3. Open a command shell with the Xilinx Design tools environment settings. Refer to Appendix B, Installation and Licensing of Xilinx Design Tools for Xilinx tool chain installation and licensing help.

   Note: To set environment variables, run the `settings32.bat` file located in the Xilinx installation area. At the command prompt, type **`C:\Xilinx\Vivado\2013.x\settings32.bat`** (for Windows XP) or **`C:\Xilinx\Vivado\2013.x\settings64.bat`** (for Windows 7) and press **Enter**.

4. Go to the unzipped directory of the demonstration package and execute these commands to download the design and connect to the MicroBlaze processor:

   ```
   $ cd k7-embedded-trd-rdf0283/ready_to_test/
   ```

   ```
   $ xmd
   ```

   ```
   XMD% fpga -f video_demo.bit
   ```

   This command downloads the hardware bitstream into the FPGA but does not download the software application:

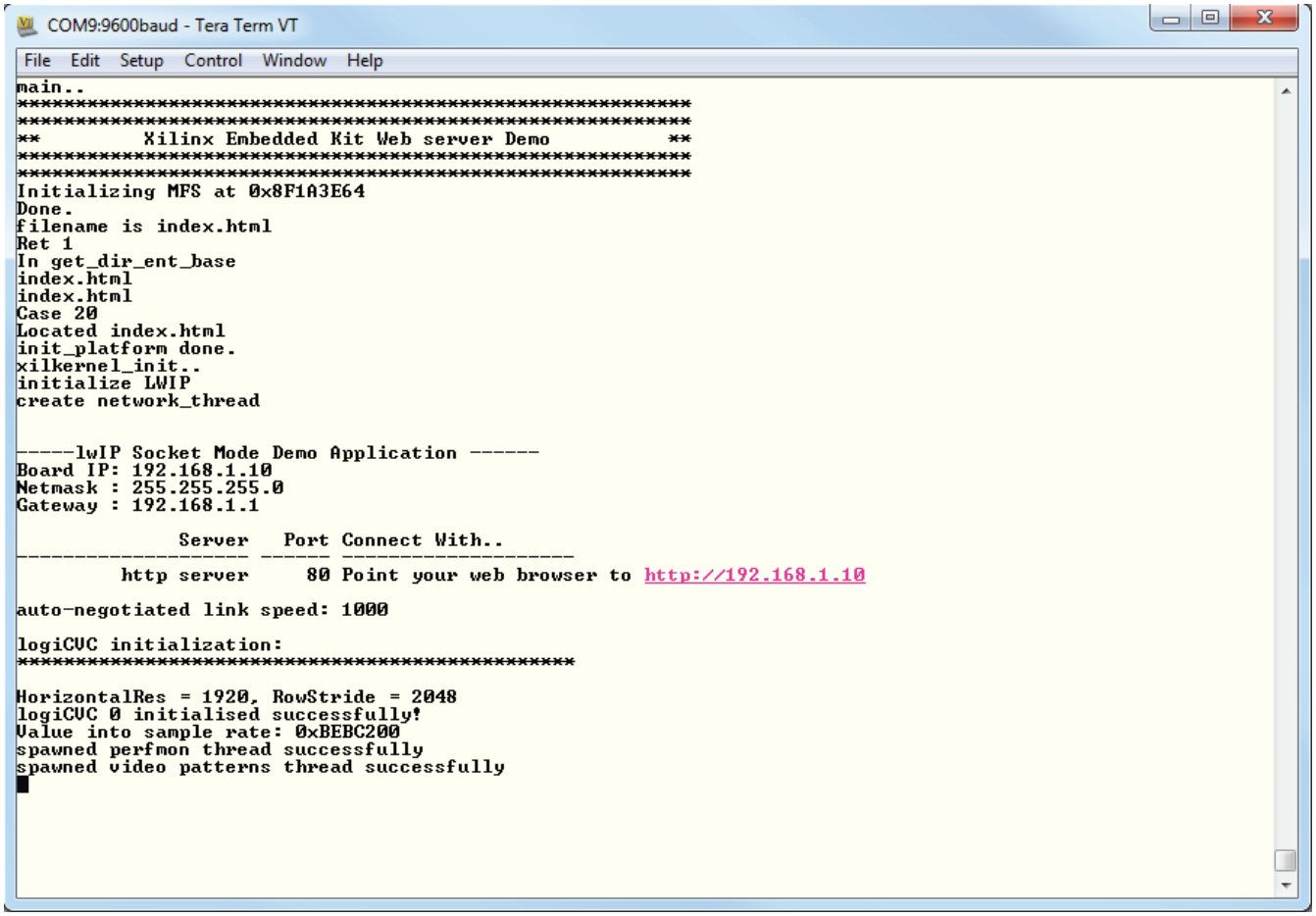
   ```
   XMD% connect mb mdm
   ```

   This command connects to the MicroBlaze processor debug module:

   ```
   XMD% dow Video_Demo.elf
   ```

   ```
   XMD% con
   ```

5. The UART output should be as shown in Figure 1-3.

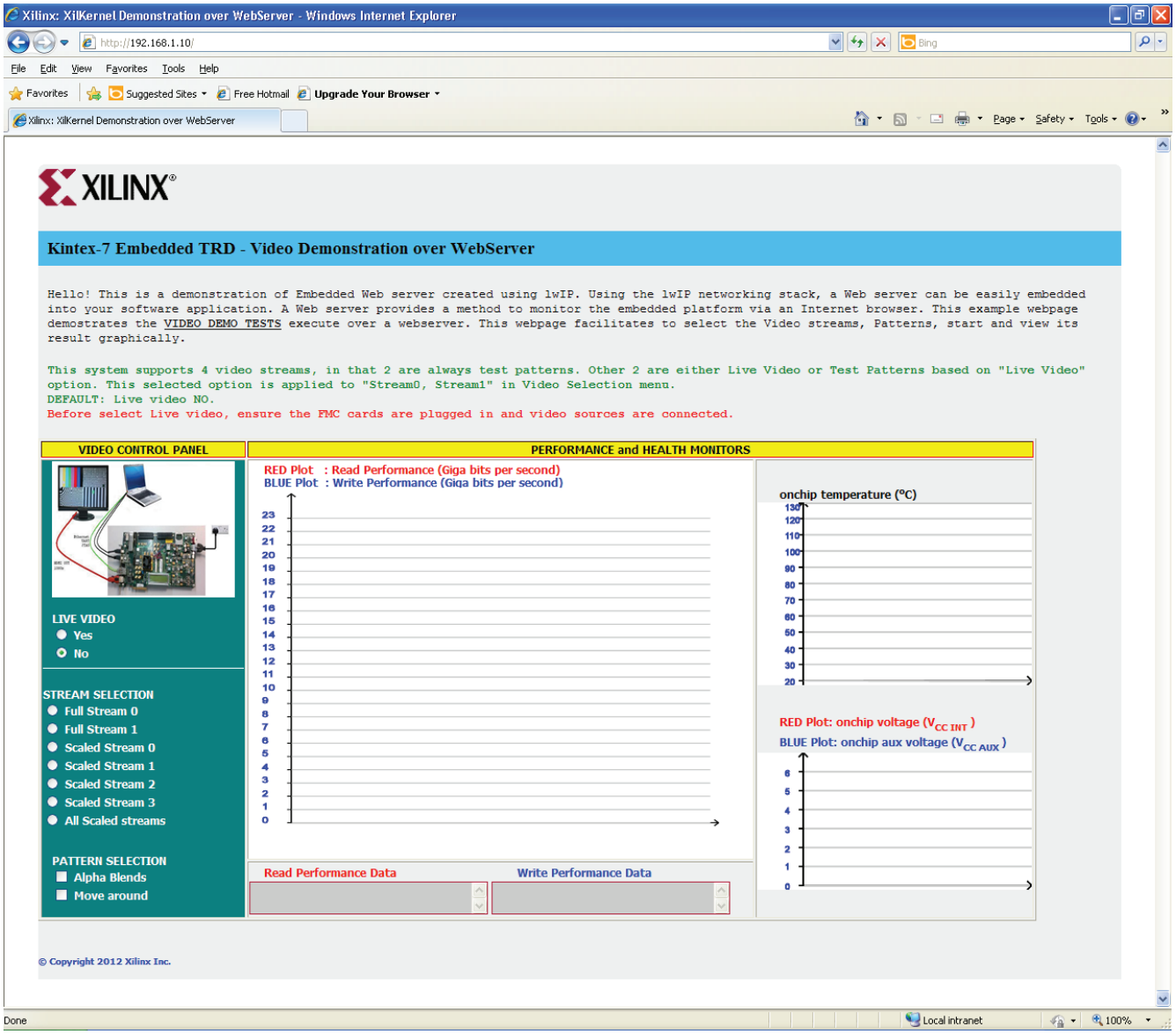


UG913_c1_03_050312

Figure 1-3: **Video Demonstration UART Output**

6. Open a Web browser on the host computer and set the URL to 192.168.1.10. The Web page shown in Figure 1-4 should be displayed. The page uses JavaScript, so the browser must have JavaScript enabled.

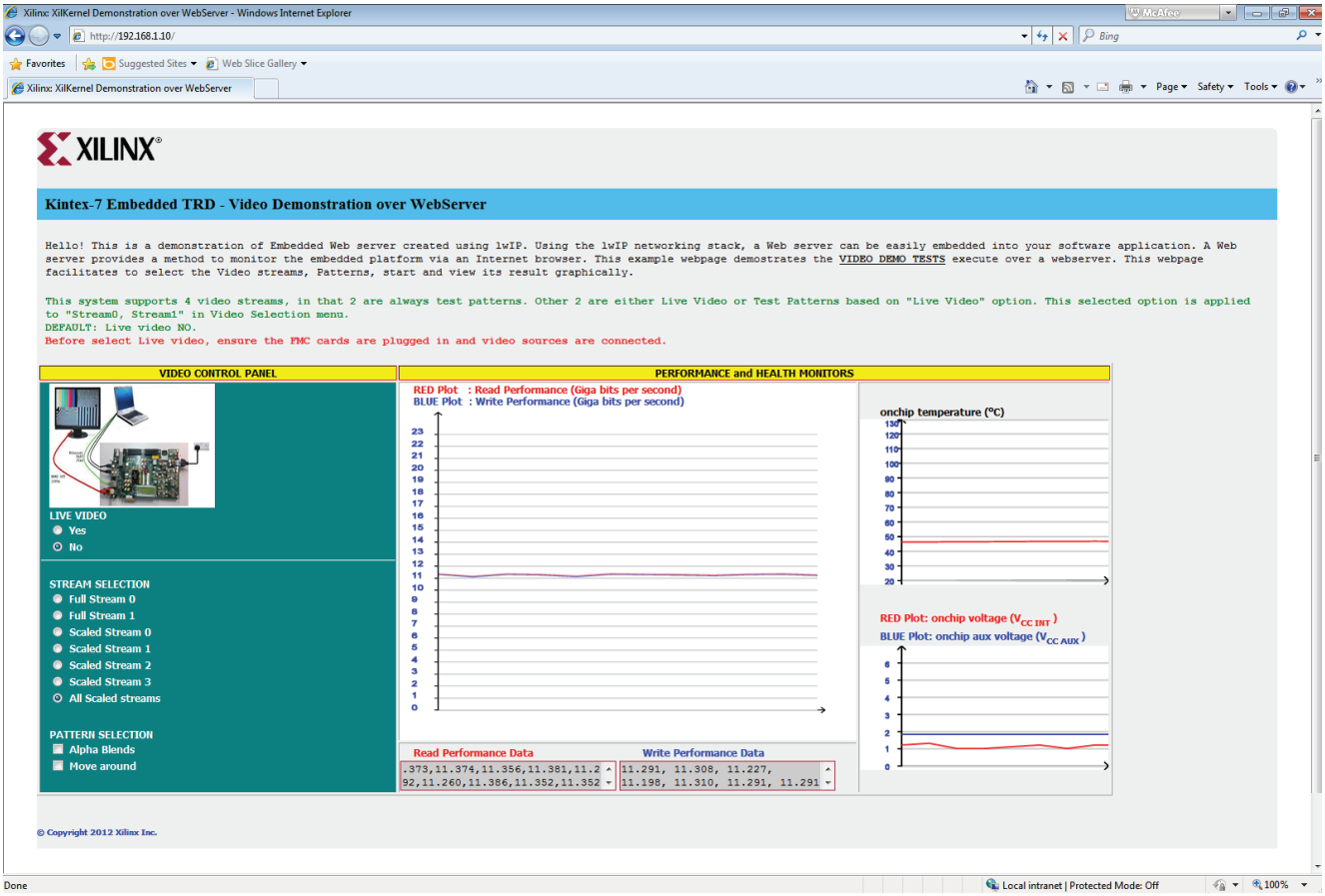
   Note: If using Internet Explorer, the Adobe SVG viewer plug-in or a similar plug-in that enables viewing of SVG files must be installed to view the graph. This demonstration is tested with Internet Explorer 8 on a Windows XP machine.



UG913_c1_04_080812

Figure 1-4: **Initial Video Demonstration Web Page**

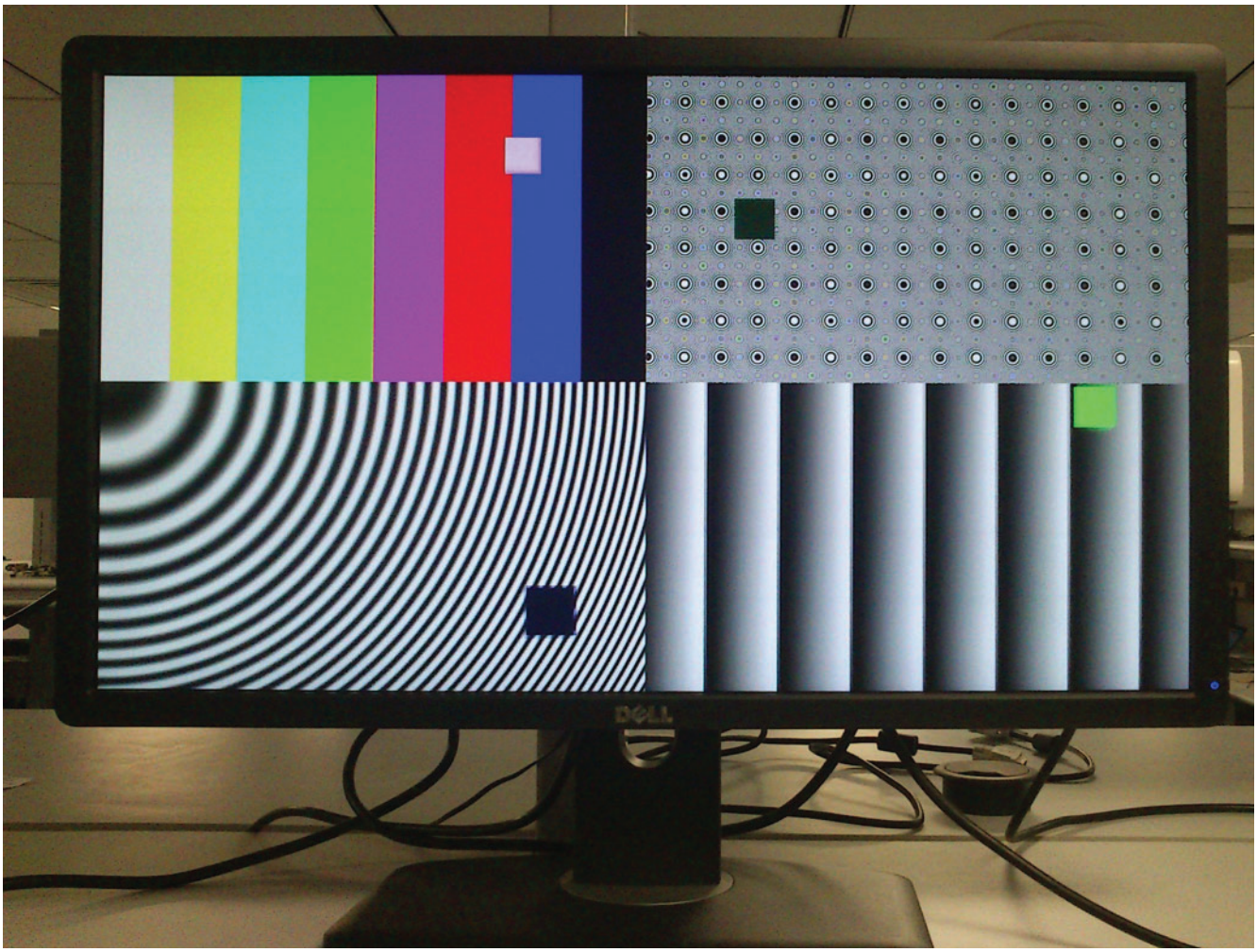
7. In the video demonstration Web page, make the following selections as shown in Figure 1-5:
   - Live Video: **No**
   - Stream Selection: **All Scaled streams**
8. The selected options take effect automatically. The performance, temperature, and voltage graphs are also plotted on the Web page (Figure 1-5).



UG913_c1_05_032313

Figure 1-5: **Video Demonstration Web Page with Data Plotted**

Figure 1-6 shows the output display for the selections made in step 7.



UG913_c1_06_051612

Figure 1-6: **Output Video Display**

The Web browser receives one packet of results at a time. This packet contain five results:

- Read throughput (Gb/s)
- Write throughput (Gb/s)
- On-chip temperature (°C)
- On-chip V_{CCINT} voltage (V)
- On-chip V_{CCAUX} voltage (V)

JavaScript is used to convert these results into coordinates and update the graphs. The graphs update every time a new data packet is received. The graph holds a maximum of 12 data points at a time. After the maximum has been reached, the oldest data point is dropped and the newest data point is added.

9. Repeat step 7 and step 8 to explore different VIDEO DEMO TESTS options by changing the selections mentioned in step 7.

Running BIST tests

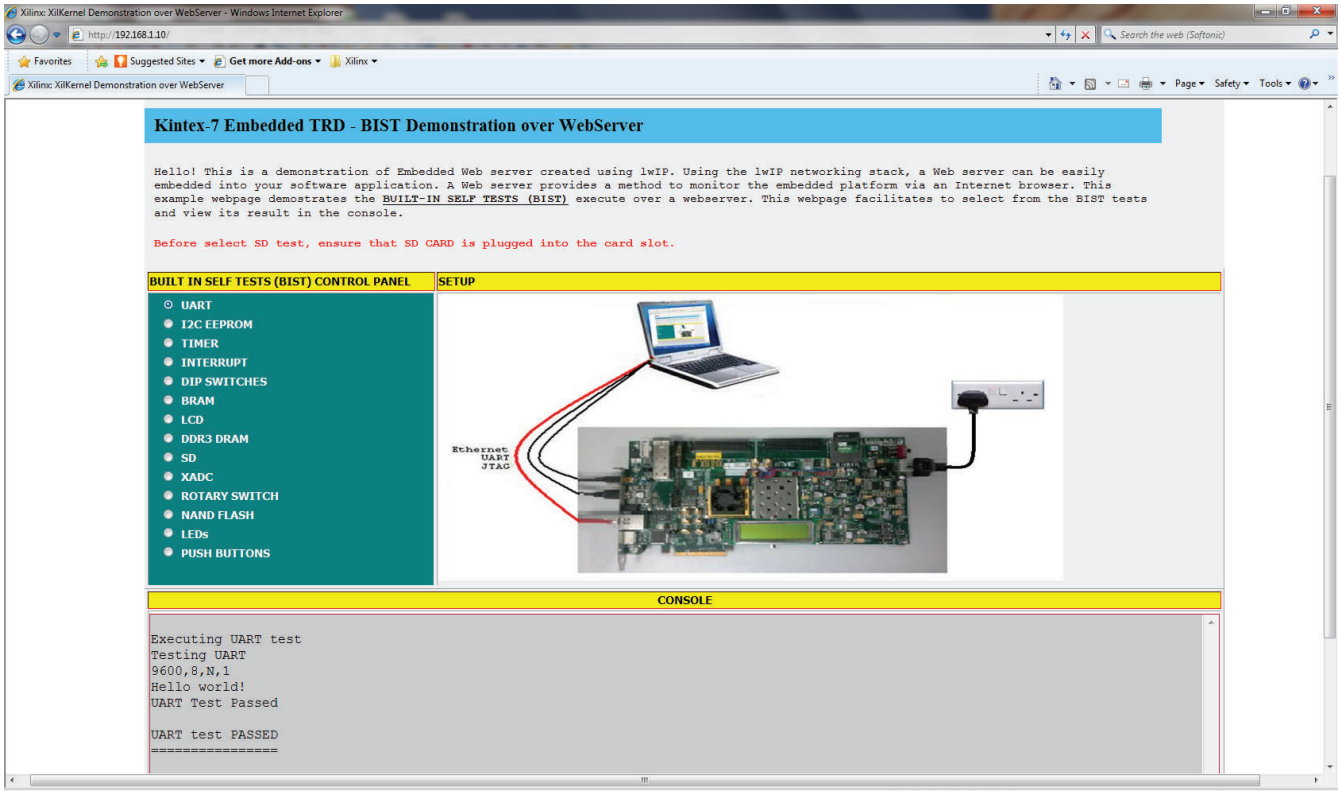
10. A Web server-based BIST demonstration can also be run on the same hardware to test different peripherals. Enter these commands at the XMD prompt to run the BIST demonstration:

```
XMD% stop

XMD% dow board_test_app_Webserver.elf

XMD% con
```

11. Reload the Web page with the same URL (192.168.1.10). The Web page should appear as shown in Figure 1-7.



UG913_c1_07_080912

Figure 1-7: **BIST Demonstration Web Page with DDR3 test results**

12. The left side of the Web page has different options for selecting the type of test to run on the hardware. For running any test, click the radio button corresponding to the test. The bottom of the Web page has a messaging section that displays the results of the tests.

The Video and BIST demonstrations using the KC705 board are complete. Because a fully configured MicroBlaze processor subsystem has been provided, the user can start developing embedded applications. Because an FPGA is being used, the processor subsystem can also be fully customized. To do this, the Xilinx Design Tools and the USB-UART driver must be installed on the computer (see Appendix B, Installation and Licensing of Xilinx Design Tools).

Next Steps

After running through an FPGA-based embedded processor demonstration and installing the Xilinx Design Tools, the user is ready to create custom embedded systems for the Kintex-7 XC7K325T FPGA.

Figure 1-8 is a snapshot of the directory structure in the `KC705_Embedded_Kit` folder from the Xilinx Kintex-7 FPGA Embedded Kit website. Xilinx recommends saving the files downloaded from this URL to a working area on the user's host computer.

Note: There should be no spaces in the path name of the working area on the host computer.

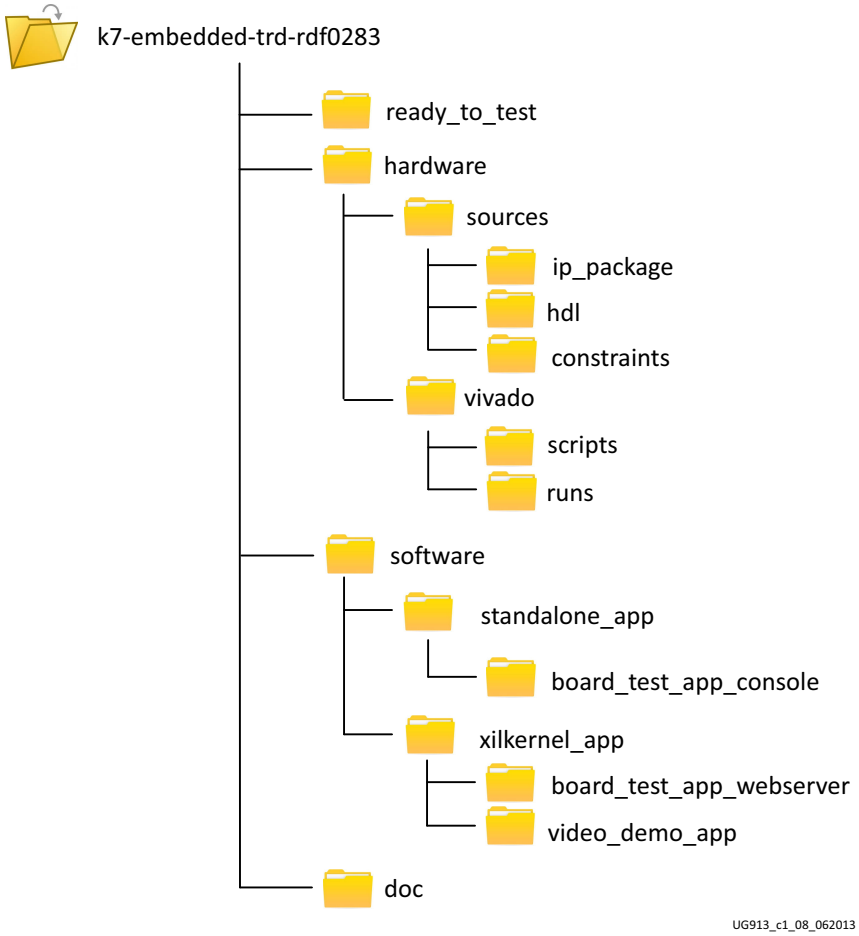


Figure 1-8: **KC705 Embedded Kit Directory Structure**

The `KC705_Embedded_Kit` directories and their content are explained in Table 1-1.

Table 1-1: **KC705 Embedded Kit Directory Structure Contents**

Directory	Purpose
`ready_to_test`	Includes pre-built hardware bitstream and software executable files to run both applications.
`hardware`	Includes hardware platform for BIST and video demonstration design.
`software`	Includes software platform for BIST and video demonstration design.
`doc`	Includes documents provided with this embedded kit.

Reference Designs

MicroBlaze Processor BIST Subsystem

- KC705_System
  - This is the base MicroBlaze processor subsystem including the software applications and platforms.

MicroBlaze Processor Video Subsystem

- Video_Demo
  - This is the MicroBlaze processor subsystem with the video cores that were run as the power-on demonstration. Source files for the demonstration including the software application and platform are included here.

Documentation

- Kintex-7 FPGA Embedded Kit Targeted Reference Design Documentation Advisory

Appendix A

Communicating with the KC705 USB-UART

This appendix explains the procedure for setting up UART communication between the KC705 board and the host machine.

Installing the USB-UART Driver

1. Execute the installer for the Silicon Labs USB-UART virtual COM port (VCP) driver from the `Drivers_and_Tools` folder in the package downloaded from the embedded kit home page: `Drivers_and_Tools\CP210x_VCP_Win2K_XP_S2K3.exe`.
2. Follow the installer instructions. Restart the computer when instructed to do so.

Connecting to the KC705 UART

3. Connect a USB Type-A to Mini-B 5-pin cable between the KC705 USB-UART connector (J21) and the host computer.
4. Power on the KC705 evaluation board if it is not already powered on.

Configuring the Host Computer

5. Right-click on **My Computer** and select **Properties**. Select the **Hardware** tab. Click on **Device Manager**.
6. Expand the **Ports (COM & LPT)** entry as shown in Figure A-1. This shows the COM port assigned to the **Silicon Labs CP210x USB to UART Bridge**. This is the COM port to use in the serial communications program.

   Note: The COM port setting for the user system might be different from the one shown in Figure A-1.

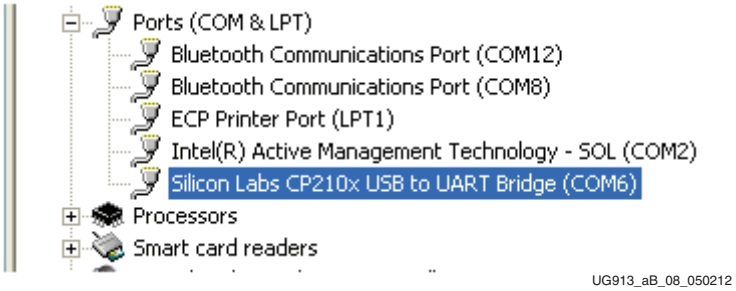


Figure A-1: **Silicon Labs USB to UART Bridge Properties**

If the Silicon Labs CP210x USB to UART bridge does not appear in the Ports list, a reboot of the computer might be required. After rebooting, repeat step 5 and step 6.

7. If using TeraTerm as the serial communications utility program, right-click on the **Silicon Labs CP210x USB to UART bridge** and select **Properties**.
   a. Click on the **Port Settings** tab and then click **Advanced**.
   b. Set the COM port to an open COM port setting from COM1 to COM4. The COM port setting for the user system might be different from the one shown in Figure A-2.

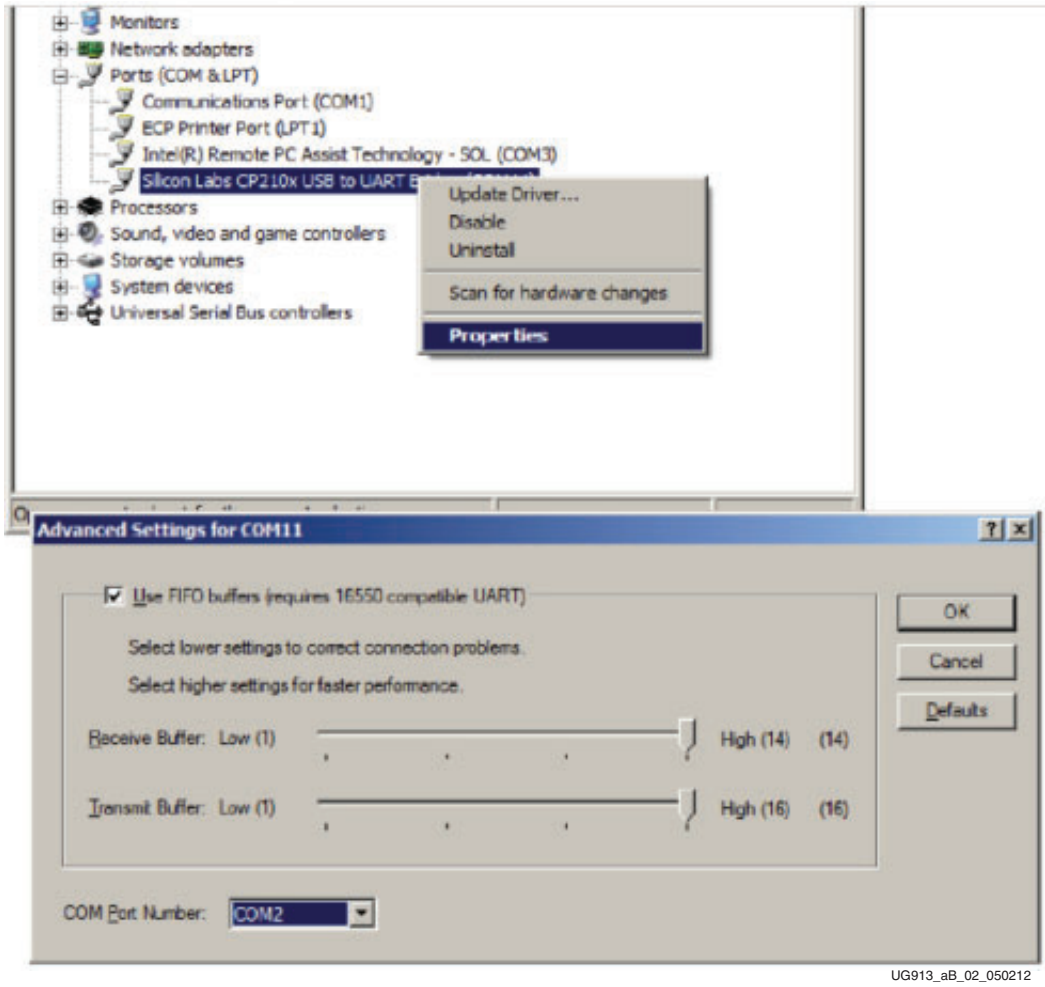


Figure A-2: **Setting the COM Port for the Silicon Labs USB to UART Bridge Driver**

8. Click **OK** to exit all open windows.

The Silicon Labs USB-UART VCP driver is now installed.

Appendix B

Installation and Licensing of Xilinx Design Tools

This KC705 embedded kit comes with entitlement to a full set of the Xilinx Design Tools that is device locked to the Kintex-7 XC7K325T device. This software can be installed from the DVD, or the Web installer can be downloaded from the Downloads website.

For detailed information on licensing and installation, see UG973, *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing*.

Getting Help and Support

For technical support including the installation and use of your product license file, see the Xilinx Support website. This site includes the following resources:

- Software, IP, and documentation updates
- Access to technical support web tools
- Searchable answer database with over 4,000 solutions
- User forums
- Training in the form of select instructor-led classes and recorded e-learning options

Appendix C

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

For a glossary of technical terms used in Xilinx documentation, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the KC705 board and its documentation is available on these websites.

Kintex-7 FPGA Embedded Kit

Kintex-7 FPGA Embedded Kit Answer Record (AR 52970)

Vivado Design Suite

UG883, *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide (Vivado Design Suite)*

UG985, *Kintex-7 FPGA Embedded Targeted Reference Design User Guide*

UG973, *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing*

Appendix D

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes: (i) engineering samples or beta versions of Development Systems (which are provided "AS-IS" without warranty); (ii) design defects or errors known as "errata"; (iii) Development Systems procured through unauthorized third parties; and (iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

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Email mkt@ameya360.com