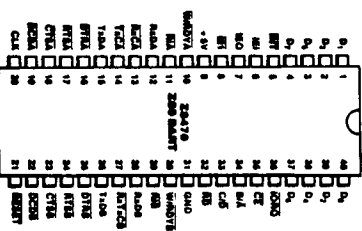


# Zilog

Z08470 Customer  
Procurement Spec (CPS)

## GENERAL DESCRIPTION

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel, multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial, converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.



40-Pin Dual-In-Line Package (DIP),  
Pin Assignments

Z80 is a registered trademark of Zilog, Inc.

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All rights reserved. Specifications (parameters) on products delivered in the future are subject to change without notice. All parameters are tested, except those which are characterized or guaranteed by design.

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00-2847-01

(MARC0M) DC2847 DOCUMENT CONTROL  
MASTER

**DC CHARACTERISTICS**

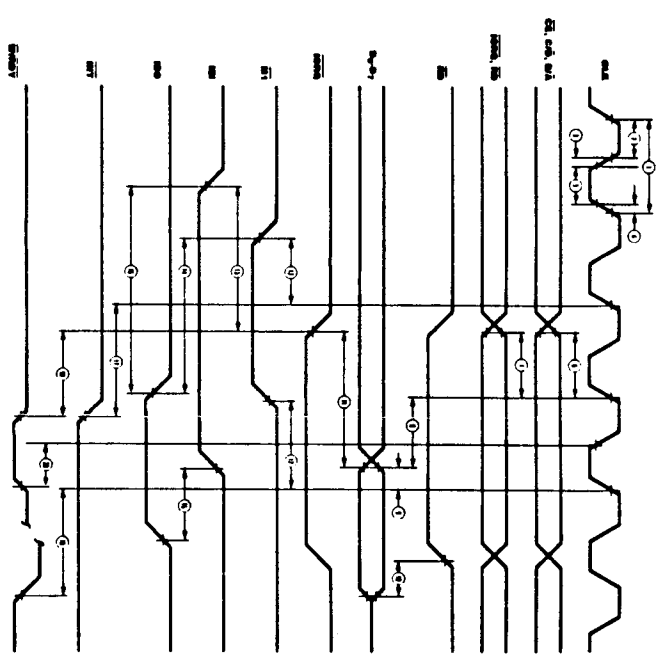
Symbol	Parameter	Min	Max	Units	Test Conditions
V <sub>CC</sub>	Clock Input Low Voltage	-0.2*	+0.45*	V	V <sub>CC</sub> = 2.0 mA 0.4 < V <sub>IN</sub> < 2.0 V 0.4 < V <sub>OUT</sub> < 2.0 V P <sub>AV</sub> < 100 mW
V <sub>CC</sub>	Clock Input High Voltage	V <sub>CC</sub> - 0.8*	+0.85*	V	
V <sub>IN</sub>	Input Low Voltage	-0.2*	+0.18*	V	
V <sub>IN</sub>	Input High Voltage	+2.0*	+0.85*	V	
V <sub>OH</sub>	Output Low Voltage	+0.4*	+0.4*	V	
V <sub>OH</sub>	Output High Voltage	+2.4*	V	V	
I <sub>OL</sub>	Input/3-State Output Leakage Current	-10*	+10*	µA	
I <sub>OH</sub>	Input/3-State Output Leakage Current	-40*	+10*	µA	
I <sub>CC</sub>	Power Supply Current		100*	mA	
V <sub>CE</sub>	Power Supply Current		100*	mA	

\* Tested  
 † Guaranteed by Design  
 ‡ Guaranteed by Characterization

**AC CHARACTERISTICS\***

Number	Symbol	Parameter	280-4 DART		280-6 DART	
			Min	Max	Min	Max
1	T <sub>DC</sub>	Clock Cycle Time	250*	4000*	185*	4000*
2	T <sub>HCH</sub>	Clock Width (High)	105*	2000*	70*	2000*
3	T <sub>TC</sub>	Clock Fall Time		30*		15*
4	T <sub>CC</sub>	Clock Rise Time		30*		15*
5	T <sub>DCI</sub>	Clock Width (Low)	105*	2000*	70*	2000*
6	T <sub>ANDQ</sub>	CE, C <sub>EN</sub> Setup to Clock Setup Time	145*		80*	
7	T <sub>ANDQ</sub>	RE, RD Setup to Clock Setup Time	115*		80*	
8	T <sub>ANDQ</sub>	Clock 1 to Data Out Delay		220*		150*
9	T <sub>ANDQ</sub>	Data In to Clock 1 Setup (Write or Hit Cycle)	50*		30*	
10	T <sub>ANDQ</sub>	RD to Data Out Read Delay		110*		80*
11	T <sub>ANDQ</sub>	RE, RD to Data Out Delay (TRACK Cycle)		180*		100*
12	T <sub>ANDQ</sub>	RT to Clock 1 Setup Time	80*		75*	
13	T <sub>ANDQ</sub>	RT to RE, RD Setup Time (TRACK Cycle)	140*		120*	
14	T <sub>ANDQ</sub>	RT to RE, RD Delay (format before hit)	180*		180*	
15	T <sub>ANDQ</sub>	RT to RE, RD Delay (after ED decode)	100*		70*	
16	T <sub>ANDQ</sub>	RT to RE, RD Delay	100*		70*	
17	T <sub>ANDQ</sub>	Clock 1 to RT Delay	200*		150*	
18	T <sub>ANDQ</sub>	RE, RD or CE 1 to W/RDY Delay (Ready Mode)	210*		175*	
19	T <sub>ANDQ</sub>	Clock 1 to W/RDY Delay (Ready Mode)	120*		100*	
20	T <sub>ANDQ</sub>	Clock 1 to W/RDY Read Delay (Ready Mode)	130*		110*	

\* Units in microseconds (µs)  
 † Tested  
 ‡ Guaranteed by Design  
 ‣ Guaranteed by Characterization



**AC CHARACTERISTICS (Continued)**

Number	Symbol	Parameter	280-4 DART		280-6 DART	
			Min	Max	Min	Max
1	T <sub>WH</sub>	Pulse Width (High)	200*	200*		
2	T <sub>WL</sub>	Pulse Width (Low)	200*	200*		
3	T <sub>CHC</sub>	CE Cycle Time	400*	300*	300*	300*
4	T <sub>WCH</sub>	CE Width (Low)	180*	100*	100*	100*
5	T <sub>WCH</sub>	CE Width (High)	180*	100*	100*	100*
6	T <sub>ANDQ</sub>	CE 1 to RD Delay	300*		220*	
7	T <sub>ANDQ</sub>	CE 1 to W/RDY Delay (Ready Mode)	5*	9*	5*	9*
8	T <sub>ANDQ</sub>	CE 1 to RT Delay	5*	9*	5*	9*
9	T <sub>ANDQ</sub>	RE Cycle Time	400*	300*	300*	300*
10	T <sub>ANDQ</sub>	RE Width (Low)	180*	100*	100*	100*
11	T <sub>ANDQ</sub>	RE Width (High)	180*	100*	100*	100*
12	T <sub>ANDQ</sub>	RD to RE, RD Setup Time (Hit Mode)	0*	0*	0*	0*
13	T <sub>ANDQ</sub>	RD Hold Time (Hit Mode)	140*	100*		
14	T <sub>ANDQ</sub>	RE 1 to W/RDY Delay (Ready Mode)	10*	13*	10*	13*
15	T <sub>ANDQ</sub>	RE 1 to RT Delay	10*	13*	10*	13*

\* In all modes, the System Clock rate must be at least five times the maximum data rate. RESET must be active a minimum of one complete clock cycle.  
 † Units equal to System Clock Period.  
 ‡ Units in microseconds (µs)  
 ‣ Tested  
 ․ Guaranteed by Design  
 ‥ Guaranteed by Characterization

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