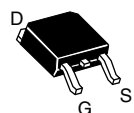


## Power MOSFET

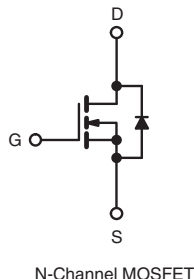
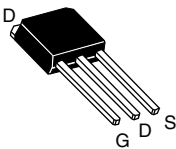
### PRODUCT SUMMARY

$V_{DS}$ (V)	400	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	3.6
$Q_g$ (Max.) (nC)	12	
$Q_{gs}$ (nC)	1.9	
$Q_{gd}$ (nC)	6.5	
Configuration	Single	

DPAK  
(TO-252)



IPAK  
(TO-251)



### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR310, SiHFR310)
- Straight Lead (IRFU310, SiHFU310)
- Available in Tape and Reel
- Fast Switching
- Fully Avalanche Rated
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

### ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR310-GE3	SiHFR310TRL-GE3	SiHFR310TR-GE3	SiHFR310TRR-GE3	SiHFU310-GE3
Lead (Pb)-free	IRFR310PbF	IRFR310TRLPbF <sup>a</sup>	IRFR310TRPbF <sup>a</sup>	IRFR310TRRPbF <sup>a</sup>	IRFU310PbF
	SiHFR310-E3	SiHFR310TL-E3 <sup>a</sup>	SiHFR310T-E3 <sup>a</sup>	SiHFR310TR-E3 <sup>a</sup>	SiHFU310-E3

#### Note

a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	400	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	6.0	W/ $^{\circ}\text{C}$
Linear Derating Factor		0.20	
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.020	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	86	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	1.7	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	2.5	mJ
Maximum Power Dissipation	$P_D$	$T_C = 25\text{ }^{\circ}\text{C}$	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>		$T_A = 25\text{ }^{\circ}\text{C}$	
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	4.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s	260	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 52\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 1.7\text{ A}$  (see fig. 12).
- $I_{SD} \leq 1.7\text{ A}$ ,  $dI/dt \leq 40\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^{\circ}\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	50	°C/W
Maximum Junction-to-Ambient	$R_{thJA}$	-	110	
Maximum Junction-to-Case	$R_{thJC}$	-	5.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

**SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		400	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.47	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 320 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.0 A <sup>b</sup>	-	-	3.6	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.0 A <sup>b</sup>		0.97	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5 <sup>c</sup>		-	170	-	pF
Output Capacitance	C <sub>OSS</sub>			-	34	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	6.3	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.0 A, V <sub>DS</sub> = 320 V, see fig. 6 and 13 <sup>b, c</sup>	-	-	12	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	1.9	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	6.5	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 200 V, I <sub>D</sub> = 2.0 A, R <sub>g</sub> = 24 Ω, R <sub>D</sub> = 95 Ω, see fig. 10 <sup>b, c</sup>		-	7.9	-	ns
Rise Time	t <sub>r</sub>			-	9.9	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	21	-	
Fall Time	t <sub>f</sub>			-	11	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	1.7	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	6.0	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.6	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 2.0 A, dI/dt = 100 A/μs <sup>b</sup>		-	240	540	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.85	1.6	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

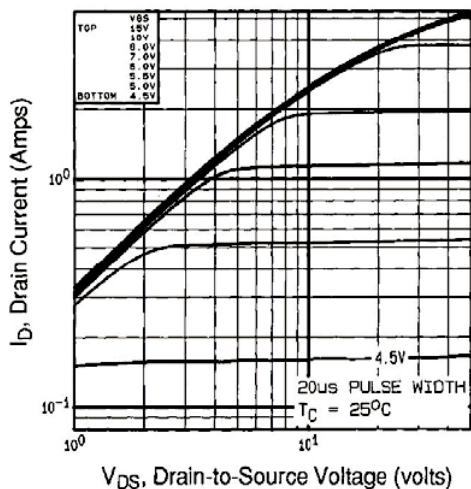


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

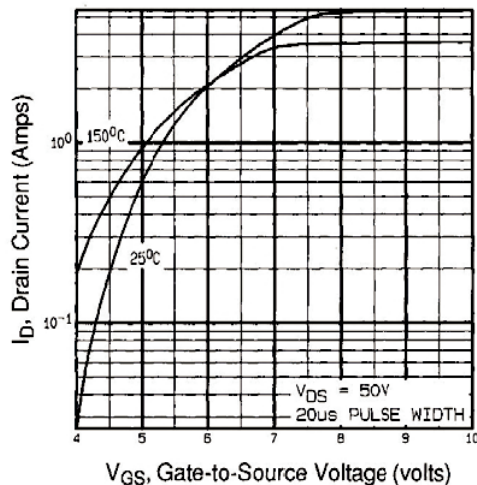


Fig. 3 - Typical Transfer Characteristics

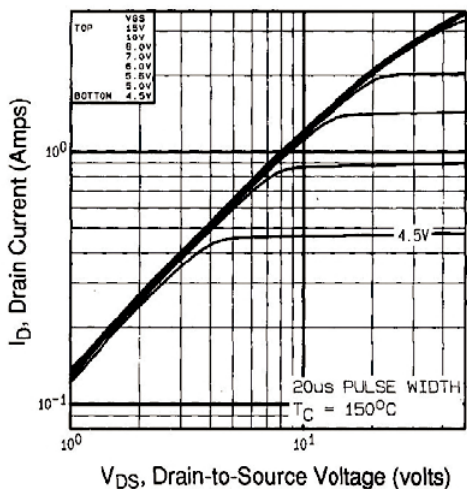


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$

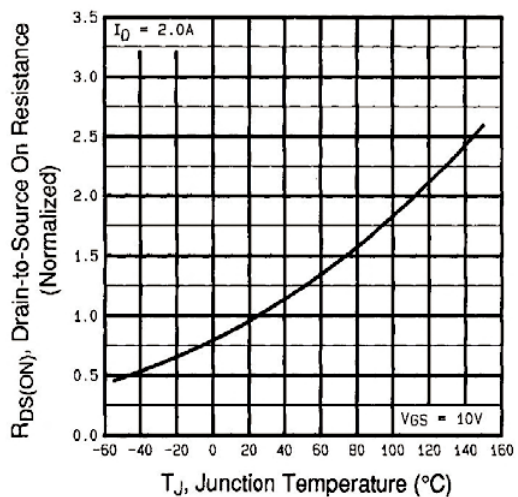


Fig. 4 - Normalized On-Resistance vs. Temperature

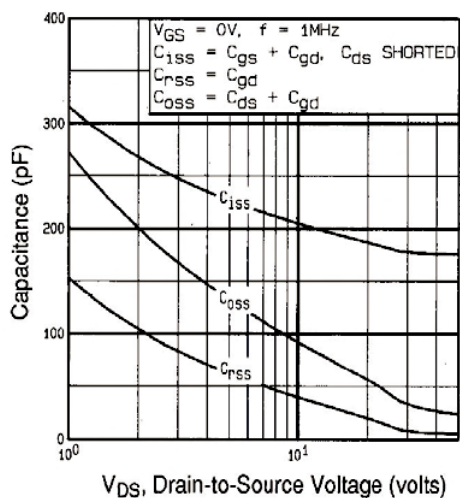


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

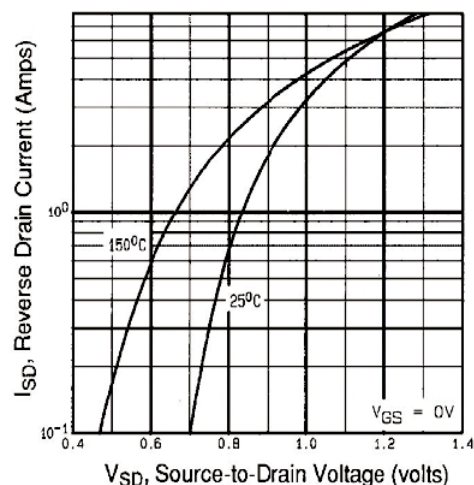


Fig. 7 - Typical Source-Drain Diode Forward Voltage

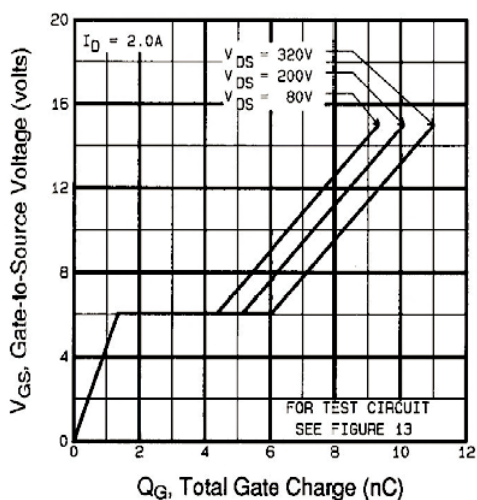


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

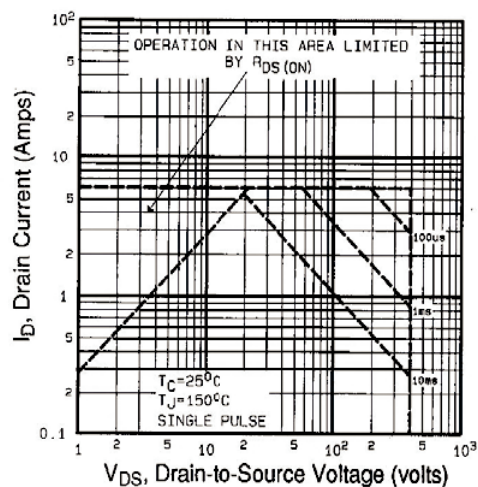


Fig. 8 - Maximum Safe Operating Area

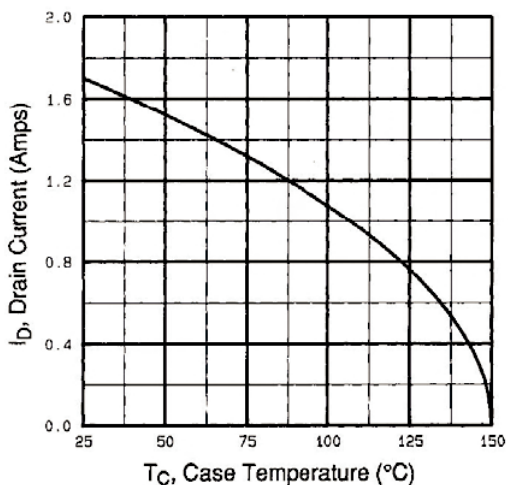


Fig. 9 - Maximum Drain Current vs. Case Temperature

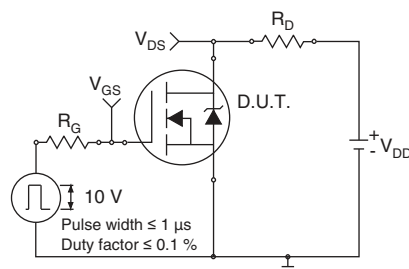


Fig. 10a - Switching Time Test Circuit

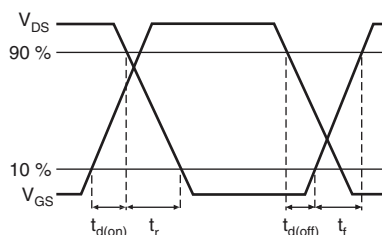


Fig. 10b - Switching Time Waveforms

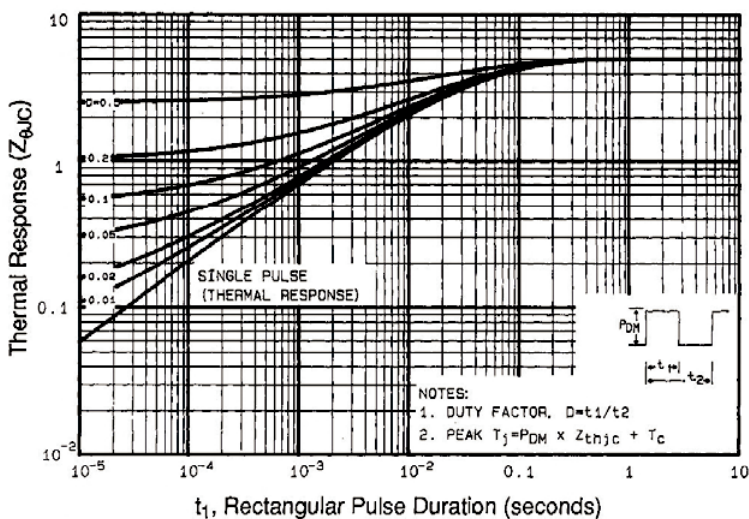


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

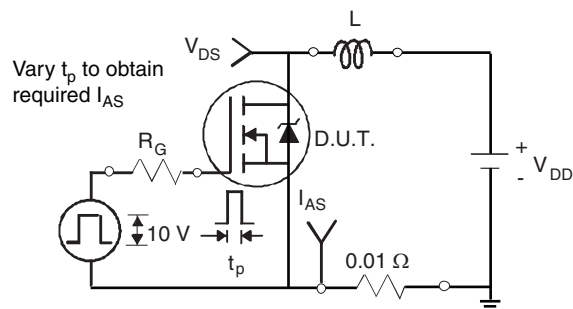


Fig. 12a - Unclamped Inductive Test Circuit

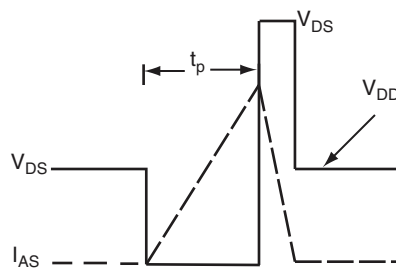


Fig. 12b - Unclamped Inductive Waveforms

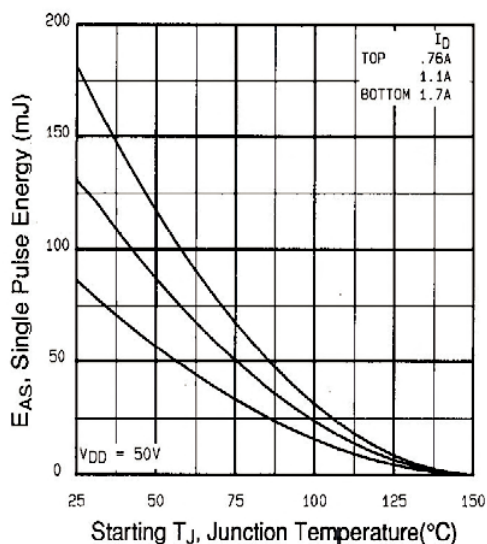


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

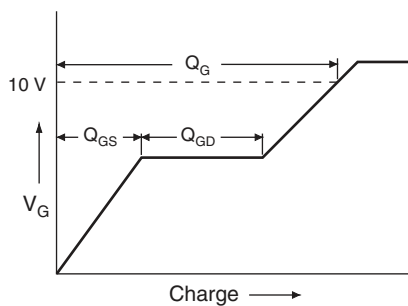


Fig. 13a - Basic Gate Charge Waveform

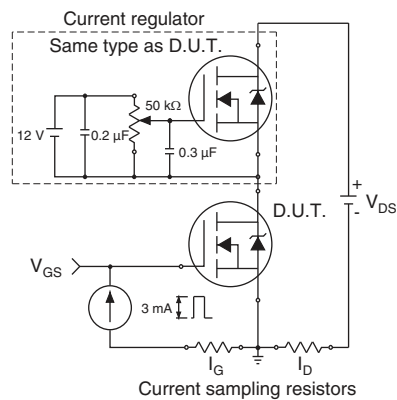
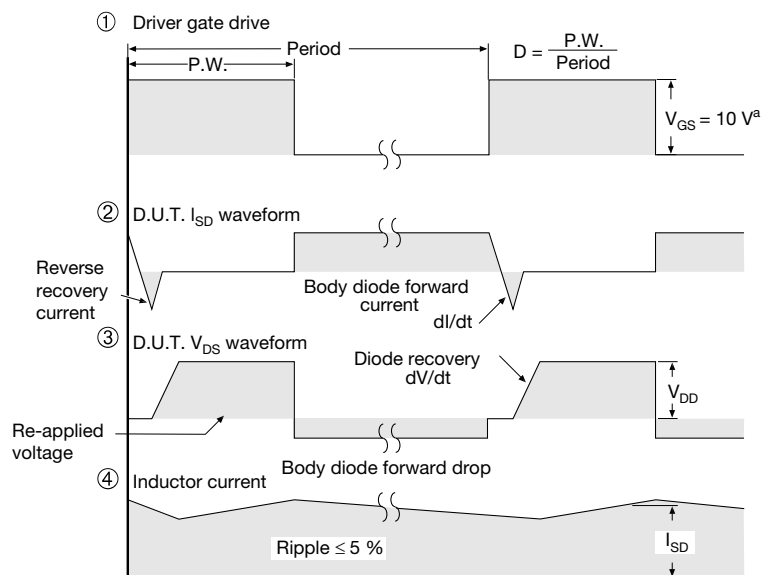
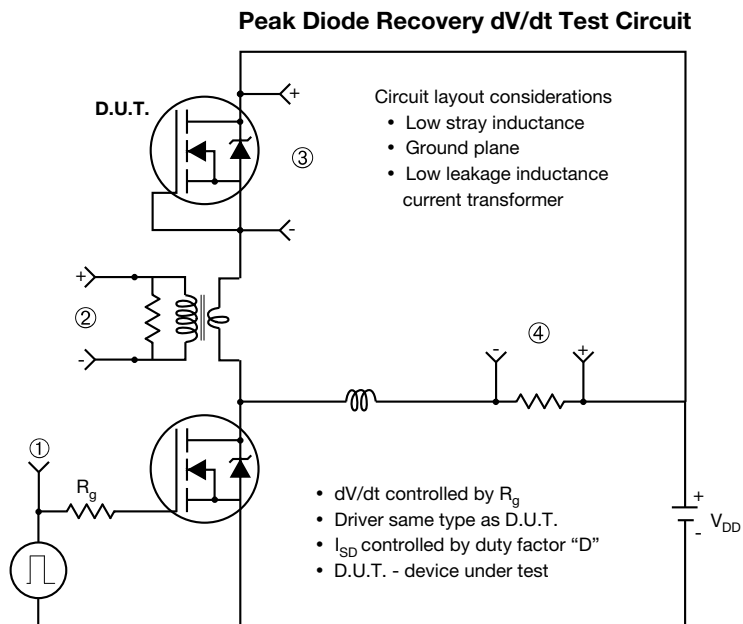


Fig. 13b - Gate Charge Test Circuit



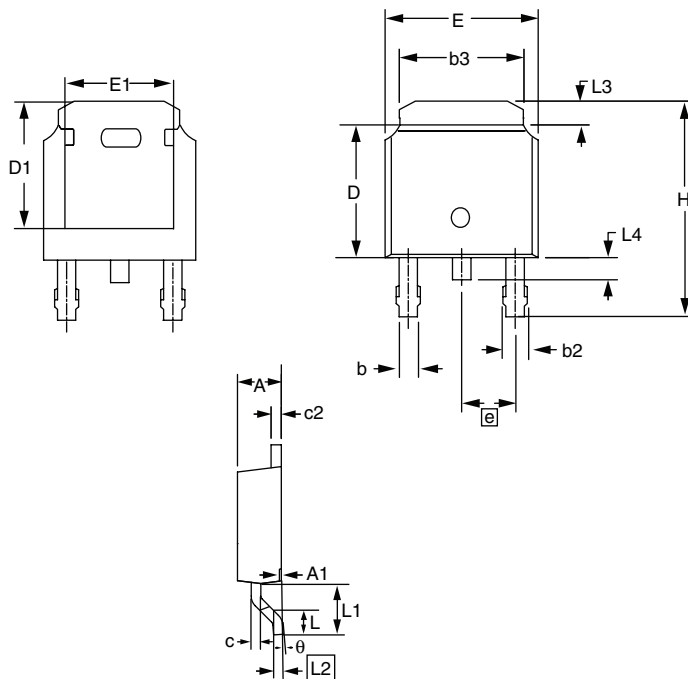
**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91272](http://www.vishay.com/ppg?91272).

## TO-252AA (HIGH VOLTAGE)



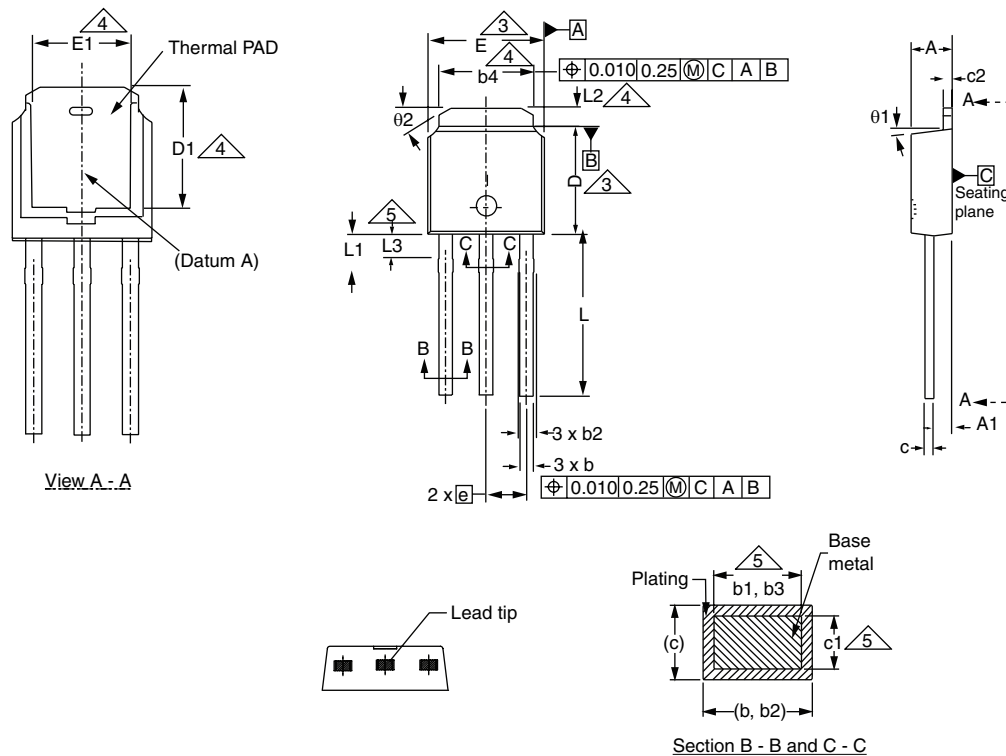
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
E	6.40	6.73	0.252	0.265
L	1.40	1.77	0.055	0.070
L1	2.743 REF		0.108 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.89	1.27	0.035	0.050
L4	0.64	1.01	0.025	0.040
D	6.00	6.22	0.236	0.245
H	9.40	10.40	0.370	0.409
b	0.64	0.88	0.025	0.035
b2	0.77	1.14	0.030	0.045
b3	5.21	5.46	0.205	0.215
e	2.286 BSC		0.090 BSC	
A	2.20	2.38	0.087	0.094
A1	0.00	0.13	0.000	0.005
c	0.45	0.60	0.018	0.024
c2	0.45	0.58	0.018	0.023
D1	5.30	-	0.209	-
E1	4.40	-	0.173	-
θ	0°	10°	0°	10°

ECN: S-81965-Rev. A, 15-Sep-08  
DWG: 5973

### Notes

1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

## TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

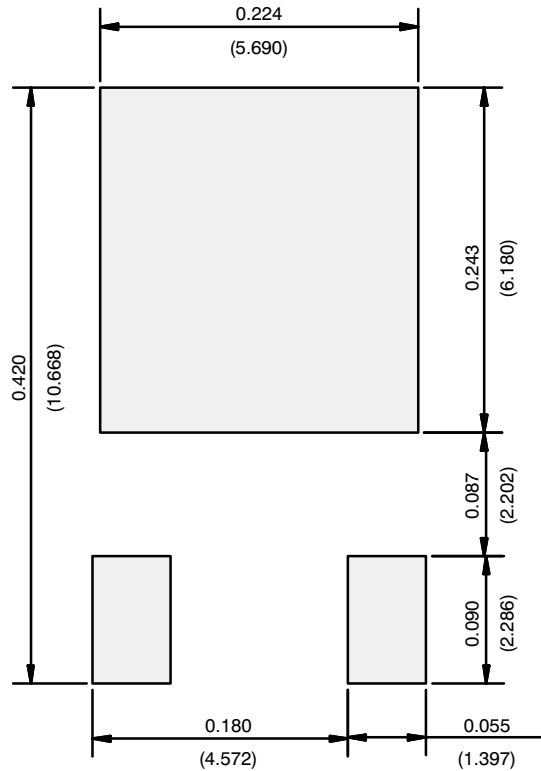
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: S-82111-Rev. A, 15-Sep-08  
DWG: 5968

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**

# AMEYA360

Components Supply Platform

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