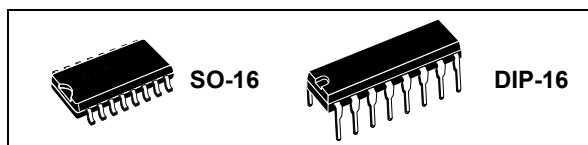


High voltage high/low-side driver

Datasheet - production data



Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
290 mA source, 430 mA sink
- Switching times 75/35 nsec rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Operational amplifier for advanced current sensing
- Comparator for fast fault protection
- Smart shutdown function
- Adjustable deadtime
- Interlocking function
- Compact and simplified layout
- Bill of material reduction

Applications

- Home appliances
- Motor drivers
 - DC, AC, PMDC and PMAC motors
 - FOC and sensorless BEMF detection systems
- Industrial applications and drives
- Induction heating
- HVAC
- Factory automation
- Power supply systems

Description

The L6390 is a full featured high voltage device manufactured with the BCD™ “offline” technology. It is a single-chip half-bridge gate driver for N-channel power MOSFETs or IGBTs. The high-side (floating) section is able to work with voltage rail up to 600 V.

Both device outputs can sink and source 430 mA and 290 mA respectively. Prevention from cross conduction is ensured by interlocking and programmable deadtime functions.

The device has dedicated input pins for each output and a shutdown pin. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing with control devices. Matched delays between low-side and high-side sections guarantee no cycle distortion and allow high frequency operation.

The L6390 embeds an operational amplifier suitable for advanced current sensing in applications such as field oriented motor control or for sensorless BEMF detection. A comparator featuring advanced smartSD function is also integrated in the device, ensuring fast and effective protection against fault events like overcurrent, overtemperature, etc.

The L6390 device features also UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions.

The integrated bootstrap diode as well as all of the integrated features of this IC make the application PCB design easier, more compact and simple thus reducing the overall bill of material.

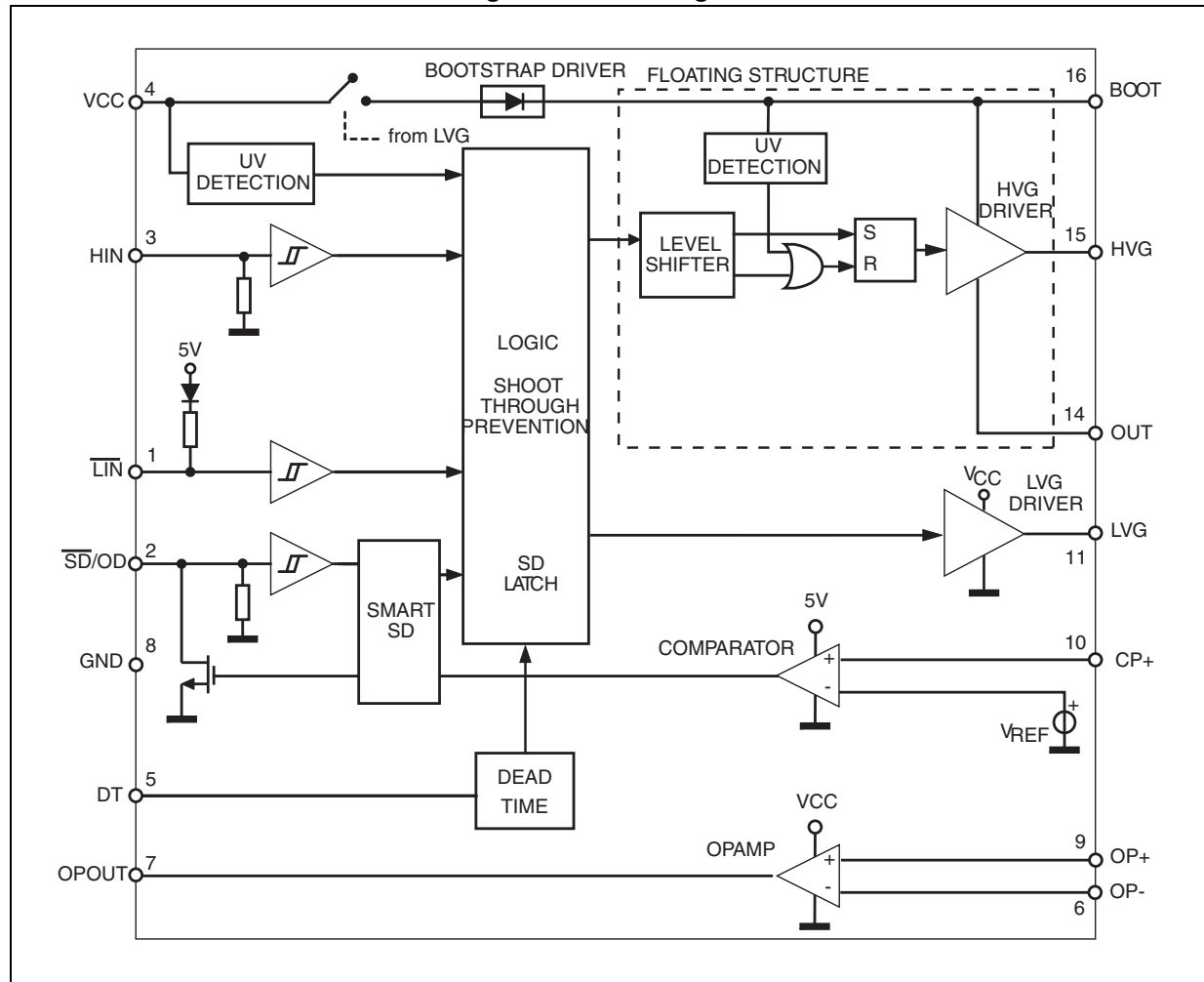
The device is available in a DIP-16 tube and SO-16 tube, and tape and reel packaging options.

Contents

1	Block diagram	3
2	Pin connection	4
3	Truth table	5
4	Electrical data	6
4.1	Absolute maximum ratings	6
4.2	Thermal data	6
4.3	Recommended operating conditions	7
5	Electrical characteristics	8
5.1	AC operation	8
5.2	DC operation	10
6	Waveforms definition	13
7	Smart shutdown function	14
8	Typical application diagram	17
9	Bootstrap driver	18
	C _{BOOT} selection and charging	18
10	Package information	20
11	Order codes	23
12	Revision history	24

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

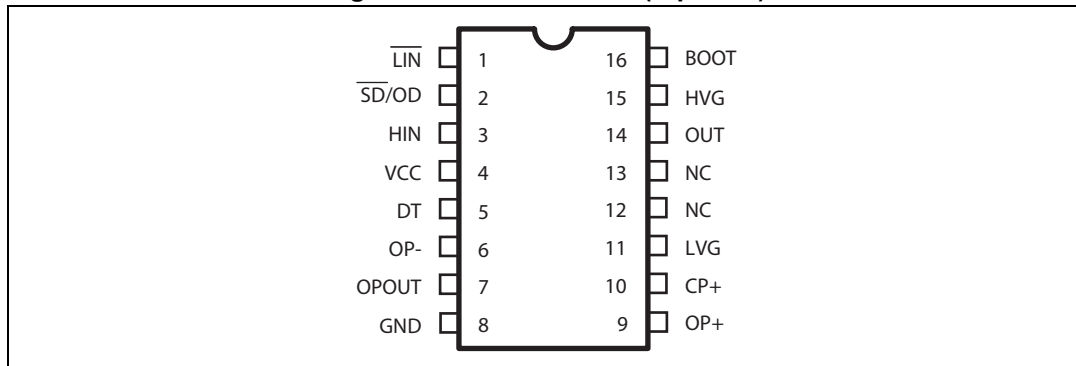


Table 1. Pin description

Pin n #	Pin name	Type	Function
1	$\overline{\text{LIN}}$	I	Low-side driver logic input (active low)
2	$\overline{\text{SD/OD}}^{(1)}$	I/O	Shutdown logic input (active low)/open drain (comparator output)
3	HIN	I	High-side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Deadtime setting
6	OP-	I	Op amp inverting input
7	OPOUT	O	Op amp output
8	GND	P	Ground
9	OP+	I	Op amp non-inverting input
10	CP+	I	Comparator input
11	LVG ⁽¹⁾	O	Low-side driver output
12, 13	NC		Not connected
14	OUT	P	High-side (floating) common voltage
15	HVG ⁽¹⁾	O	High-side driver output
16	BOOT	P	Bootstrap supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (at $I_{\text{sink}} = 10 \text{ mA}$), with $V_{\text{CC}} > 3 \text{ V}$. This allows the omission of the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

3 Truth table

Table 2. Truth table

Input			Output	
$\overline{\text{SD}}$	$\overline{\text{LIN}}$	HIN	LVG	HVG
L	X ⁽¹⁾	X ⁽¹⁾	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

1. X: don't care.

4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{CC}	Supply voltage	- 0.3	21	V
V_{out}	Output voltage	$V_{boot} - 21$	$V_{boot} + 0.3$	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{hvg}	High-side gate output voltage	$V_{out} - 0.3$	$V_{boot} + 0.3$	V
V_{lvg}	Low-side gate output voltage	- 0.3	$V_{CC} + 0.3$	V
V_{op+}	Op amp non-inverting input	- 0.3	$V_{CC} + 0.3$	V
V_{op-}	Op amp inverting input	- 0.3	$V_{CC} + 0.3$	V
V_{cp+}	Comparator input voltage	- 0.3	$V_{CC} + 0.3$	V
V_i	Logic input voltage	- 0.3	15	V
V_{od}	Open drain voltage	- 0.3	15	V
dV_{out}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation ($T_A = 25\text{ °C}$)		800	mW
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	SO-16	DIP-16	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	155	100	°C/W

4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
V_{CC}	4	Supply voltage		12.5	20	V
$V_{BO}^{(1)}$	16 - 14	Floating supply voltage		12.4	20	V
V_{out}	14	DC output voltage		- 9 ⁽²⁾	580	V
f_{sw}		Switching frequency	HVG, LVG load $C_L = 1$ nF		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{BO} = V_{boot} - V_{out}$.

2. LVG off. $V_{CC} = 12.5$ V. Logic is operational if $V_{boot} > 5$ V. Refer to the AN2738 for more details.

5 Electrical characteristics

5.1 AC operation

Table 6. AC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ }^{\circ}\text{C}$)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{on}	1 vs. 11	High/low-side driver turn-on propagation delay	$V_{out} = 0\text{ V}$ $V_{boot} = V_{CC}$ $C_L = 1\text{ nF}$ $V_i = 0\text{ to }3.3\text{ V}$ See Figure 3 .	50	125	200	ns
t_{off}	3 vs. 15	High/low-side driver turn-off propagation delay		50	125	200	ns
t_{sd}	2 vs. 11, 15	Shutdown to high/low-side driver propagation delay		50	125	200	ns
t_{isd}		Comparator triggering to high/low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CP+.	50	200	250	ns
MT		Delay matching, HS and LS turn-on/off				30	ns
DT	5	Deadtime setting range ⁽¹⁾	$R_{DT} = 0, C_L = 1\text{ nF}$	0.1	0.18	0.25	μs
			$R_{DT} = 37\text{ k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$	0.48	0.6	0.72	μs
			$R_{DT} = 136\text{ k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$	1.35	1.6	1.85	μs
			$R_{DT} = 260\text{ k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$	2.6	3.0	3.4	μs
MDT		Matching deadtime ⁽²⁾	$R_{DT} = 0, C_L = 1\text{ nF}$			80	ns
			$R_{DT} = 37\text{ k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$			120	ns
			$R_{DT} = 136\text{ k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$			250	ns
			$R_{DT} = 260\text{ k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$			400	ns
t_r	11, 15	Rise time	$C_L = 1\text{ nF}$		75	120	ns
t_f		Fall time	$C_L = 1\text{ nF}$		35	70	ns

1. See [Figure 4](#).

2. $MDT = |DT_{LH} - DT_{HL}|$ see [Figure 5 on page 13](#).

Figure 3. Timing

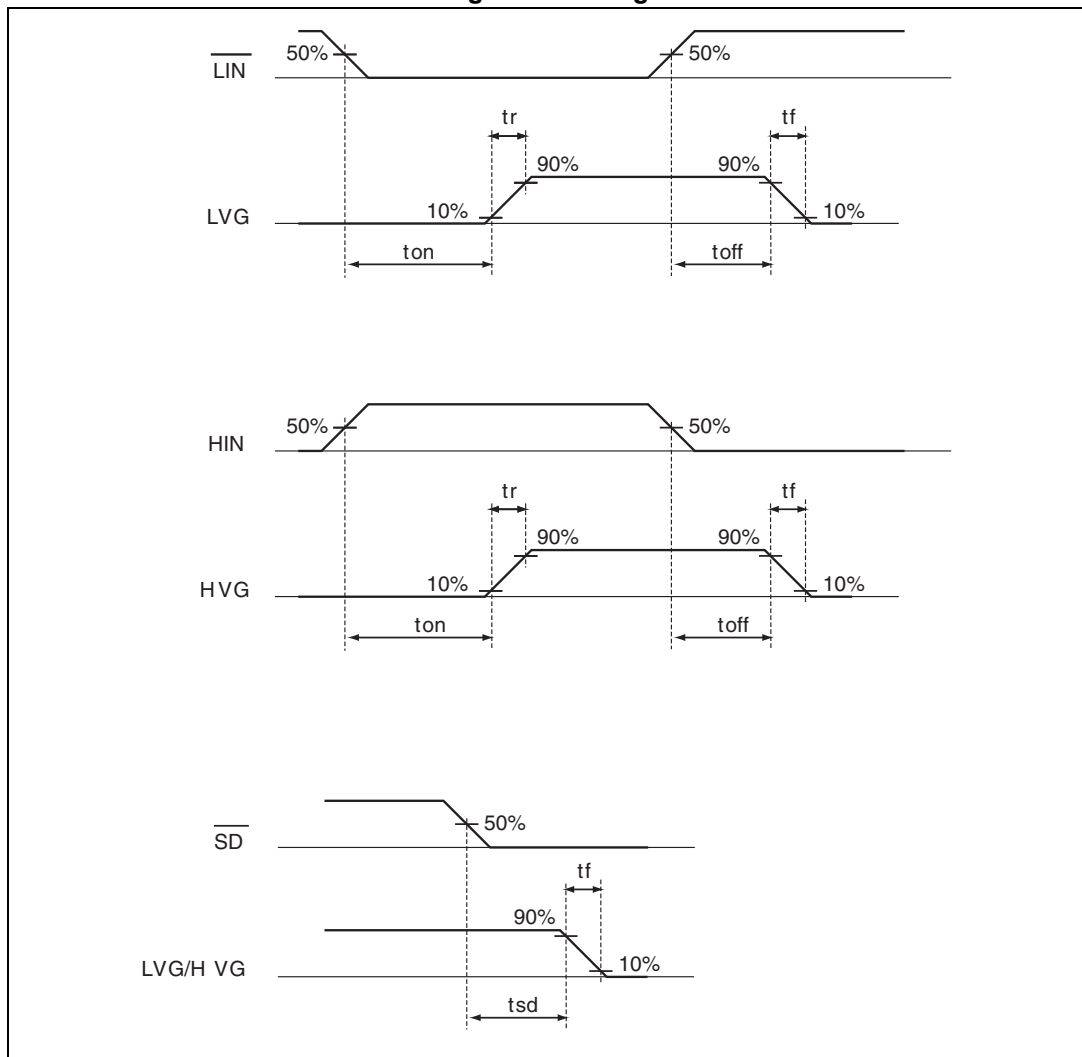
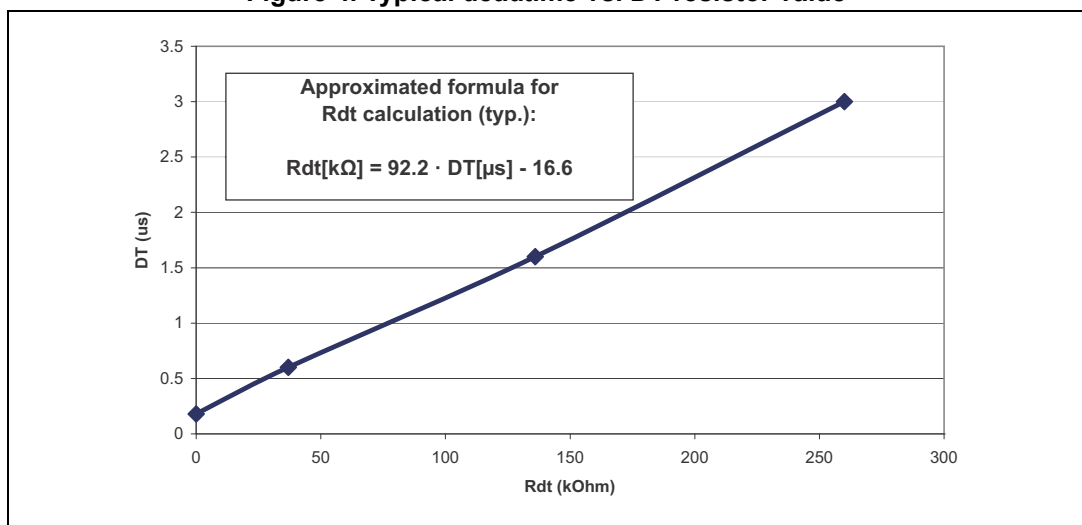


Figure 4. Typical deadtime vs. DT resistor value



5.2 DC operation

Table 7. DC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ }^{\circ}\text{C}$)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low supply voltage section							
V_{CC_hys}	4	V_{CC} UV hysteresis		1200	1500	1800	mV
V_{CC_thON}		V_{CC} UV turn-ON threshold		11.5	12	12.5	V
V_{CC_thOFF}		V_{CC} UV turn-OFF threshold		10	10.5	11	V
I_{qccu}		Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $HIN = GND$; $R_{DT} = 0\text{ }\Omega$; $CP+ = OP+ = GND$; $OP- = 5\text{ V}$	90	120	150	μA
I_{qcc}		Quiescent current	$V_{CC} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $HIN = GND$; $R_{DT} = 0\text{ }\Omega$; $CP+ = OP+ = GND$; $OP- = 5\text{ V}$	300	720	1000	μA
V_{ref}		Internal reference voltage		500	540	580	mV
Bootstrapped supply voltage section⁽¹⁾							
V_{BO_hys}	16	V_{BO} UV hysteresis		1200	1500	1800	mV
V_{BO_thON}		V_{BO} UV turn-ON threshold		11.1	11.5	12.1	V
V_{BO_thOFF}		V_{BO} UV turn-OFF threshold		9.8	10	10.6	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	$V_{BO} = 9\text{ V}$ $\overline{SD} = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $R_{DT} = 0\text{ }\Omega$; $CP+ = OP+ = GND$; $OP- = 5\text{ V}$	30	70	110	μA
I_{QBO}		V_{BO} quiescent current	$V_{BO} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $R_{DT} = 0\text{ }\Omega$; $CP+ = OP+ = GND$; $OP- = 5\text{ V}$	30	150	240	μA
I_{LK}		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot} = 600\text{ V}$			10	μA
$R_{DS(on)}$		Bootstrap driver on-resistance ⁽²⁾	LVG ON		120		Ω

Table 7. DC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ }^{\circ}\text{C}$) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Driving buffers section							
I _{so}	11, 15	High/low-side source short-circuit current	V _{IN} = V _{ih} (t _p < 10 μs)	200	290		mA
I _{si}		High/low-side sink short-circuit current	V _{IN} = V _{il} (t _p < 10 μs)	250	430		mA
Logic inputs							
V _{il}	1, 2, 3	Low level logic threshold voltage		0.8		1.1	V
V _{ih}		High level logic threshold voltage		1.9		2.25	V
V _{il_S}	1, 3	Single input voltage	$\overline{\text{LIN}}$ and HIN connected together and floating			0.8	V
I _{HINh}	3	HIN logic “1” input bias current	HIN = 15 V	110	175	260	μA
I _{HINI}		HIN logic “0” input bias current	HIN = 0 V			1	μA
I _{LINI}	1	$\overline{\text{LIN}}$ logic “0” input bias current	$\overline{\text{LIN}}$ = 0 V	3	6	20	μA
I _{LINh}		$\overline{\text{LIN}}$ logic “1” input bias current	$\overline{\text{LIN}}$ = 15 V			1	μA
I _{SDh}	2	$\overline{\text{SD}}$ logic “1” input bias current	$\overline{\text{SD}}$ = 15 V	10	40	100	μA
I _{SDI}		$\overline{\text{SD}}$ logic “0” input bias current	$\overline{\text{SD}}$ = 0 V			1	μA

1. $V_{BO} = V_{boot} - V_{out}$.

2. $R_{DS(on)}$ is tested in the following way: $R_{DS(on)} = [(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})] / [I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})]$ where I_1 is the pin 16 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

Table 8. Op amp characteristics⁽¹⁾ ($V_{CC} = 15\text{ V}$, $T_J = +25\text{ °C}$)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{io}	6, 9	Input offset voltage	V _{ic} = 0 V, V _o = 7.5 V			6	mV
I _{io}		Input offset current	V _{ic} = 0 V, V _o = 7.5 V		4	40	nA
I _{ib}		Input bias current ⁽²⁾			100	200	nA
V _{icm}		Input common mode voltage range		0		V _{CC} -4	V
V _{OPOUT}	7	Output voltage swing	OPOUT = OP-; no load	0.07		V _{CC} -4	V
I _o		Output short-circuit current	Source, V _{id} = +1; V _o = 0 V	16	30		mA
			Sink, V _{id} = -1; V _o = V _{CC}	50	80		mA
SR		Slew rate	V _i = 1 ÷ 4 V; C _L = 100 pF; unity gain	2.5	3.8		V/μs
GBWP		Gain bandwidth product	V _o = 7.5 V	8	12		MHz
A _{vd}		Large signal voltage gain	R _L = 2 kΩ	70	85		dB
SVR		Supply voltage rejection ratio	vs. V _{CC}	60	75		dB
CMRR		Common mode rejection ratio		55	70		dB

1. The operational amplifier is disabled when V_{CC} is in UVLO condition.

2. The direction of the input current is out of the IC.

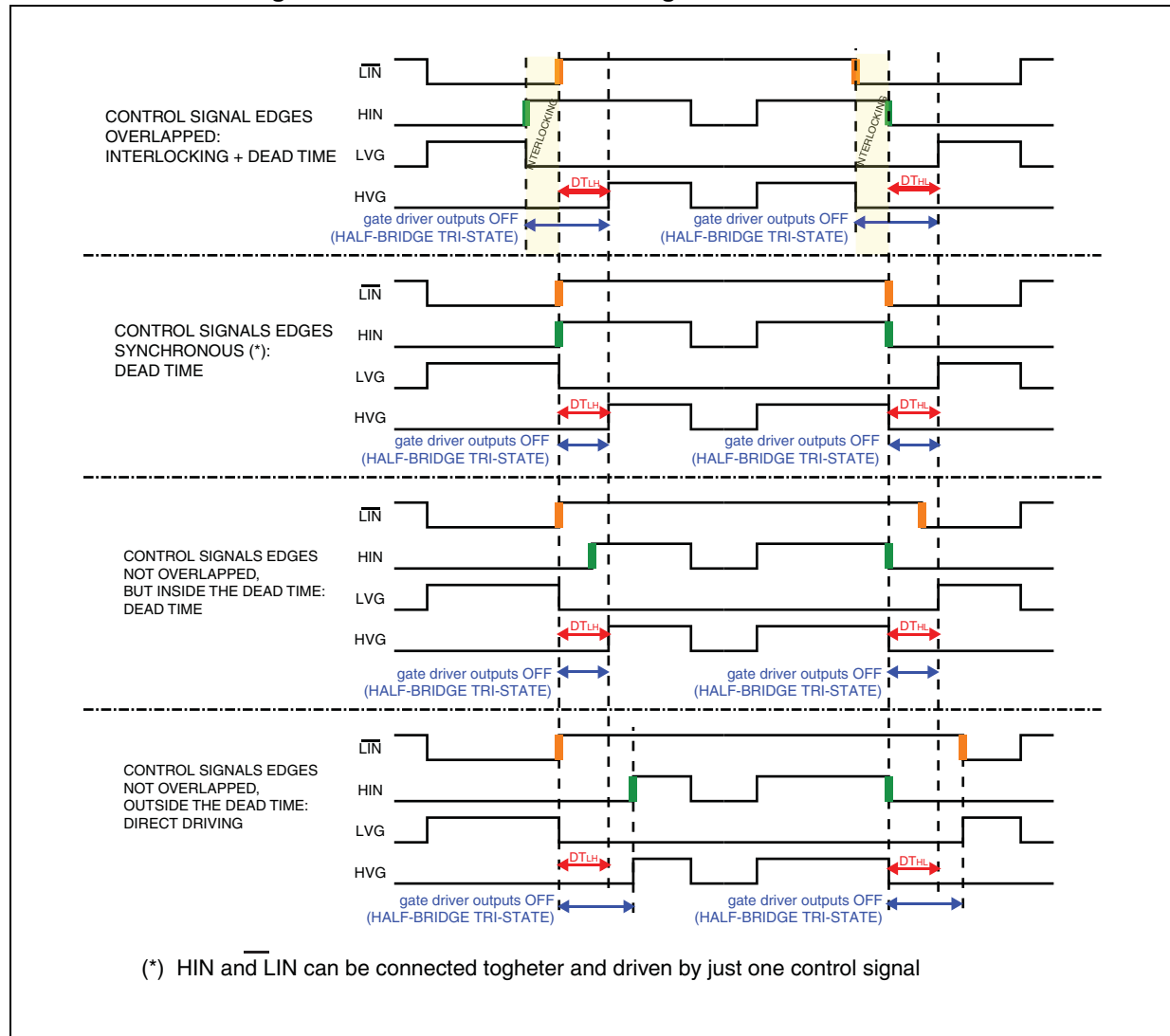
Table 9. Sense comparator characteristics⁽¹⁾ ($V_{CC} = 15\text{ V}$, $T_J = +25\text{ °C}$)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{ib}	10	Input bias current	$V_{CP+} = 1\text{ V}$			1	μA
V_{ol}	2	Open drain low level output voltage	$I_{od} = -3\text{ mA}$			0.5	V
t_{d_comp}		Comparator delay	\overline{SD}/OD pulled to 5 V through 100 k Ω resistor		90	130	ns
SR	2	Slew rate	$C_L = 180\text{ pF}$; $R_{pu} = 5\text{ k}\Omega$		60		V/ μs

1. The comparator is disabled when V_{CC} is in UVLO condition.

6 Waveforms definition

Figure 5. Deadtime and interlocking waveforms definition



7 Smart shutdown function

The L6390 device integrates a comparator committed to the fault sensing function. The comparator has an internal voltage reference V_{ref} connected to the inverting input, while the non-inverting input is available on the pin 10. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function. The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on the pin 2, shared with the SD input. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low level leaving the half-bridge in tristate.

Figure 6. Smart shutdown timing waveforms

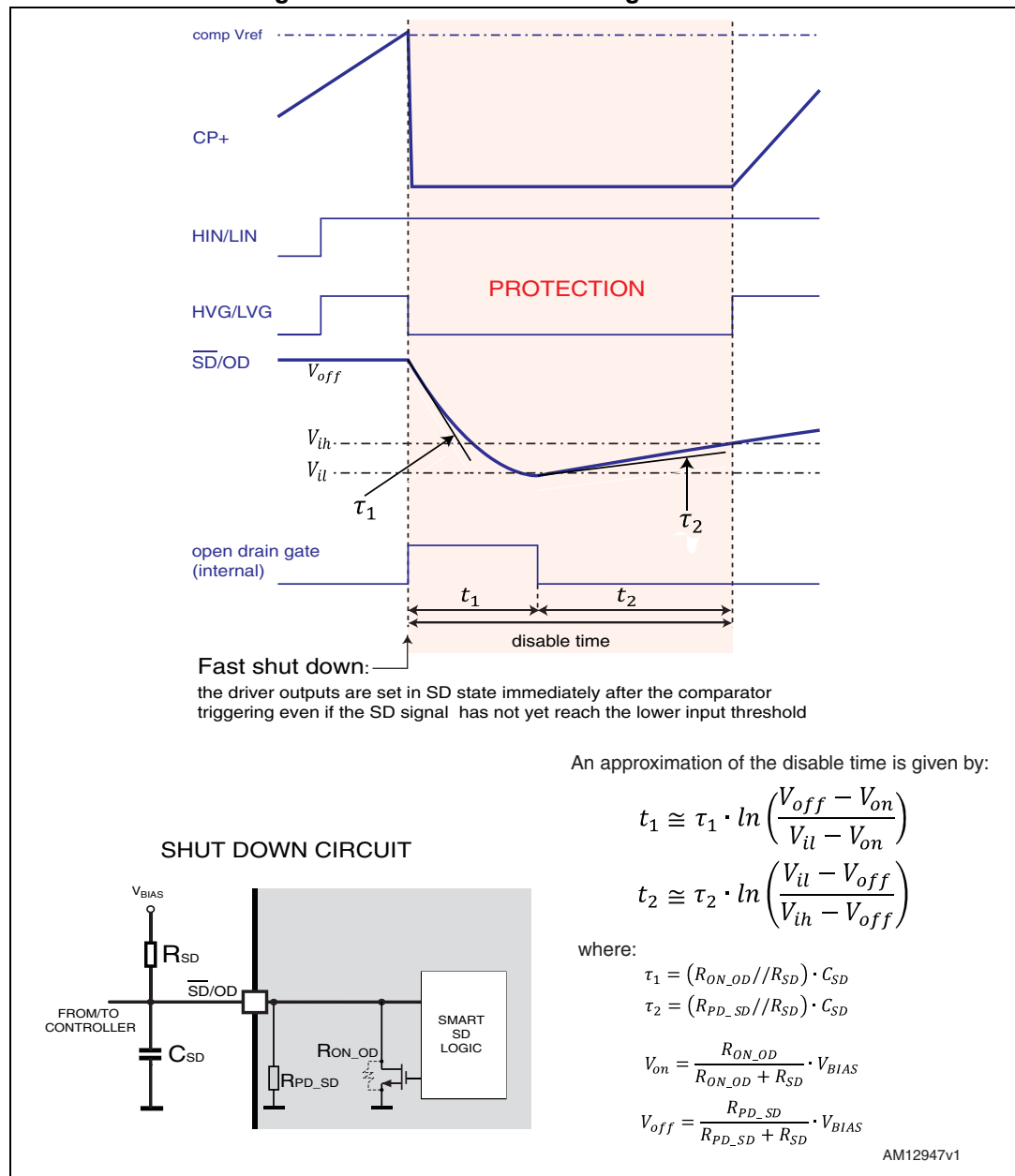
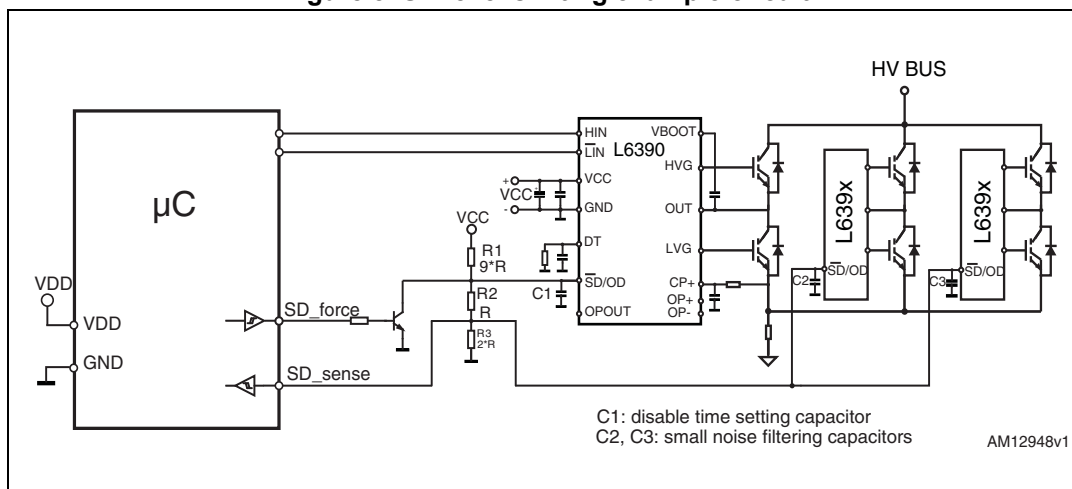
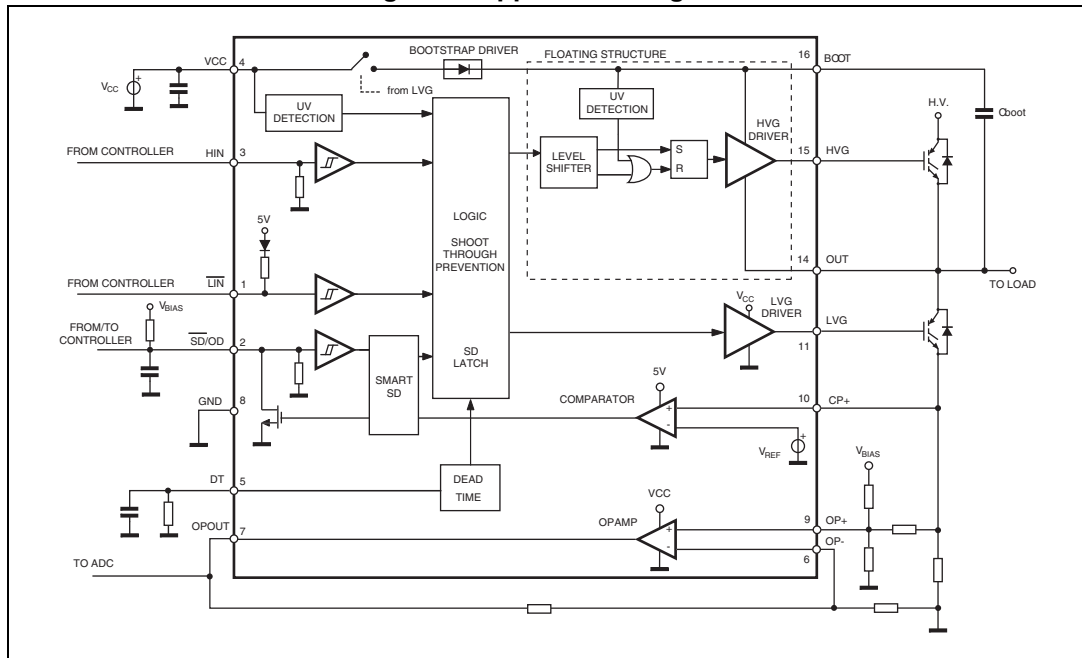


Figure 8. SD level shifting example circuit



8 Typical application diagram

Figure 9. Application diagram



9 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode ([Figure 10.a](#)). In the L6390 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in [Figure 10.b](#). An internal charge pump ([Figure 10.b](#)) provides the DMOS driving voltage.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It must be:

Equation 2

$$C_{BOOT} \gg C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG must be supplied for a long time, the C_{BOOT} selection must also take the leakage and quiescent losses into account.

E.g.: HVG steady-state consumption is lower than 240 μA, so if HVG T_{ON} is 5 ms, C_{BOOT} must supply 1.2 μC to C_{EXT}. This charge on a 1 μF capacitor means a voltage drop of 1.2 V.

The internal bootstrap driver offers important advantages: the external fast recovery diode can be avoided (it usually has a high leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and, at the same time, the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 120 Ω). This drop can be neglected at low switching frequency, but it should be taken into account when operating at high switching frequency.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{\text{drop}} = I_{\text{charge}} R_{\text{dson}} \rightarrow V_{\text{drop}} = \frac{Q_{\text{gate}}}{T_{\text{charge}}} R_{\text{dson}}$$

where Q_{gate} is the gate charge of the external power MOSFET, R_{dson} is the on-resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

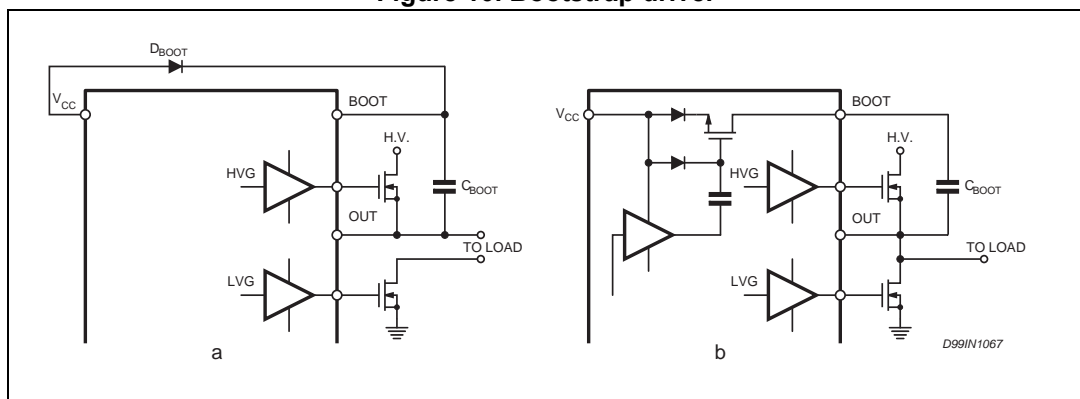
For example: using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 μs . In fact:

Equation 4

$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 120\Omega \sim 0.7\text{V}$$

V_{drop} should be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 10. Bootstrap driver



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 11. DIP-16 package outline

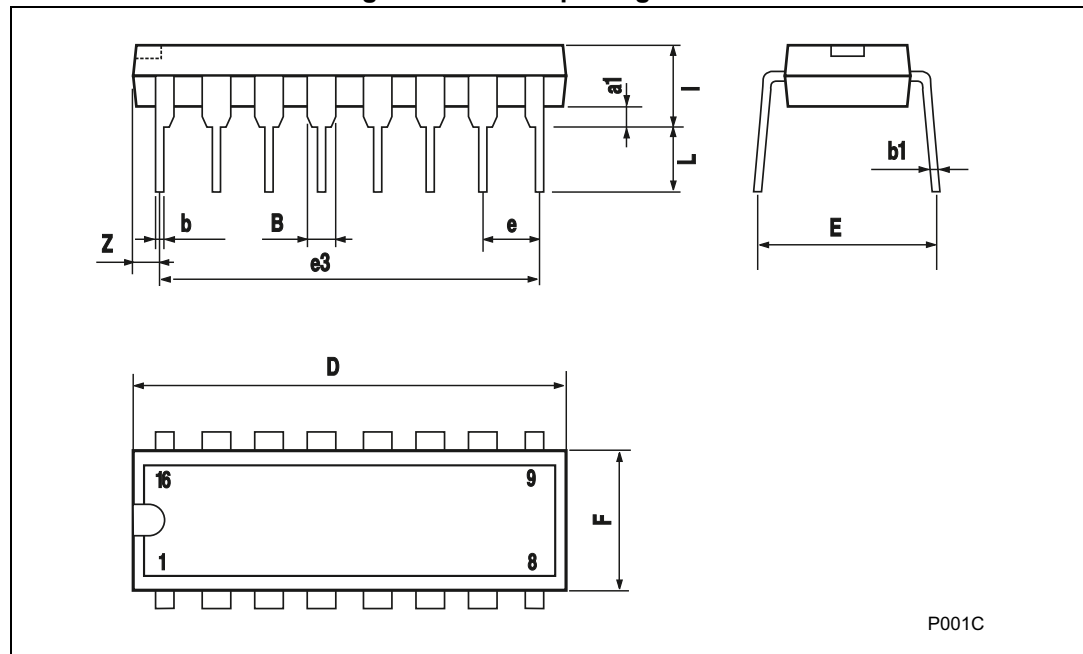


Table 10. DIP-16 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
a1	0.51		
B	0.77		1.65
b		0.5	
b1		0.25	
D			20
E		8.5	
e		2.54	
e3		17.78	
F			7.1
L		3.3	5.1
Z			1.27

Figure 12. SO-16 narrow package outline

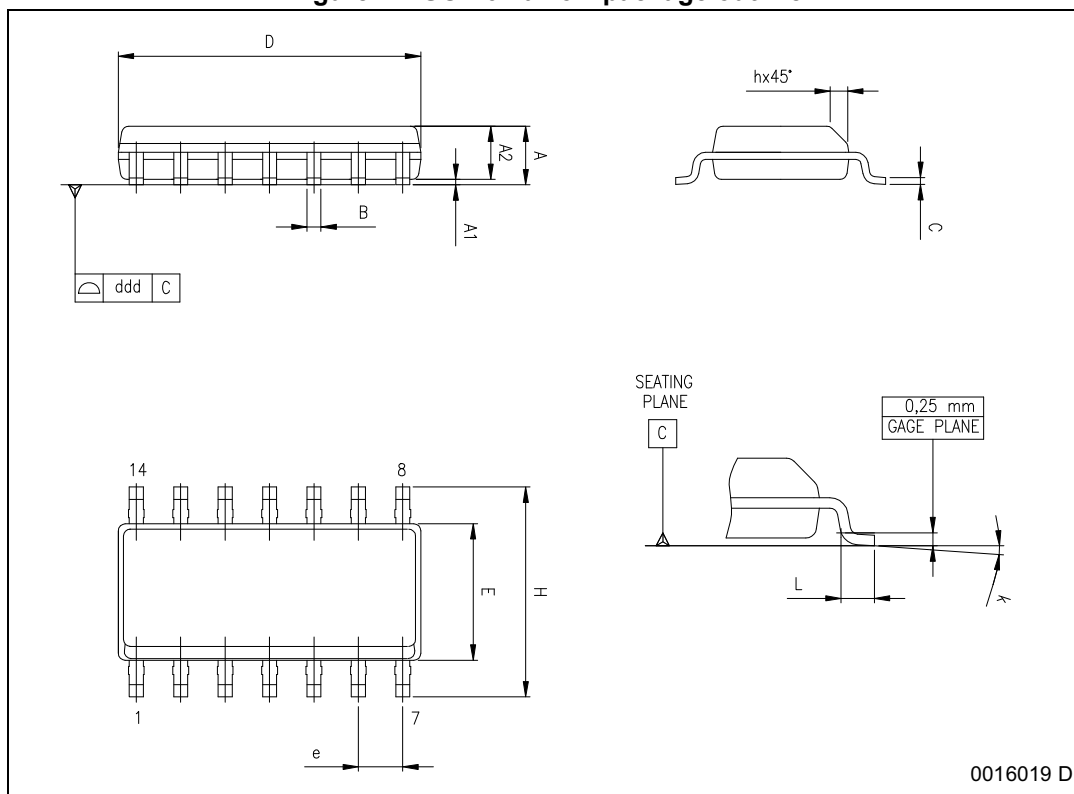
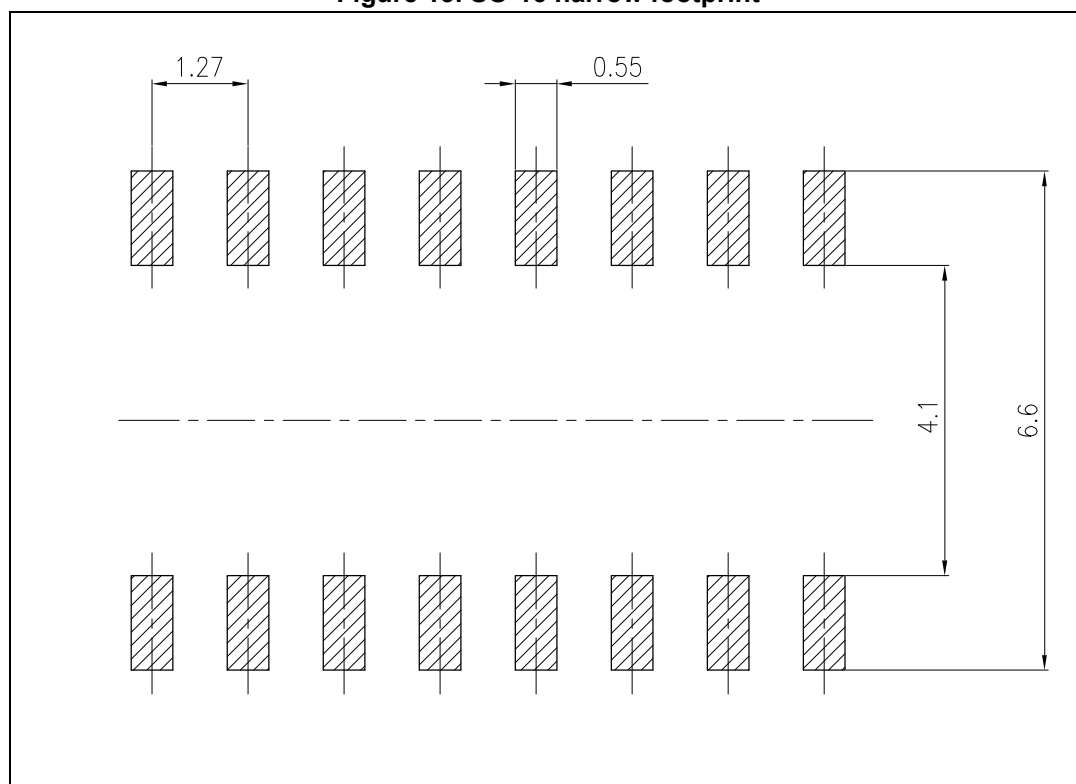


Table 11. SO-16 narrow package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8°
ccc			0.10

Figure 13. SO-16 narrow footprint



11 Order codes

Table 12. Order codes

Order code	Package	Packaging
L6390N	DIP-16	Tube
L6390D	SO-16	Tube
L6390DTR	SO-16	Tape and reel

12 Revision history

Table 13. Document revision history

Date	Revision	Changes
29-Feb-2008	1	First release
09-Jul-2008	2	Updated: Cover page, Table 1 on page 4 , Table 2 on page 5 , Section 4 on page 6 , Section 5 on page 8 , Section on page 18
17-Sep-2008	3	Updated test condition values on Table 7 and Table 8
17-Feb-2009	4	Updated Table 6 on page 8 , Table 7 on page 10 , Table 8 on page 12 Added Table 3 on page 6
11-Aug-2010	5	Updated Table 1 on page 1 , Table 6 on page 8 , Table 8 on page 12 , Table 9 on page 12
10-Jul-2012	6	Table 6 changed test conditions of DT and MDT values. Table 7 added minimum values to I_{QCCU} - I_{QCC} - I_{QBOU} - I_{QBO} . Table 7 changed V_{BO_thON} and V_{BO_thOFF} minimum and maximum values. Table 8 and Table 9 added footnote to the title of the tables. Changed HVG values on page 17. Updated SO-16 narrow mechanical data. Changed Section 7 and added Figure 7 and Figure 8 .
25-Jul-2012	7	Content reworked in Section 9: Bootstrap driver to improve readability, no technical changes.
20-Jun-2014	8	Updated Section : Applications on page 1 (replaced by new applications). Updated Section : Description on page 1 (replaced by new description). Updated Table 1: Device summary (moved from page 1 to page 24, updated title to Table 12: Order codes). Updated Section 4.1: Absolute maximum ratings on page 6 (removed note below Table 3: Absolute maximum ratings). Updated Table 7 on page 10 (updated I_{QBO} max. value). Updated Section : C_{BOOT} selection and charging on page 18 (updated values of "E.g.: HVG"). Updated Section 10: Package information on page 20 (updated titles, reversed order of Figure 11 and Table 10 , Figure 12 and Table 11 , updated headers of Table 10 and Table 11). Minor modifications throughout document.

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