November 2014

NC7SZ11
TinyLogic® UHS Three-Input AND Gate

Features

- Ultra-High Speed: t_{PD} 2.7 ns (Typical) into 50 pF at 5V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Power Down High Impedance Inputs/Outputs
- Over-Voltage Tolerance inputs facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SC70 Package

Description

The NC7SZ11 is a single three-input AND Gate from Fairchild's Ultra-High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 7 V, independent of V_{CC} operating voltage.

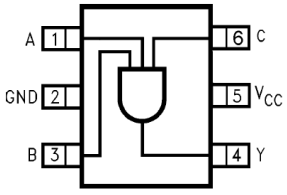
Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ11P6X	Z11	6-Lead SC70, EIAJ SC-88a, 1.25 mm Wide	3000 Units on Tape & Reel
NC7SZ11L6X	E7	6-Lead MicroPak™, 1.00 mm Wide	5000 Units on Tape & Reel

Connection Diagrams

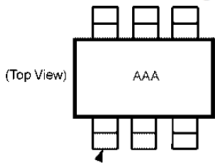
Figure 1. Logic Symbol

Pin Configurations



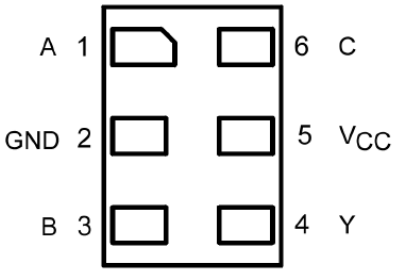
(Top View)

Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code.
Note: Orientation of Top Mark determines Pin One location. Read the Top Product Code Mark left to right, Pin One is the lower left pin (see diagram)

Figure 2. SC70 (Top View)



(Top Thru View)

Figure 3. MicroPak (Top Through View)

Pin Definitions

Pin # SC70	Pin # MicroPak	Name	Description
1	1	A	Input
2	2	GND	Ground
3	3	B	Input
4	4	Y	Output
5	5	V_{CC}	Supply Voltage
6	6	C	Input

Function Table

Y=ABC

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = HIGH Logic Level

L = LOW Logic Level

X = Either LOW or HIGH Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage		-0.5	7.0	V
V_{OUT}	DC Output Voltage		-0.5	7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < -0.5 V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < -0.5 V		-50	mA
		V_{OUT} > 6 V, V_{CC}=GND		+20	
I_{OUT}	DC Output Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C	SC70-6		150	mW
		MicroPak-6		130	
ESD	Human Body Model, JESD22-A114			4000	V
	Charged Device Model, JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8 V, 2.5 V ± 0.2 V	0	20	ns/V
		V_{CC} at 3.3 V ± 0.3 V	0	10	
		V_{CC} at 5.0 V ± 0.5 V	0	5	
θ_{JA}	Thermal Resistance	SC70-6		425	°C/W
		MicroPak-6		500	

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

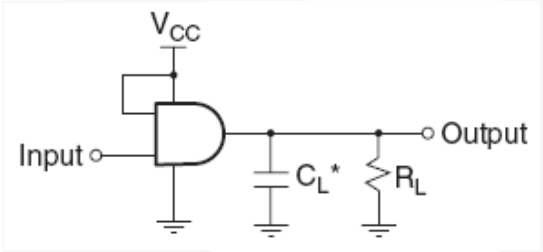
Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.8 ± 0.15		0.75 V_{CC}			0.75 V_{CC}		V
		2.30 to 5.50		0.70 V_{CC}			0.70 V_{CC}		
V_{IL}	LOW Level Input Voltage	1.8 ± 0.15				0.25 V_{CC}		0.25 V_{CC}	V
		2.30 to 5.50				0.30 V_{CC}		0.30 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN}=V_{IH}, I_{OH}=-100 µA	1.55	1.65		1.55		V
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I_{OH}=-4 mA	1.29	1.52		1.29		
		2.30	I_{OH}=-8 mA	1.90	2.15		1.90		
		3.00	I_{OH}=-16 mA	2.50	2.80		2.40		
		3.00	I_{OH}=-24 mA	2.40	2.68		2.30		
		4.50	I_{OH}=-32 mA	3.90	4.20		3.80		
V_{OL}	LOW Level Output Voltage	1.65	V_{IN}=V_{IL}, I_{OL}=100 µA		0.00	0.10		0.10	V
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I_{OL}=4 mA		0.80	0.24		0.24	
		2.30	I_{OL}=8 mA		0.10	0.30		0.30	
		3.00	I_{OL}=16 mA		0.15	0.40		0.40	
		3.00	I_{OL}=24 mA		0.22	0.55		0.55	
		4.50	I_{OL}=32 mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0 to 5.5	V_{IN}=5.5 V, GND			±1		±10	µA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT}=5.5 V			1		10	µA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN}=5.5 V, GND			2		20	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PHL}	Propagation Delay	1.80 ± 0.15	C_L=15 pF, R_L=1M Ω	2.0	9.0	18.5	2.0	19.0	ns	Figure 4 Figure 5
		2.50 ± 0.20		0.8	4.9	10.5	0.8	11.0		
		3.30 ± 0.30		0.5	3.5	8.5	0.5	9.0		
		5.00 ± 0.50		0.5	2.5	6.5	0.5	7.0		
		3.30 ± 0.30	C_L=50 pF, R_L=500 Ω	1.5	4.1	8.5	1.5	9.0		
		5.00 ± 0.50		0.8	2.9	7.5	0.8	8.0		
C_{IN}	Input Capacitance	0.00			4				pF	
C_{PD}	Power Dissipation Capacitance(2)	3.30			20				pF	Figure 6
		5.00			25					

Note:

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output lading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)$.



Notes:

3. C_L includes load and stray capacitance.
4. Input PRR=1.0 MHz; t_W500 ns.

Figure 4. AC Test Circuit

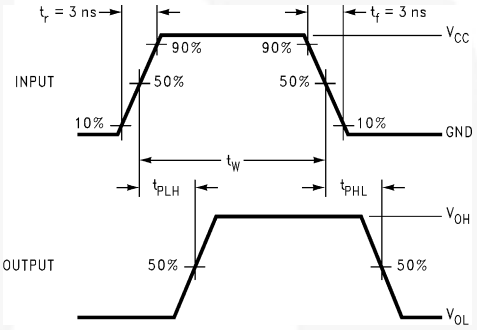
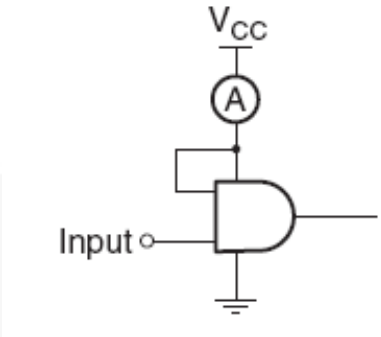


Figure 5. AC Waveforms



Note:

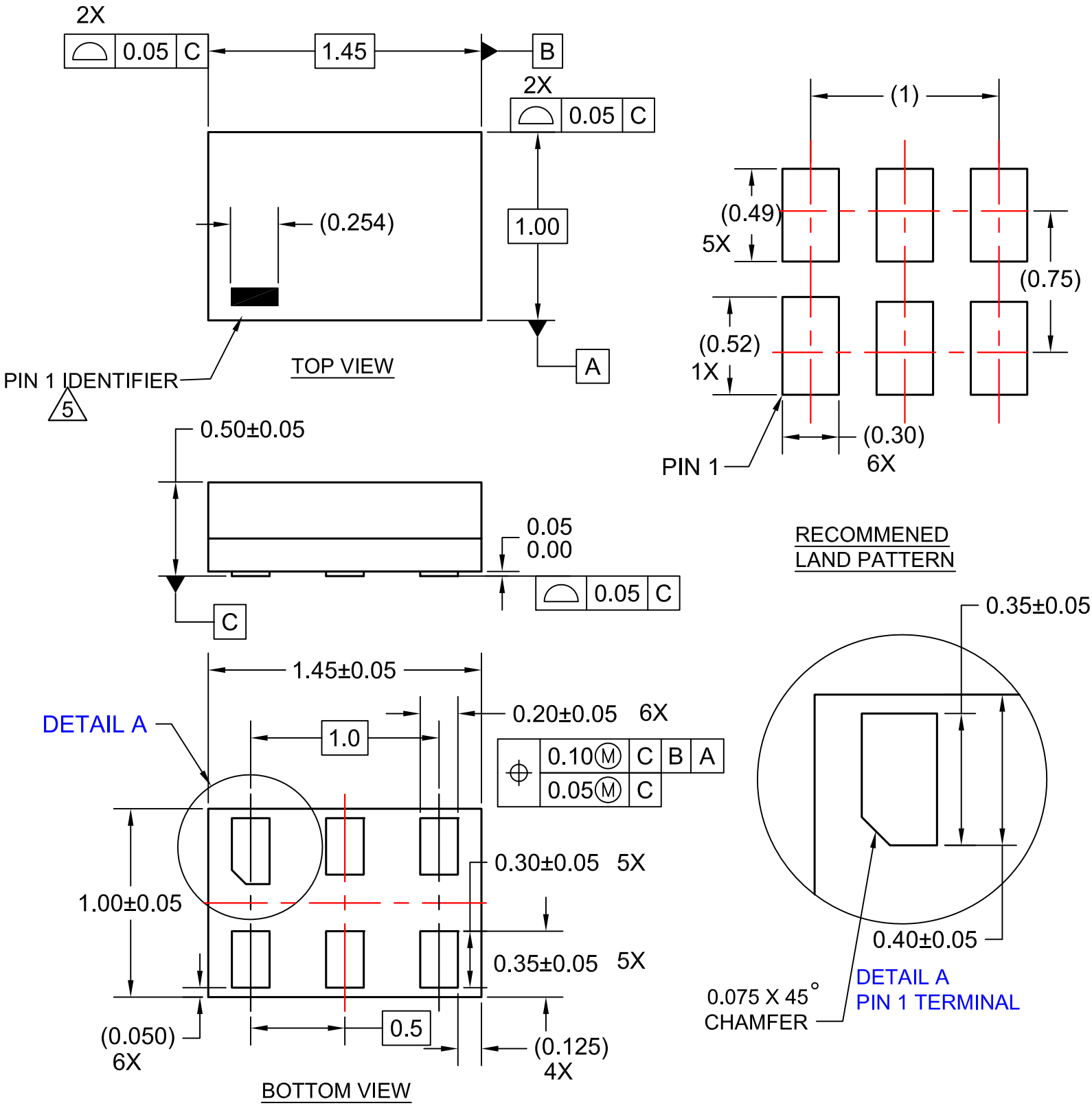
5. Input=AC Waveform; t_r=t_f=1.8 ns; PRR=10 MHz; Duty Cycle=50%.

Figure 6. I_{CCD} Test Circuit

Tape and Reel Specifications

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



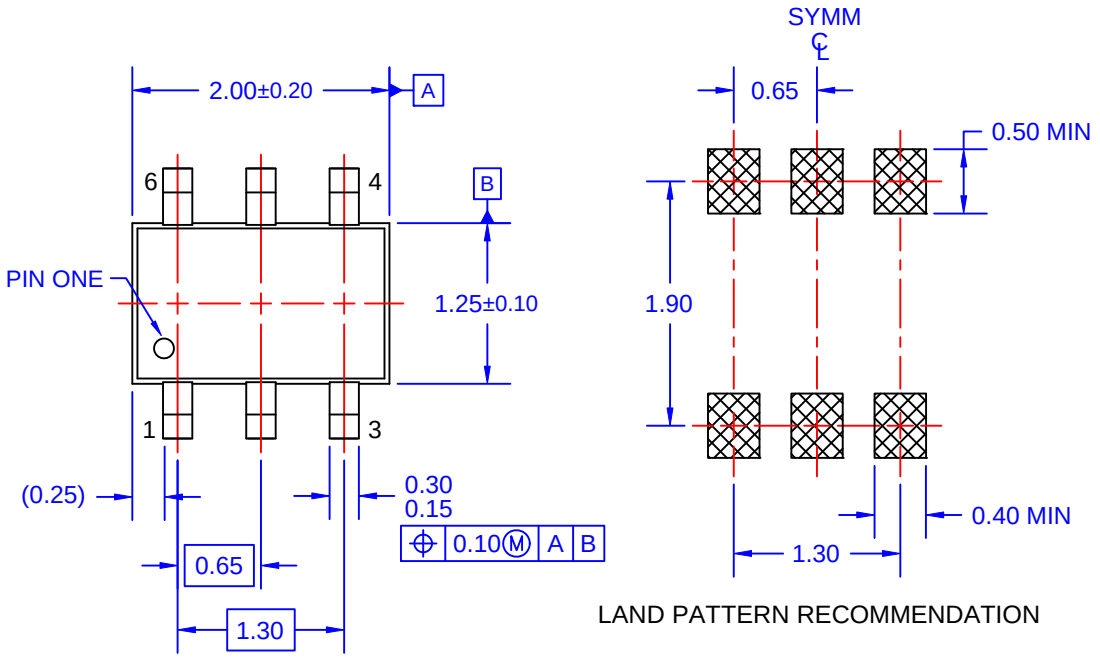
NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. LANDPATTERN RECOMMENDATION PER FSC
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.
6. FILENAME AND REVISION: MAC06AREV6

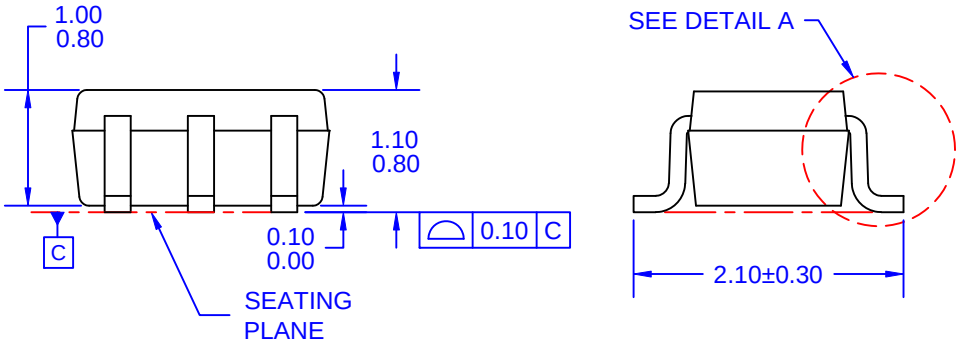
FAIRCHILD

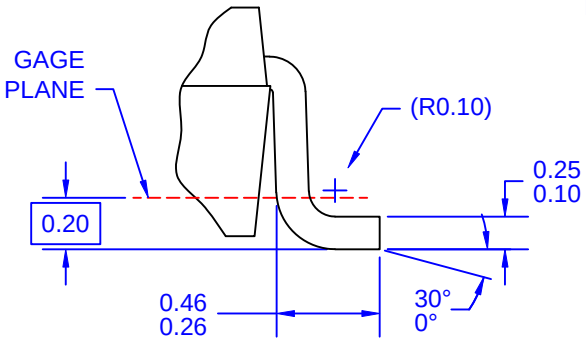
REVISIONS

LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL		
B	REVISE AS PER EIAJ	JUL.21,1998	H. ALLEN
C	FSC LAND PATTERN REC.	AUG.18,1998	H. ALLEN
D	REDRAW AS PER STD DW TEMPLATE; ADD MIN FOOT LENGHT DIM. CHG DIM STYLE FR DEVIATION TO LIMITS. REARRANGE DWG TITLE. ADD DWG NUMBER &REV. AT LOWER LEFT CORNER OF TEMPLATE.	AUG.04,1999	MAG
5	CHG LD WIDTH DIM FR $^{0.50}_{0.15}$ TO $^{0.35}_{0.15}$; LD THICK FR $^{0.25}_{0.10}$ TO $^{0.25}_{0.08}$; LD SPREAD FR 2.10±0.30 TO 2.10$^{+0.35}_{-0.30}$; FT LENGTH FR $^{0.45}_{0.30}$ TO $^{0.46}_{0.26}$; REM LD DIM (0.43)	17JAN2007	BMR
6	ADD PIN ONE INDICATOR; CHG DWG TEMPLATE & FORMAT TO STANDARD.	14JUL2009	H. ALLEN



LAND PATTERN RECOMMENDATION





DETAIL A
SCALE: 60X

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ SC-88, 1996.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
D) DRAWING FILENAME: MKT-MAA06AREV6

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	14JUL2009
CHECKED: H. ALLEN	
APPROVED: M.R. GESTOLE	
C.N. TANGPUZ	

PROJECTION
INCH
[MM]

FAIRCHILD SEMICONDUCTOR TM

6LD, SC-70,
EIAJ SC-88, 1.25MM WIDE

SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT-MAA06A	6

FORMERLY: N/A
SHEET : 1 OF 1

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I72

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Components Supply Platform

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