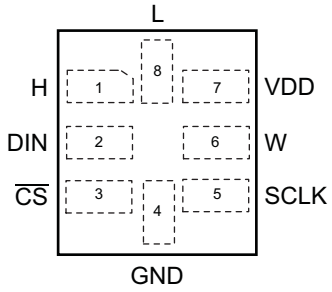
256 Taps Single Channel Digital Potentiometer With SPI Interface

Check for Samples: TPL0501

FEATURES

- **Single Channel, 256-Position Resolution**
- **100 kΩ End-to-End Resistance Options**
- **Low Temperature Coefficient: 35 ppm/°C**
- **SPI-Compatible Serial Interface**
- **2.7 V to 5.5V Single-Supply Operation**
- **±20% Resistance Tolerance**
- **Operating Temperature –40°C to 125°C**
- **ESD Performance Tested per JESD 22**
  - **2000 V Human Body Model (A114-B, Class II)**

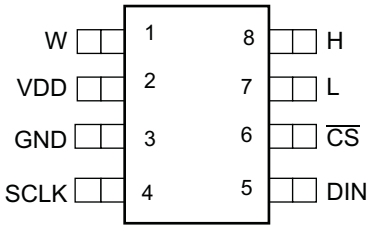
MicroQFN – RSE PACKAGE
(TOP VIEW)



APPLICATIONS

- **Adjustable Power Supplies**
- **Adjustable Gain Amplifiers and Offset Trimming**
- **Precision Calibration of Set Point Thresholds**
- **Sensor Trimming and Calibration**
- **Mechanical Potentiometer Replacement**

SOT-23 – DCN PACKAGE
(TOP VIEW)



DESCRIPTION

The TPL0501 is a single channel, linear-taper digital potentiometer with 256 wiper positions. This device can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0501 is currently offered with end-to-end resistance of 100kΩ.

The internal registers of the TPL0501 can be accessed using a SPI-compatible interface. The TPL0501 has a nominal temperature coefficient of 35ppm/°C.

The TPL0501 is available in an 8-pin SOT-23 and 8-microQFN package with a specified temperature range of –40°C to 85°C.

ORDERING INFORMATION

TA	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	microQFN-RSE	Tape and Reel	TPL0501-100RSER	7M
	SOT23 – DCN		TPL0501-100DCNR	NF5T

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

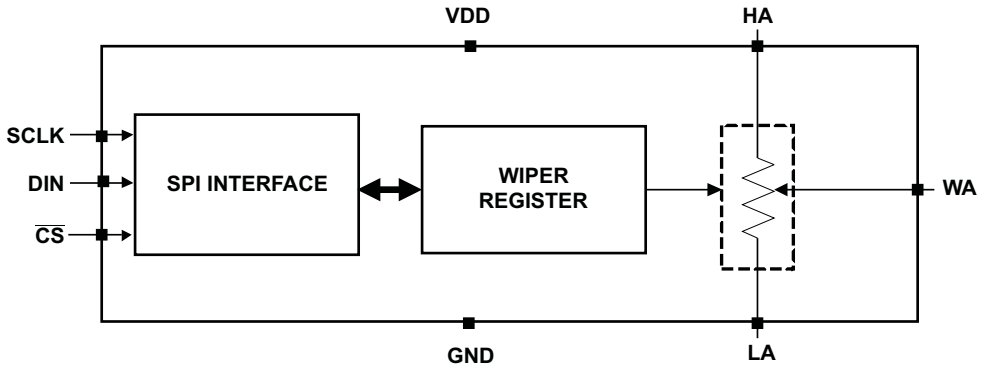
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011, Texas Instruments Incorporated

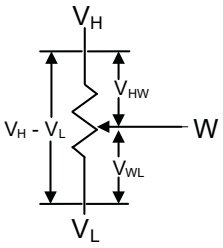
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



DIGITAL POTENTIOMETER CONFIGURATIONS

VOLTAGE DIVIDER MODE

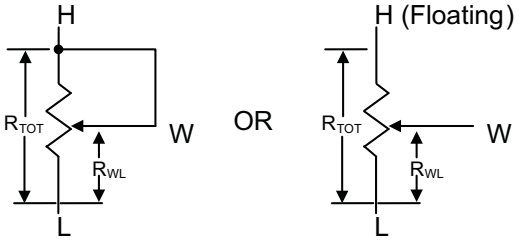


$V_{HW} = (V_H – V_L) \times (1 – (D/256))$

$V_{WL} = (V_H – V_L) \times D/256$

Where D = Decimal Value of Wiper Code

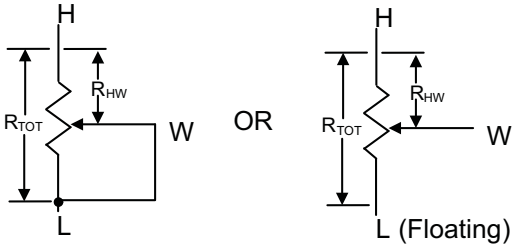
RHEOSTAT MODE A



$R_{WL} = R_{TOT} \times D/256$

Where D = Decimal Value of Wiper Code

RHEOSTAT MODE B



$R_{HW} = R_{TOT} \times (1 – (D/256))$

Where D = Decimal Value of Wiper Code

Figure 1. DPOT Configurations

Copyright © 2011, Texas Instruments Incorporated

PIN FUNCTIONS

PIN		NAME	TYPE	DESCRIPTION
NUMBER				
DCN	RSE			
1	6	W	I/O	Wiper terminal
2	7	V_{DD}	Power	Positive Supply Voltage
3	4	GND	Ground	Ground
4	5	SCLK	Input	SPI Clock
5	2	DIN	Input	SPI Input
6	3	$\overline{CS}$	Input	SPI Chip Select. Active Low
7	8	L	I/O	Low terminal
8	1	H	I/O	High terminal

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD} to GND	Supply voltage range		–0.3	7	V
V_H, V_L, V_W			–0.3	V_{DD}+0.3	V
I_H I_L I_W	Pulse current			±20	mA
	Continuous current	TPL0501-100		±5	mA
V_I	Digital input voltage range		–0.3	7	V
θ_{JA}	Package thermal impedance(4)	RSE package			°C/W
		DCN package			
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

ANALOG SPECIFICATIONS

Typical Values are specified at VDD=5V and operating temperature of 25 C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
R_{TOTAL}	End-to-end resistance (between Hi and Li terminals)		80	100	120	kΩ
V_H, V_L	Terminal voltage range		0		VDD	V
R_H, R_L	Terminal resistance			50	150	Ω
R_W	Wiper resistance	H terminal floating, V_L = GND, Force I_W = (V_{DD}/2)/R_{TOTAL}, Input code = 0x80h		25	100	Ω
C_H, C_L	Terminal capacitance	f = 1 MHz, measured to GND, Input code = 0x80h		15		pF
C_W	Wiper capacitance			12		
I_{LKG}	Terminal leakage current	V_H = GND to V_{DD}, V_L = Floating OR V_L = GND to V_{DD}, V_H = Floating		0.1	1	uA
TC_R	Resistance temperature coefficient			35		ppm/°C
VOLTAGE DIVIDER MODE (V_H = V_{DD}, V_L = GND, V_W = Not Loaded)						
INL	Integral non-linearity		–1		1	LSB
DNL	Differential non-linearity		–0.5		0.5	LSB
ZS_{ERROR}	Zero-scale error		0	0.5	2	LSB
FS_{ERROR}	Full-scale error		–2	–0.5	0	LSB

Copyright © 2011, Texas Instruments Incorporated

ANALOG SPECIFICATIONS (continued)

Typical Values are specified at VDD=5V and operating temperature of 25 C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
T_{CV}	Ratiometric temperature coefficient	Wiper set at mid-scale		4		ppm/°C
BW	Bandwidth	Wiper set at mid-scale, TPL0501-100, C_{LOAD}=10pF		265		kHz
T_{SW}	Wiper settling time	TPL0501-100		3		µS
THD	Total harmonic distortion	$V_H = 1V_{RMS}$ at 1kHz, $V_L = V_{DD}/2$, measurement at W		0.005		%
RHEOSTAT MODE (Measurements between Wi and Li with Hi not connected, or between Wi and Hi with Li not connected)						
RINL	Integral non-linearity		–1		1	LSB
RDNL	Differential non-linearity		–0.5		0.5	LSB
R_{OFFSET}	Offset		0	0.5	2	LSB
RBW	Bandwidth	Code=0x00h, L Floating, Input applied to W, 10 pF on H		60		kHz

OPERATING SPECIFICATIONS

Typical Values are specified at VDD=5V and operating temperature of 25 C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(STBY)}$	V_{DD} Standby current			0.3	8	µA
I_{IN-DIG}	Digital pins leakage current (SCLK, DIN, $\overline{CS}$ inputs)		–1		1	µA
$I_{DD(SUPPLY)}$	V_{DD} Supply Current	Digital Input= 1.8V, VDD=2.7V		5		µA
		Digital Input= 1.8V, VDD=5V		500		µA
SERIAL INTERFACE SPECS (SCLK, DIN, $\overline{CS}$ Inputs)						
V_{IH}	Input high voltage	V_{DD} = 2.7 V to 5.5 V	1.8		5.5	V
V_{IL}	Input low voltage	SCLK, DIN, $\overline{CS}$ Inputs	0		0.6	V
C_{IN}	Pin capacitance	SCLK, DIN, $\overline{CS}$ Inputs		7	10	pF
SPI INTERFACE TIMING CHARACTERISTICS						
f_{SCLK}	SCLK Frequency				25	MHz
t_{SCP}	SCLK Period		40			ns
t_{SCH}	SCLK High time		20			ns
t_{SCL}	SCLK Low time		20			ns
t_{DS}	DIN to SCLK setup time		5			ns
t_{DH}	DIN hold after SCLK		5			ns
t_{CSS}	$\overline{CS}$ Fall to SCLK rise setup time		15			ns
t_{CSW}	$\overline{CS}$ Pulse width high		40			ns

Copyright © 2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

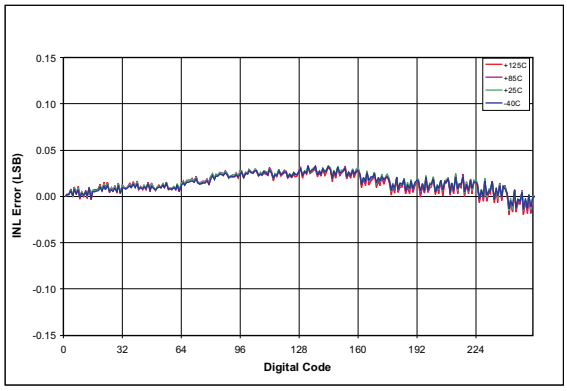


Figure 2. INL vs TAP POSITION (Potentiometer Mode)

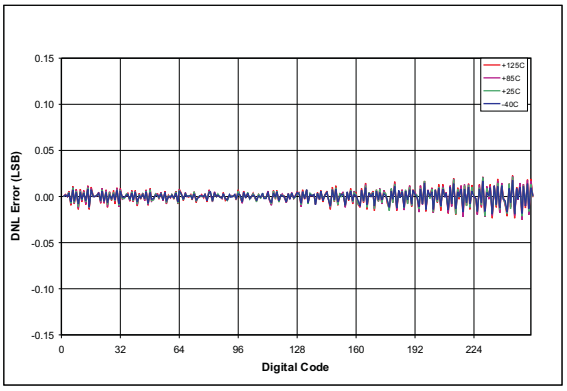


Figure 3. DNL vs TAP POSITION (Potentiometer Mode)

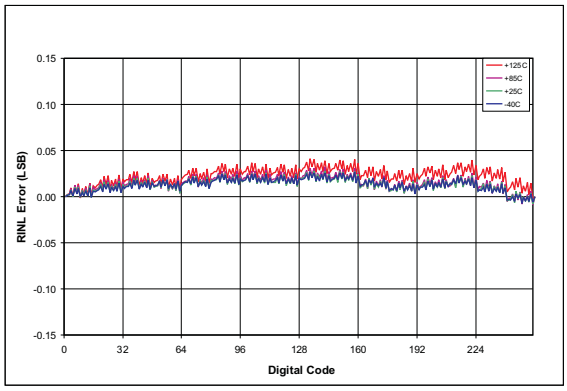


Figure 4. INL vs TAP POSITION (Rheostat Mode)

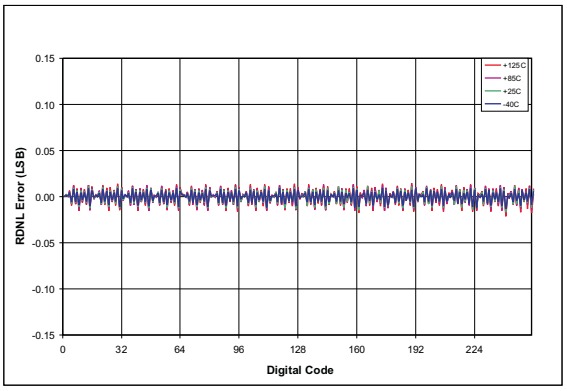


Figure 5. DNL vs. TAP POSITION (Rheostat Mode)

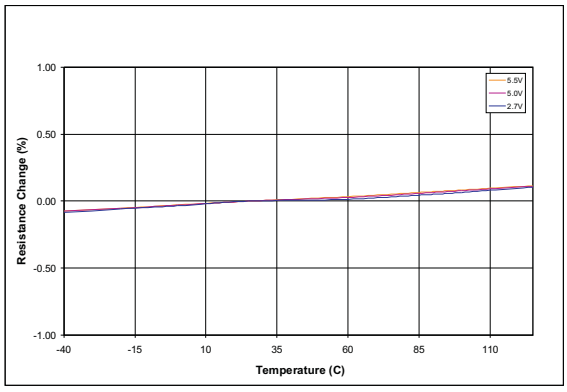


Figure 6. End to End resistance change vs Temperature

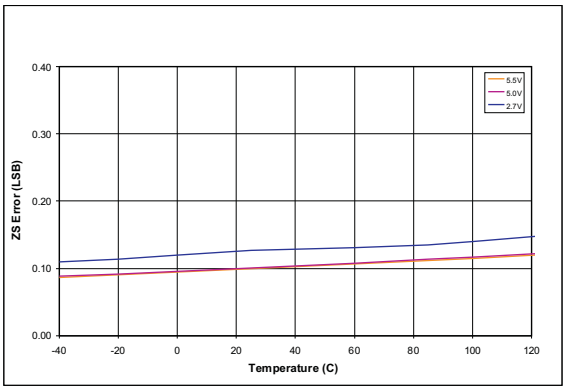


Figure 7. Zero Scale Error vs Temperature

Copyright © 2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

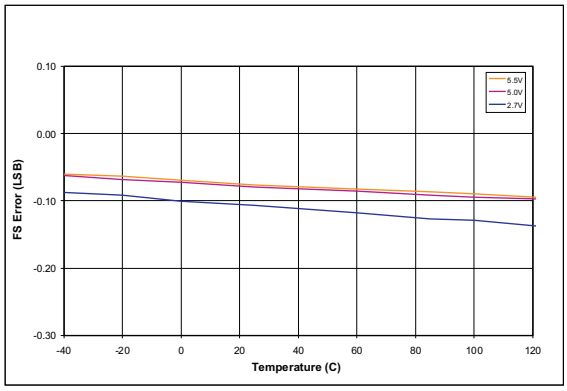


Figure 8. Full scale Error vs Temperature

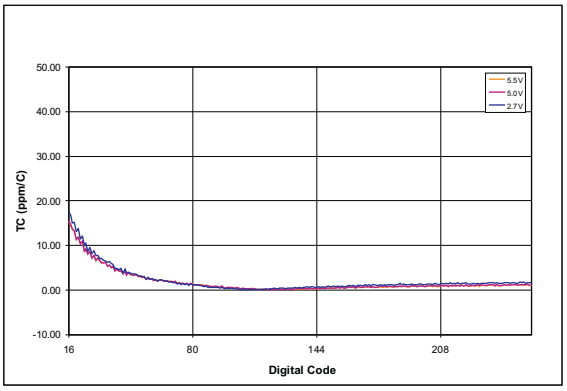


Figure 9. Temperature Coefficient vs Tap Position (Potentiometer Mode)

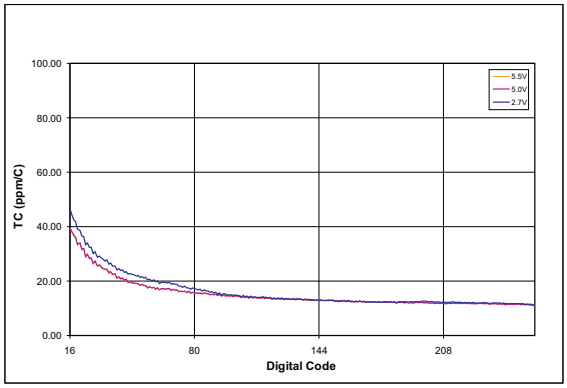


Figure 10. Temperature Coefficient vs Tap Position (Rheostat Mode)

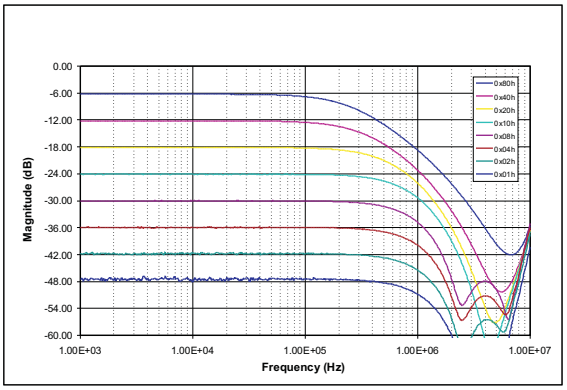


Figure 11. Bandwidth (potentiometer mode)

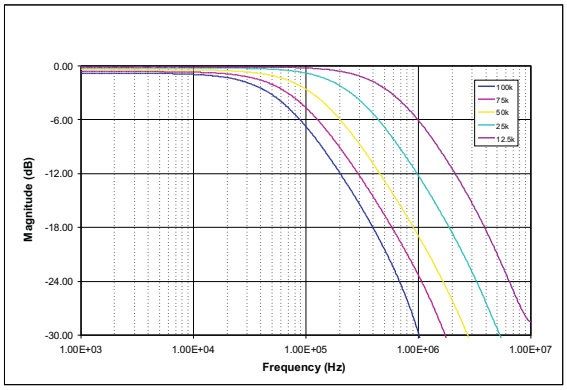


Figure 12. Bandwidth (Rheostat mode)

Copyright © 2011, Texas Instruments Incorporated

APPLICATION INFORMATION

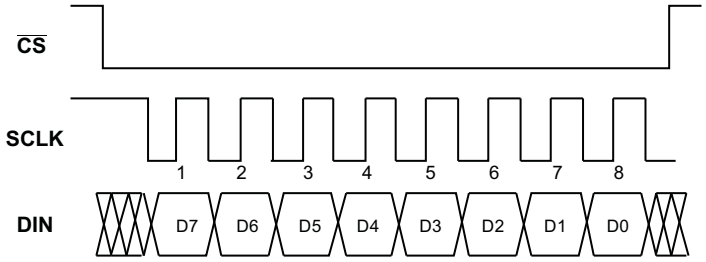
SPI Digital Interface

The TPL0501 uses a 3-wire SPI compatible serial data interface. This write-only interface has three inputs: chip-select ($\overline{CS}$), data clock (SCLK), and data input (DIN). Drive $\overline{CS}$ low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge. After loading data into the shift register, drive $\overline{CS}$ high to latch the data into the appropriate potentiometer control register and disable the serial interface. Keep $\overline{CS}$ low during the entire serial data stream to avoid corruption of the data.

Register Map:

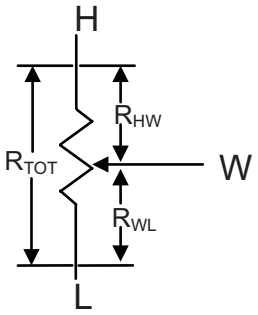
Bit	7	6	5	4	3	2	1	0
	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0

SPI WRITE SEQUENCE



Copyright © 2011, Texas Instruments Incorporated

IDEAL RESISTANCE VALUES



$R_{WL} = R_{TOT} \times D/256$

$R_{HW} = R_{TOT} \times (1 - (D/256))$

Where D = Decimal Value of Wiper Code

Below table shows the ideal values for DPOT with end-to End resistance of 10kΩ. The absolute values of resistance can vary significantly but the Ratio (Rhw/Rwl) is extremely accurate.

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
0	0	0.00	100.00	0.00
1	1	0.39	99.61	0.00
2	10	0.78	99.22	0.01
3	11	1.17	98.83	0.01
4	100	1.56	98.44	0.02
5	101	1.95	98.05	0.02
6	110	2.34	97.66	0.02
7	111	2.73	97.27	0.03
8	1000	3.13	96.88	0.03
9	1001	3.52	96.48	0.04
10	1010	3.91	96.09	0.04
11	1011	4.30	95.70	0.04
12	1100	4.69	95.31	0.05
13	1101	5.08	94.92	0.05
14	1110	5.47	94.53	0.06
15	1111	5.86	94.14	0.06
16	10000	6.25	93.75	0.07
17	10001	6.64	93.36	0.07
18	10010	7.03	92.97	0.08
19	10011	7.42	92.58	0.08
20	10100	7.81	92.19	0.08
21	10101	8.20	91.80	0.09
22	10110	8.59	91.41	0.09
23	10111	8.98	91.02	0.10
24	11000	9.38	90.63	0.10
25	11001	9.77	90.23	0.11
26	11010	10.16	89.84	0.11
27	11011	10.55	89.45	0.12
28	11100	10.94	89.06	0.12
29	11101	11.33	88.67	0.13
30	11110	11.72	88.28	0.13
31	11111	12.11	87.89	0.14
32	100000	12.50	87.50	0.14

Copyright © 2011, Texas Instruments Incorporated

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
33	100001	12.89	87.11	0.15
34	100010	13.28	86.72	0.15
35	100011	13.67	86.33	0.16
36	100100	14.06	85.94	0.16
37	100101	14.45	85.55	0.17
38	100110	14.84	85.16	0.17
39	100111	15.23	84.77	0.18
40	101000	15.63	84.38	0.19
41	101001	16.02	83.98	0.19
42	101010	16.41	83.59	0.20
43	101011	16.80	83.20	0.20
44	101100	17.19	82.81	0.21
45	101101	17.58	82.42	0.21
46	101110	17.97	82.03	0.22
47	101111	18.36	81.64	0.22
48	110000	18.75	81.25	0.23
49	110001	19.14	80.86	0.24
50	110010	19.53	80.47	0.24
51	110011	19.92	80.08	0.25
52	110100	20.31	79.69	0.25
53	110101	20.70	79.30	0.26
54	110110	21.09	78.91	0.27
55	110111	21.48	78.52	0.27
56	111000	21.88	78.13	0.28
57	111001	22.27	77.73	0.29
58	111010	22.66	77.34	0.29
59	111011	23.05	76.95	0.30
60	111100	23.44	76.56	0.31
61	111101	23.83	76.17	0.31
62	111110	24.22	75.78	0.32
63	111111	24.61	75.39	0.33
64	1000000	25.00	75.00	0.33
65	1000001	25.39	74.61	0.34
66	1000010	25.78	74.22	0.35
67	1000011	26.17	73.83	0.35
68	1000100	26.56	73.44	0.36
69	1000101	26.95	73.05	0.37
70	1000110	27.34	72.66	0.38
71	1000111	27.73	72.27	0.38
72	1001000	28.13	71.88	0.39
73	1001001	28.52	71.48	0.40
74	1001010	28.91	71.09	0.41
75	1001011	29.30	70.70	0.41
76	1001100	29.69	70.31	0.42
77	1001101	30.08	69.92	0.43
78	1001110	30.47	69.53	0.44
79	1001111	30.86	69.14	0.45
80	1010000	31.25	68.75	0.45

Copyright © 2011, Texas Instruments Incorporated

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
81	1010001	31.64	68.36	0.46
82	1010010	32.03	67.97	0.47
83	1010011	32.42	67.58	0.48
84	1010100	32.81	67.19	0.49
85	1010101	33.20	66.80	0.50
86	1010110	33.59	66.41	0.51
87	1010111	33.98	66.02	0.51
88	1011000	34.38	65.63	0.52
89	1011001	34.77	65.23	0.53
90	1011010	35.16	64.84	0.54
91	1011011	35.55	64.45	0.55
92	1011100	35.94	64.06	0.56
93	1011101	36.33	63.67	0.57
94	1011110	36.72	63.28	0.58
95	1011111	37.11	62.89	0.59
96	1100000	37.50	62.50	0.60
97	1100001	37.89	62.11	0.61
98	1100010	38.28	61.72	0.62
99	1100011	38.67	61.33	0.63
100	1100100	39.06	60.94	0.64
101	1100101	39.45	60.55	0.65
102	1100110	39.84	60.16	0.66
103	1100111	40.23	59.77	0.67
104	1101000	40.63	59.38	0.68
105	1101001	41.02	58.98	0.70
106	1101010	41.41	58.59	0.71
107	1101011	41.80	58.20	0.72
108	1101100	42.19	57.81	0.73
109	1101101	42.58	57.42	0.74
110	1101110	42.97	57.03	0.75
111	1101111	43.36	56.64	0.77
112	1110000	43.75	56.25	0.78
113	1110001	44.14	55.86	0.79
114	1110010	44.53	55.47	0.80
115	1110011	44.92	55.08	0.82
116	1110100	45.31	54.69	0.83
117	1110101	45.70	54.30	0.84
118	1110110	46.09	53.91	0.86
119	1110111	46.48	53.52	0.87
120	1111000	46.88	53.13	0.88
121	1111001	47.27	52.73	0.90
122	1111010	47.66	52.34	0.91
123	1111011	48.05	51.95	0.92
124	1111100	48.44	51.56	0.94
125	1111101	48.83	51.17	0.95
126	1111110	49.22	50.78	0.97
127	1111111	49.61	50.39	0.98
128	10000000	50.00	50.00	1.00

Copyright © 2011, Texas Instruments Incorporated

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
129	10000001	50.39	49.61	1.02
130	10000010	50.78	49.22	1.03
131	10000011	51.17	48.83	1.05
132	10000100	51.56	48.44	1.06
133	10000101	51.95	48.05	1.08
134	10000110	52.34	47.66	1.10
135	10000111	52.73	47.27	1.12
136	10001000	53.13	46.88	1.13
137	10001001	53.52	46.48	1.15
138	10001010	53.91	46.09	1.17
139	10001011	54.30	45.70	1.19
140	10001100	54.69	45.31	1.21
141	10001101	55.08	44.92	1.23
142	10001110	55.47	44.53	1.25
143	10001111	55.86	44.14	1.27
144	10010000	56.25	43.75	1.29
145	10010001	56.64	43.36	1.31
146	10010010	57.03	42.97	1.33
147	10010011	57.42	42.58	1.35
148	10010100	57.81	42.19	1.37
149	10010101	58.20	41.80	1.39
150	10010110	58.59	41.41	1.42
151	10010111	58.98	41.02	1.44
152	10011000	59.38	40.63	1.46
153	10011001	59.77	40.23	1.49
154	10011010	60.16	39.84	1.51
155	10011011	60.55	39.45	1.53
156	10011100	60.94	39.06	1.56
157	10011101	61.33	38.67	1.59
158	10011110	61.72	38.28	1.61
159	10011111	62.11	37.89	1.64
160	10100000	62.50	37.50	1.67
161	10100001	62.89	37.11	1.69
162	10100010	63.28	36.72	1.72
163	10100011	63.67	36.33	1.75
164	10100100	64.06	35.94	1.78
165	10100101	64.45	35.55	1.81
166	10100110	64.84	35.16	1.84
167	10100111	65.23	34.77	1.88
168	10101000	65.63	34.38	1.91
169	10101001	66.02	33.98	1.94
170	10101010	66.41	33.59	1.98
171	10101011	66.80	33.20	2.01
172	10101100	67.19	32.81	2.05
173	10101101	67.58	32.42	2.08
174	10101110	67.97	32.03	2.12
175	10101111	68.36	31.64	2.16
176	10110000	68.75	31.25	2.20

Copyright © 2011, Texas Instruments Incorporated

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
177	10110001	69.14	30.86	2.24
178	10110010	69.53	30.47	2.28
179	10110011	69.92	30.08	2.32
180	10110100	70.31	29.69	2.37
181	10110101	70.70	29.30	2.41
182	10110110	71.09	28.91	2.46
183	10110111	71.48	28.52	2.51
184	10111000	71.88	28.13	2.56
185	10111001	72.27	27.73	2.61
186	10111010	72.66	27.34	2.66
187	10111011	73.05	26.95	2.71
188	10111100	73.44	26.56	2.76
189	10111101	73.83	26.17	2.82
190	10111110	74.22	25.78	2.88
191	10111111	74.61	25.39	2.94
192	11000000	75.00	25.00	3.00
193	11000001	75.39	24.61	3.06
194	11000010	75.78	24.22	3.13
195	11000011	76.17	23.83	3.20
196	11000100	76.56	23.44	3.27
197	11000101	76.95	23.05	3.34
198	11000110	77.34	22.66	3.41
199	11000111	77.73	22.27	3.49
200	11001000	78.13	21.88	3.57
201	11001001	78.52	21.48	3.65
202	11001010	78.91	21.09	3.74
203	11001011	79.30	20.70	3.83
204	11001100	79.69	20.31	3.92
205	11001101	80.08	19.92	4.02
206	11001110	80.47	19.53	4.12
207	11001111	80.86	19.14	4.22
208	11010000	81.25	18.75	4.33
209	11010001	81.64	18.36	4.45
210	11010010	82.03	17.97	4.57
211	11010011	82.42	17.58	4.69
212	11010100	82.81	17.19	4.82
213	11010101	83.20	16.80	4.95
214	11010110	83.59	16.41	5.10
215	11010111	83.98	16.02	5.24
216	11011000	84.38	15.63	5.40
217	11011001	84.77	15.23	5.56
218	11011010	85.16	14.84	5.74
219	11011011	85.55	14.45	5.92
220	11011100	85.94	14.06	6.11
221	11011101	86.33	13.67	6.31
222	11011110	86.72	13.28	6.53
223	11011111	87.11	12.89	6.76
224	11100000	87.50	12.50	7.00

Copyright © 2011, Texas Instruments Incorporated

Step	Binary	10 kΩ		R_{HW}/R_{WL}
		R_{HW} (kΩ)	R_{WL} (kΩ)	
225	11100001	87.89	12.11	7.26
226	11100010	88.28	11.72	7.53
227	11100011	88.67	11.33	7.83
228	11100100	89.06	10.94	8.14
229	11100101	89.45	10.55	8.48
230	11100110	89.84	10.16	8.85
231	11100111	90.23	9.77	9.24
232	11101000	90.63	9.38	9.67
233	11101001	91.02	8.98	10.13
234	11101010	91.41	8.59	10.64
235	11101011	91.80	8.20	11.19
236	11101100	92.19	7.81	11.80
237	11101101	92.58	7.42	12.47
238	11101110	92.97	7.03	13.22
239	11101111	93.36	6.64	14.06
240	11110000	93.75	6.25	15.00
241	11110001	94.14	5.86	16.07
242	11110010	94.53	5.47	17.29
243	11110011	94.92	5.08	18.69
244	11110100	95.31	4.69	20.33
245	11110101	95.70	4.30	22.27
246	11110110	96.09	3.91	24.60
247	11110111	96.48	3.52	27.44
248	11111000	96.88	3.13	31.00
249	11111001	97.27	2.73	35.57
250	11111010	97.66	2.34	41.67
251	11111011	98.05	1.95	50.20
252	11111100	98.44	1.56	63.00
253	11111101	98.83	1.17	84.33
254	11111110	99.22	0.78	127.00
255	11111111	99.61	0.39	255.00

Copyright © 2011, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL0501-100DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(NF5J ~ NF5T)	Samples
TPL0501-100RSER	ACTIVE	UQFN	RSE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

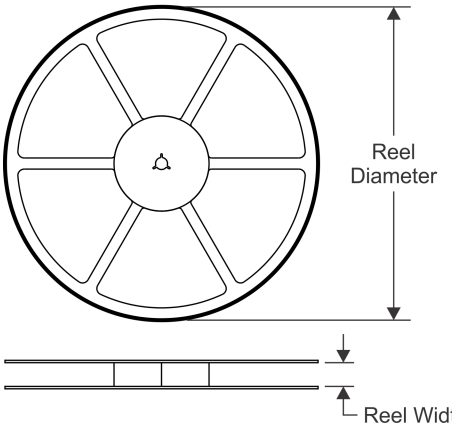
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

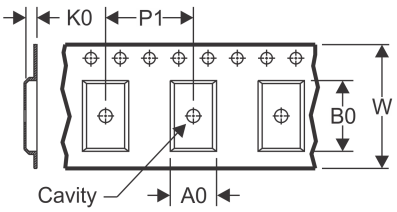
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

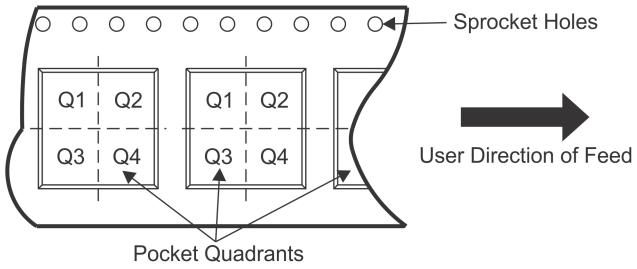


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

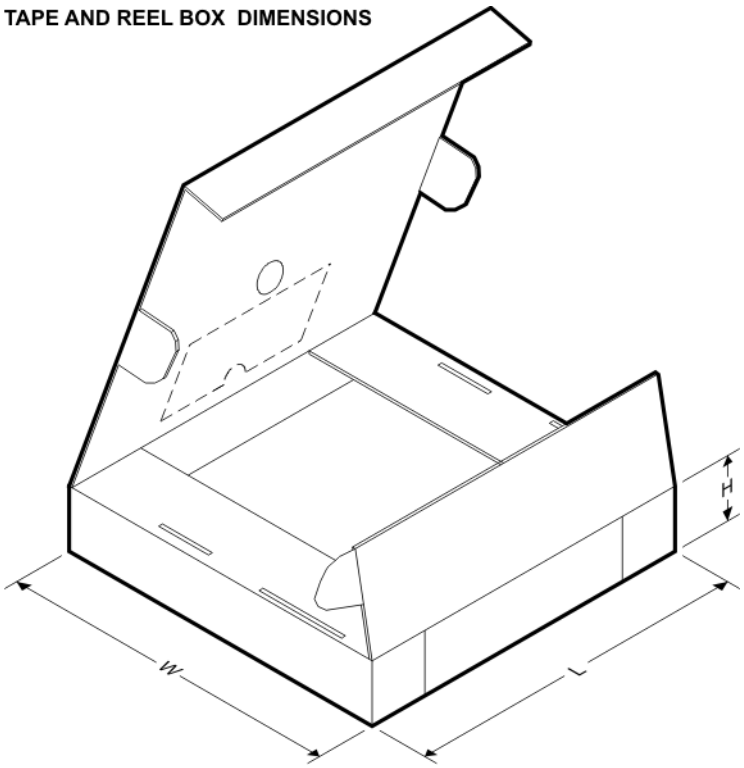
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL0501-100DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPL0501-100RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q1

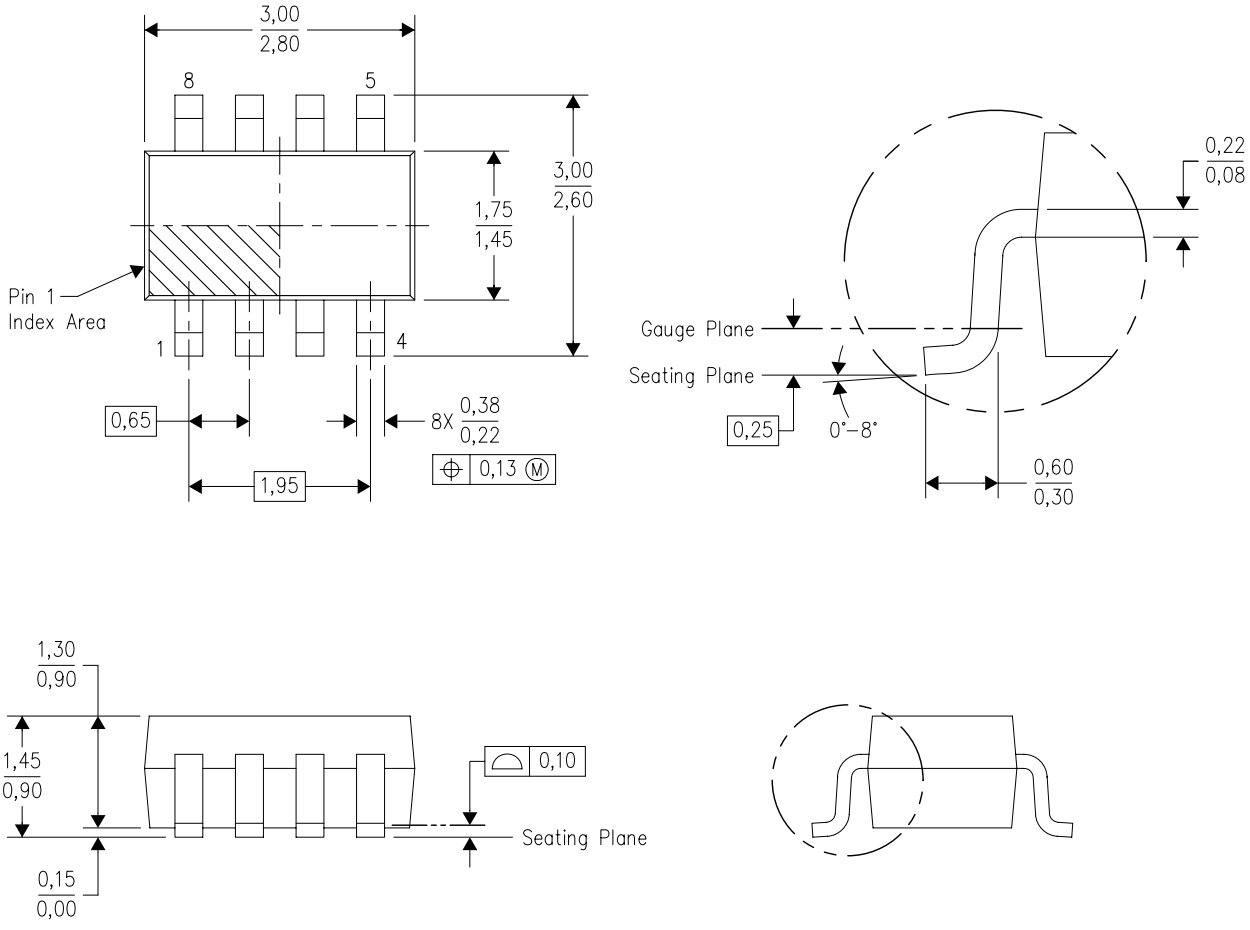
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

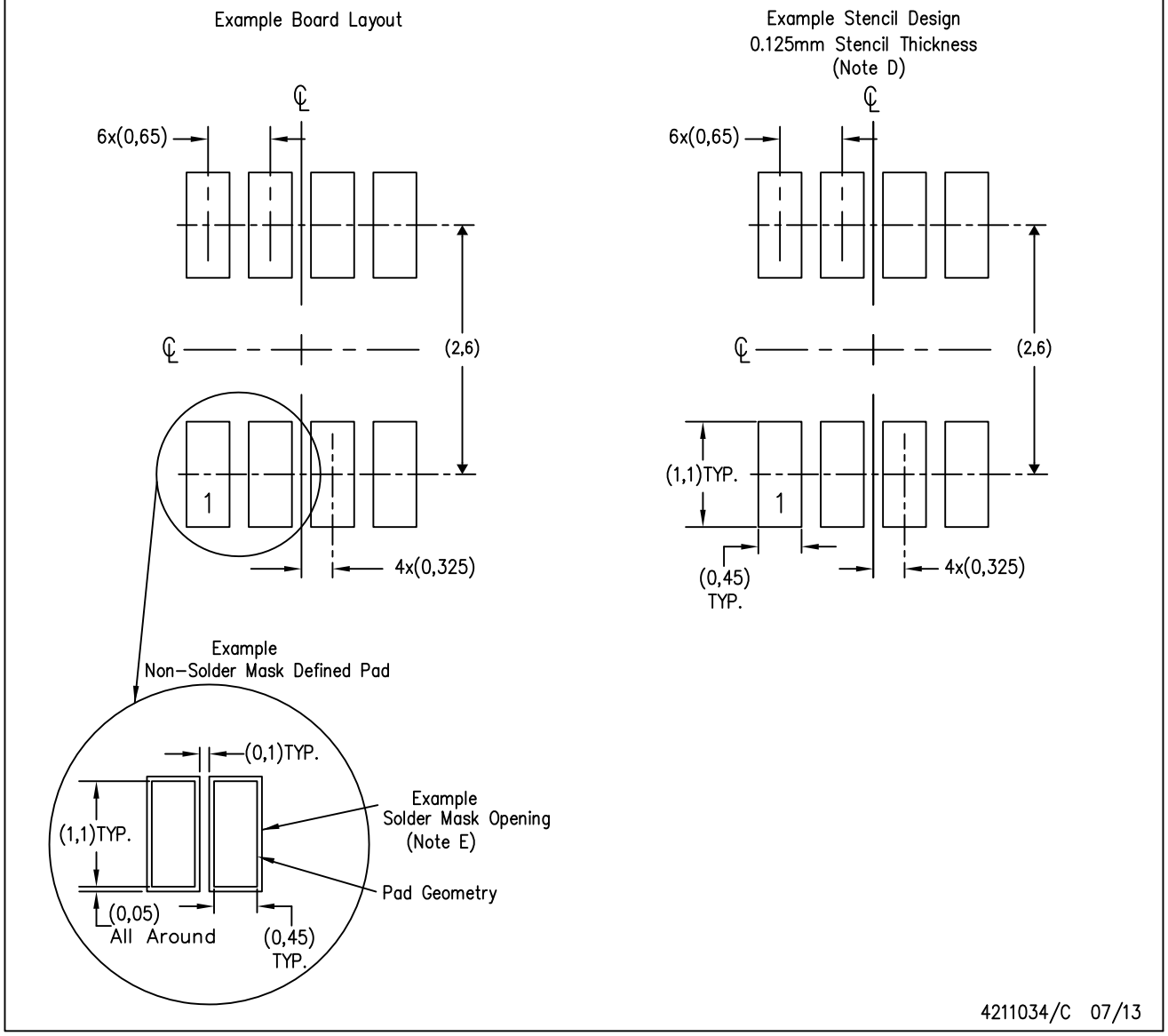
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL0501-100DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TPL0501-100RSER	UQFN	RSE	8	5000	202.0	201.0	28.0

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



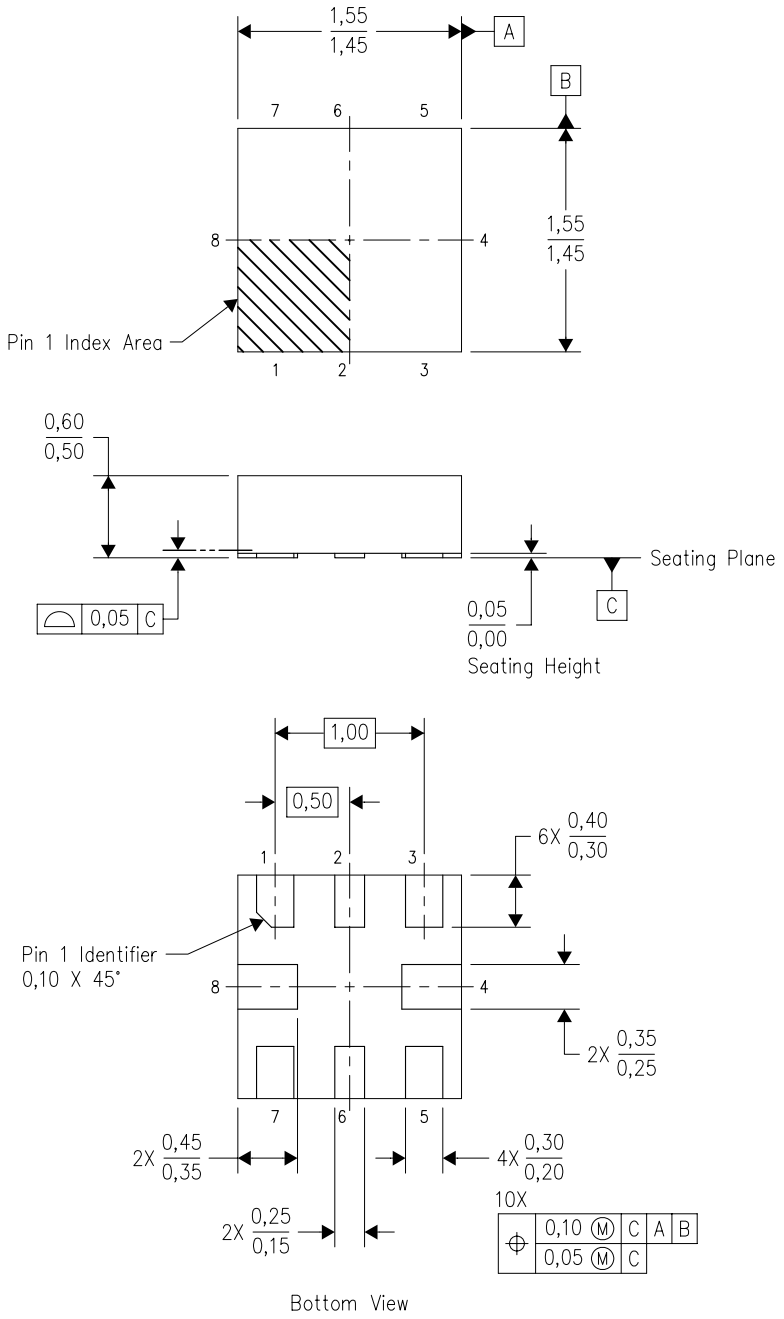
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

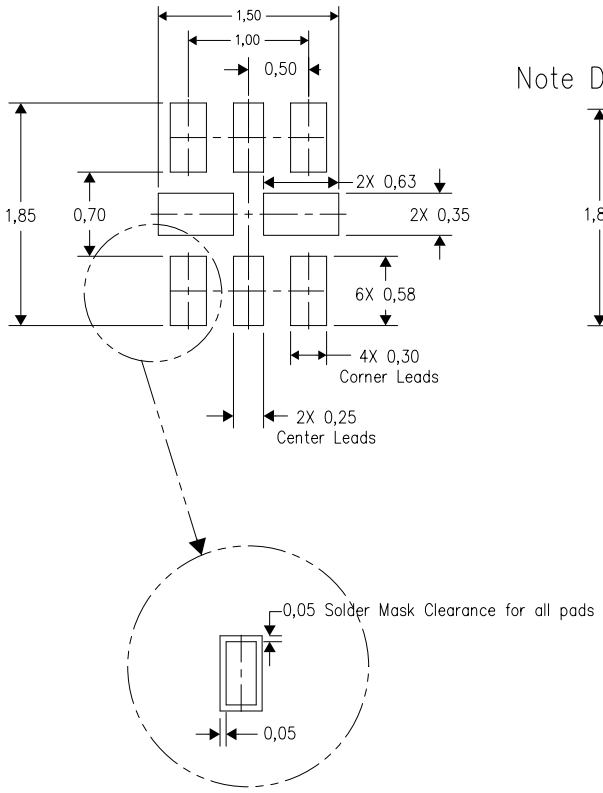


4207268–2/D 01/11

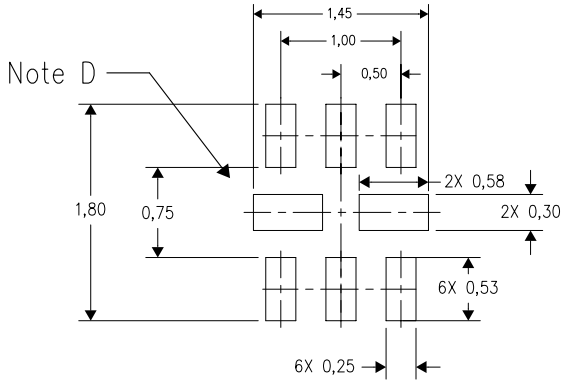
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UECD.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)



4208106–2/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com