NVMFS5885NL

Power MOSFET
60 V, 15 mΩ, 39 A, Single N−Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFS5885NLWF − Wettable Flanks Product
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3)	Steady State	T_{mb} = 25°C	I_D	39	A
		T_{mb} = 100°C		28	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)		T_{mb} = 25°C	P_D	54	W
		T_{mb} = 100°C		27	
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3)	Steady State	T_A = 25°C	I_D	10.2	A
		T_A = 100°C		7.2	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)		T_A = 25°C	P_D	3.7	W
		T_A = 100°C		1.8	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	179	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	46	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, $I_{L(pk)}$ = 18 A, L = 0.3 mH, R_G = 25 Ω)			E_{AS}	49	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Mounting Board (top) − Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	2.8	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	41	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.

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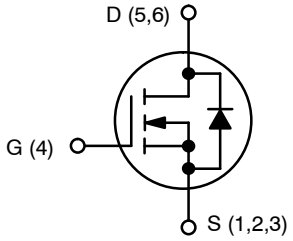
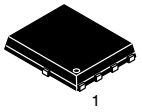
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	15 mΩ @ 10 V	39 A
	21 mΩ @ 4.5 V	

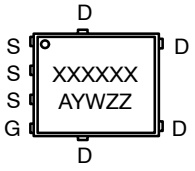


N−CHANNEL MOSFET



DFN5
(SO−8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		2.5	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A			11.6	15	mΩ
		V_{GS} = 4.5 V, I_D = 15 A			15.2	21	
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			1340		pF
Output Capacitance	C_{oss}				125		
Reverse Transfer Capacitance	C_{rss}				85		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 15 A			12		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.1		
Gate−to−Source Charge	Q_{GS}				4.0		
Gate−to−Drain Charge	Q_{GD}				6.3		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 15 A			21		nC
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 15 A, R_G = 2.5 Ω			10		ns
Rise Time	t_r				64		
Turn−Off Delay Time	$t_{d(OFF)}$				18		
Fall Time	t_f				52		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 15 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 15 A			20		ns
Charge Time	t_a				15		
Discharge Time	t_b				5.0		
Reverse Recovery Charge	Q_{RR}				16		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

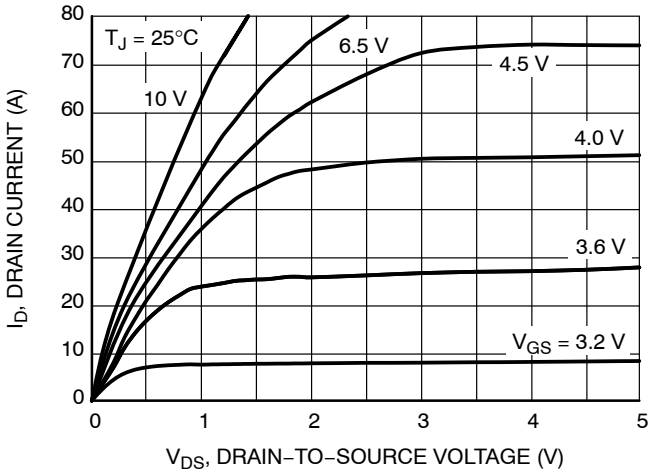


Figure 1. On−Region Characteristics

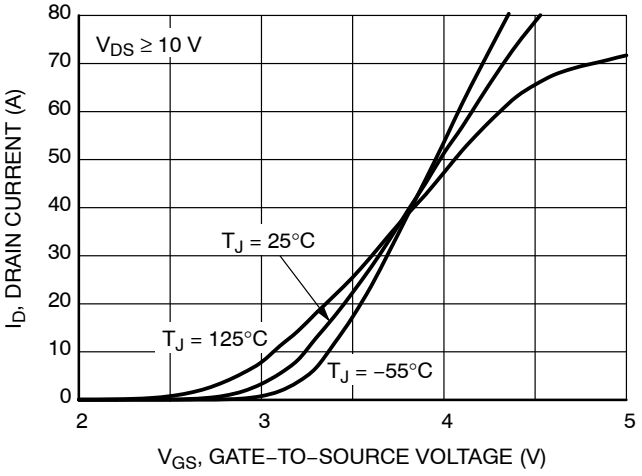


Figure 2. Transfer Characteristics

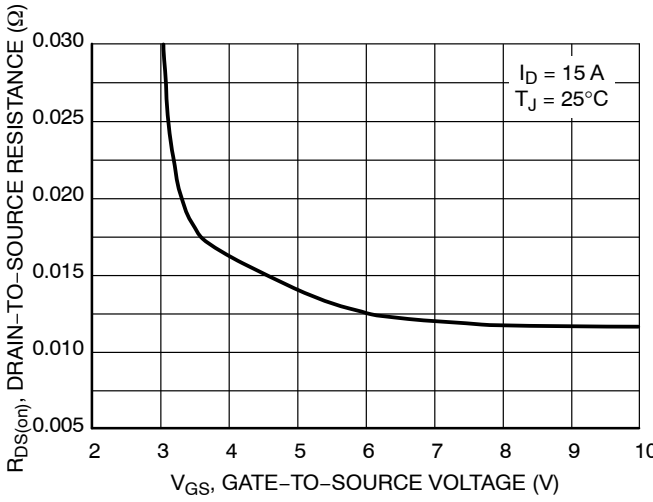


Figure 3. On−Resistance vs. Gate−to−Source Voltage

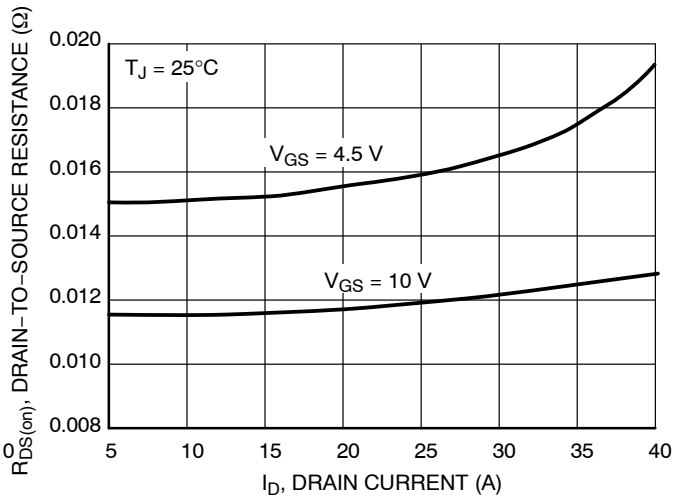


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

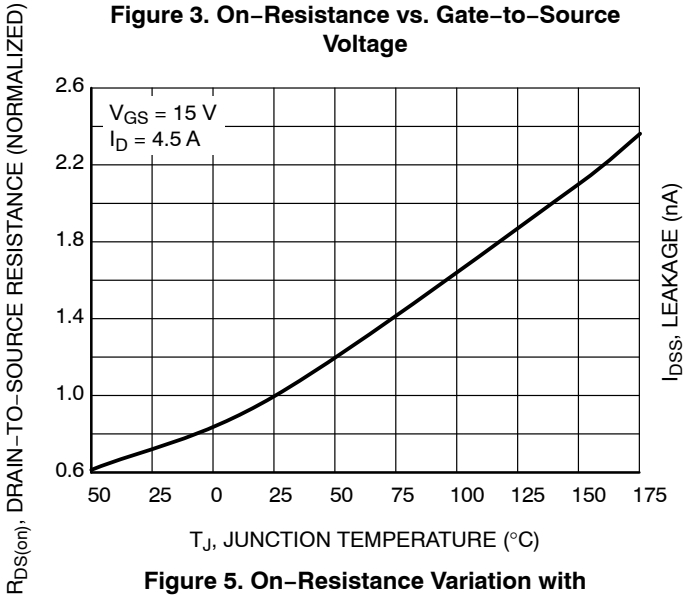


Figure 5. On−Resistance Variation with Temperature

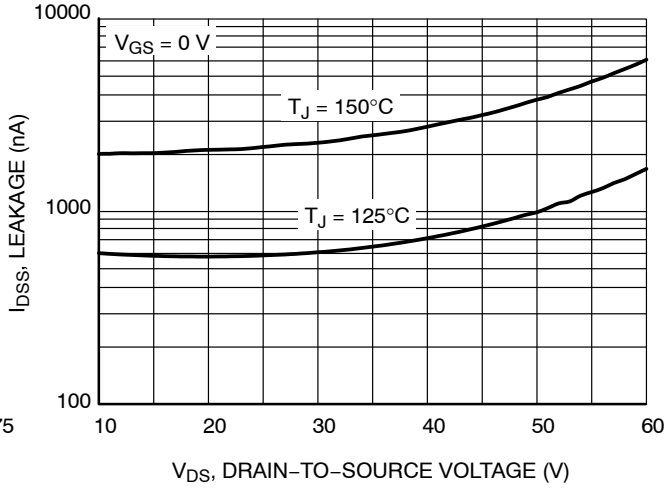


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

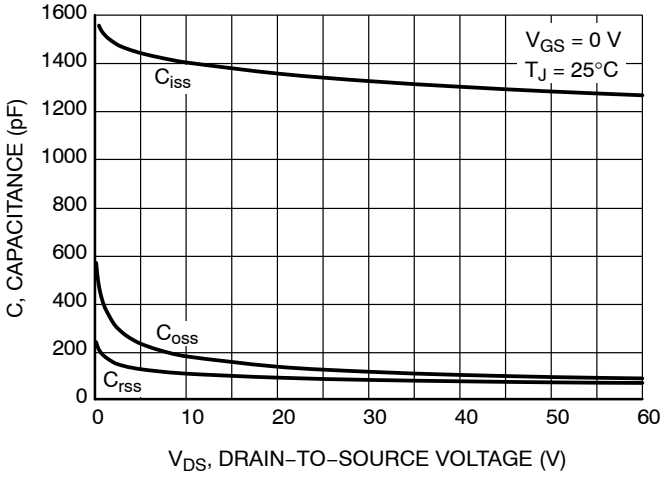


Figure 7. Capacitance Variation

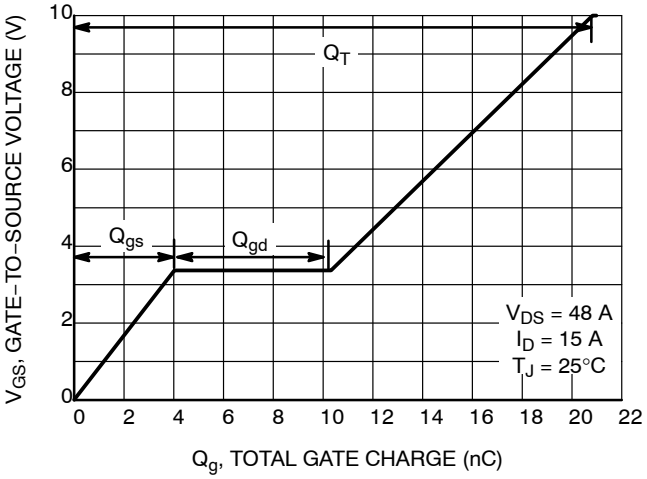


Figure 8. Gate−to−Source Voltage vs. Total Charge

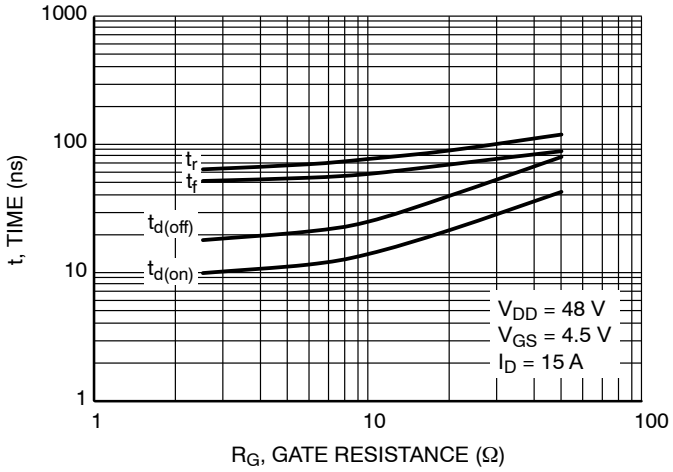


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

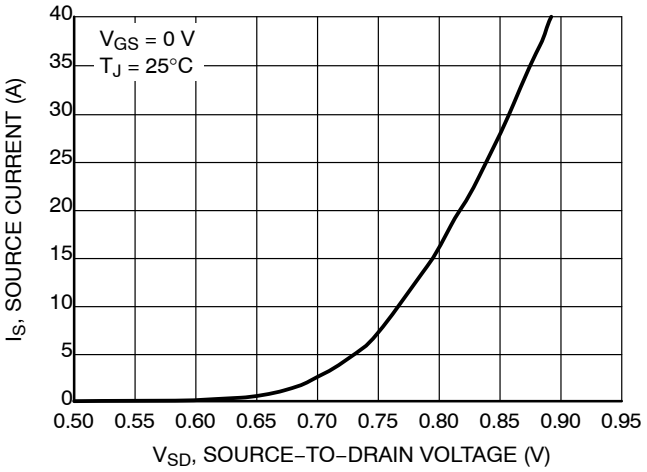


Figure 10. Diode Forward Voltage vs. Current

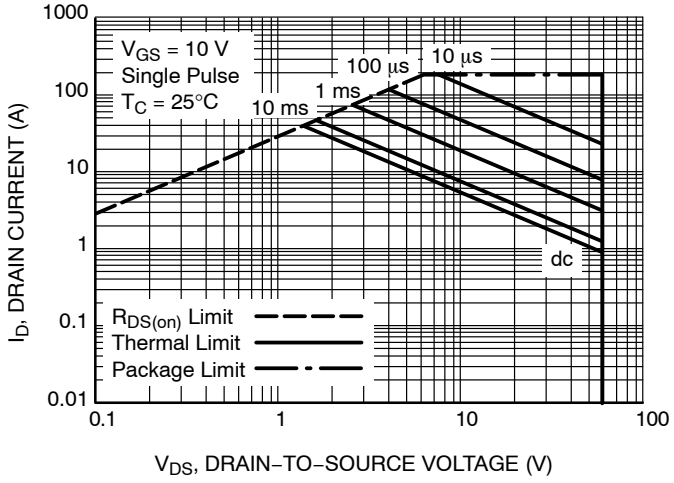


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

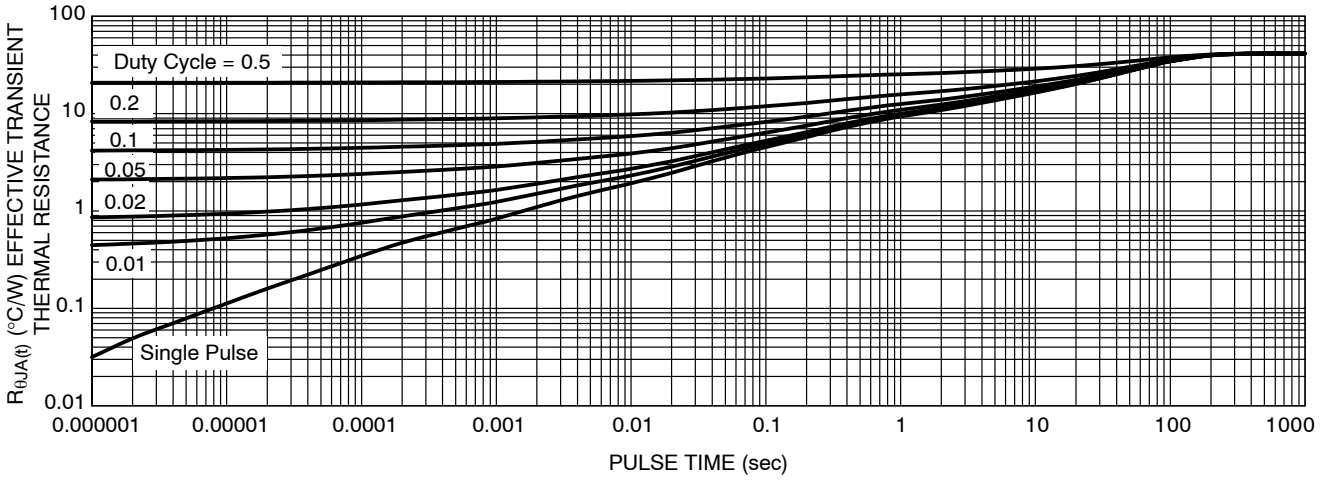


Figure 12. Thermal Response

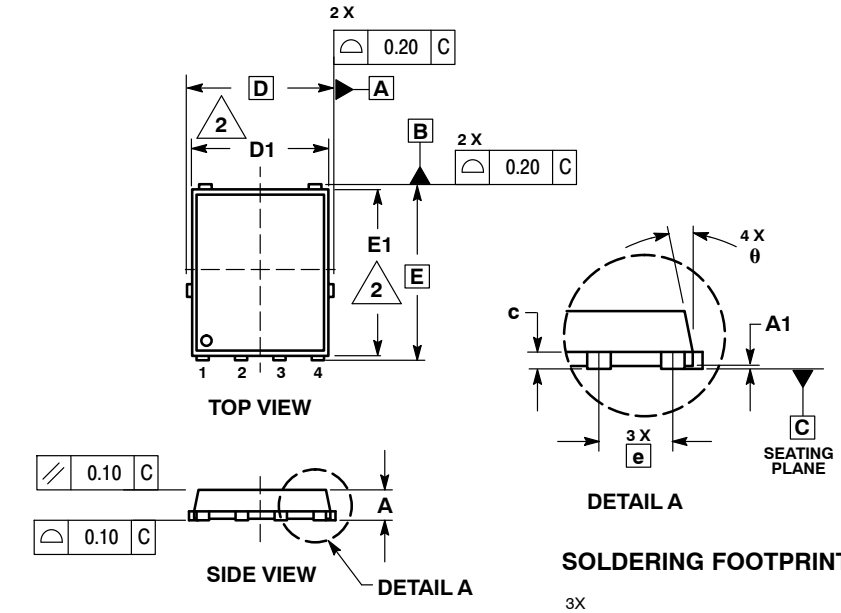
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS5885NLT1G	V5885L	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5885NLWFT1G	5885LW	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5885NLT3G	V5885L	DFN5 (Pb−Free)	5000 / Tape & Reel
NVMFS5885NLWFT3G	5885LW	DFN5 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

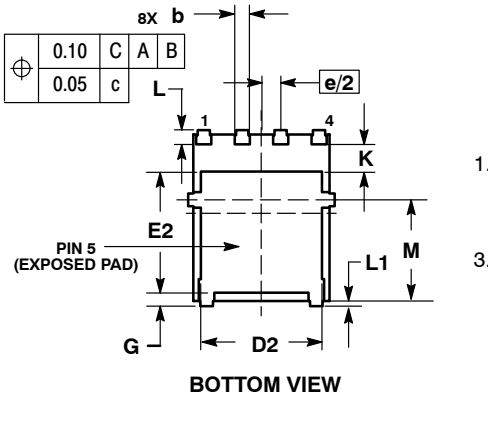
PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE H

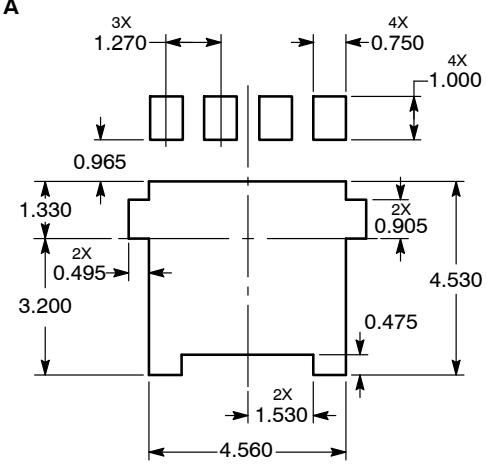


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E		6.15 BSC	
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e		1.27 BSC	
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	−−−	12 °



SOLDERING FOOTPRINT*



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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P.O. Box 5163, Denver, Colorado 80217 USA
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