LM96550 Ultrasound Transmit Pulser

Check for Samples: LM96550

FEATURES

- **8-Channel High-Voltage CMOS Pulse Generator**
- **Output Pulses with ±50V and 2A Peak Current**
- **Active Damper with Built-In Blocking Diodes**
- **Up to 15 MHz Operating Frequency**
- **Matched Delays for Rising and Falling Edges**
- **Low Second Harmonic Distortion Allows and Improves Harmonic Imaging**
- **Continuous-Wave (CW) Operation Down to ±3.3V**
- **Low Phase Noise Enables Doppler Measurements**
  - **-145 dBc/Hz Phase Noise at 10 MHz (1 kHz offset)**
- **Output State Over-Temperature Protection**
- **Blocking Diodes for Direct Interface to Transducer**
- **2.5V to 5.0V CMOS Logic Interface**
- **Low-Power Consumption per Channel**
- **Over Temperature Protection**

KEY SPECIFICATIONS

- **Output Voltage: ±50 V**
- **Output Peak Current: ±2.0 A**
- **Output Pulse Rate: Up to 15 MHz**
- **Rise/fall Delay Matching (Max): < 3 ns**
- **Pulser HD2 (5 MHz): -40 dB**
- **Operating Temp. : 0 to +70 °C**

APPLICATIONS

- **Ultrasound Imaging**

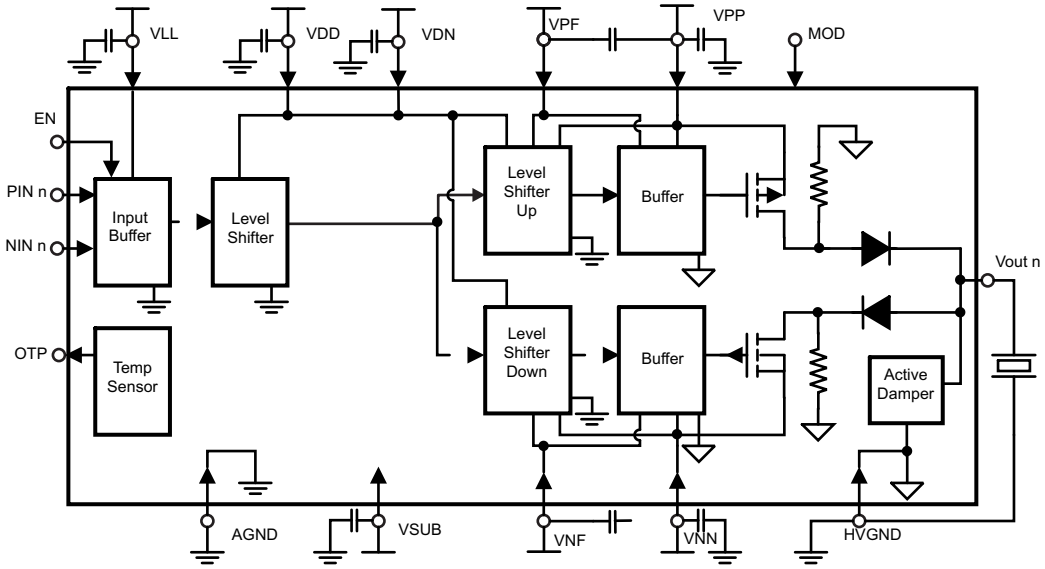
DESCRIPTION

The LM96550 is an eight-channel monolithic high-voltage, high-speed pulse generator for multi-channel medical ultrasound applications. It is well-suited for use with TI's LM965XX series chipset which offers a complete medical ultrasound solution targeted towards low-power, portable systems.

The LM96550 contains eight high-voltage pulsers with integrated diodes generating ±50V bipolar pulses with peak currents of up to 2A and pulse rates of up to 15 MHz. Advanced features include low-jitter and low-phase-noise output pulses ideal for continuous-wave (CW) modes of operation. Active clamp circuitry is integrated for ensuring low harmonic distortion of the output signal waveform.

The LM96550 also features a low-power operation mode and over-temperature protection (OTP) which are enabled by on-chip temperature sensing and power-down logic.

BLOCK DIAGRAM



Typical Application

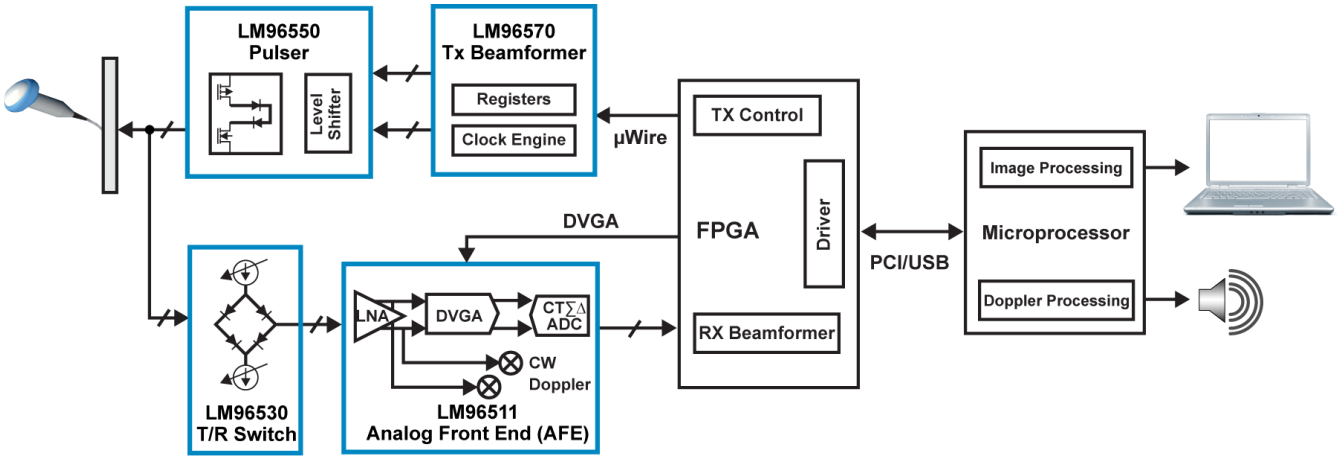


Figure 1. 8-Channel Transmit/Receive Chipset

Pin Diagram

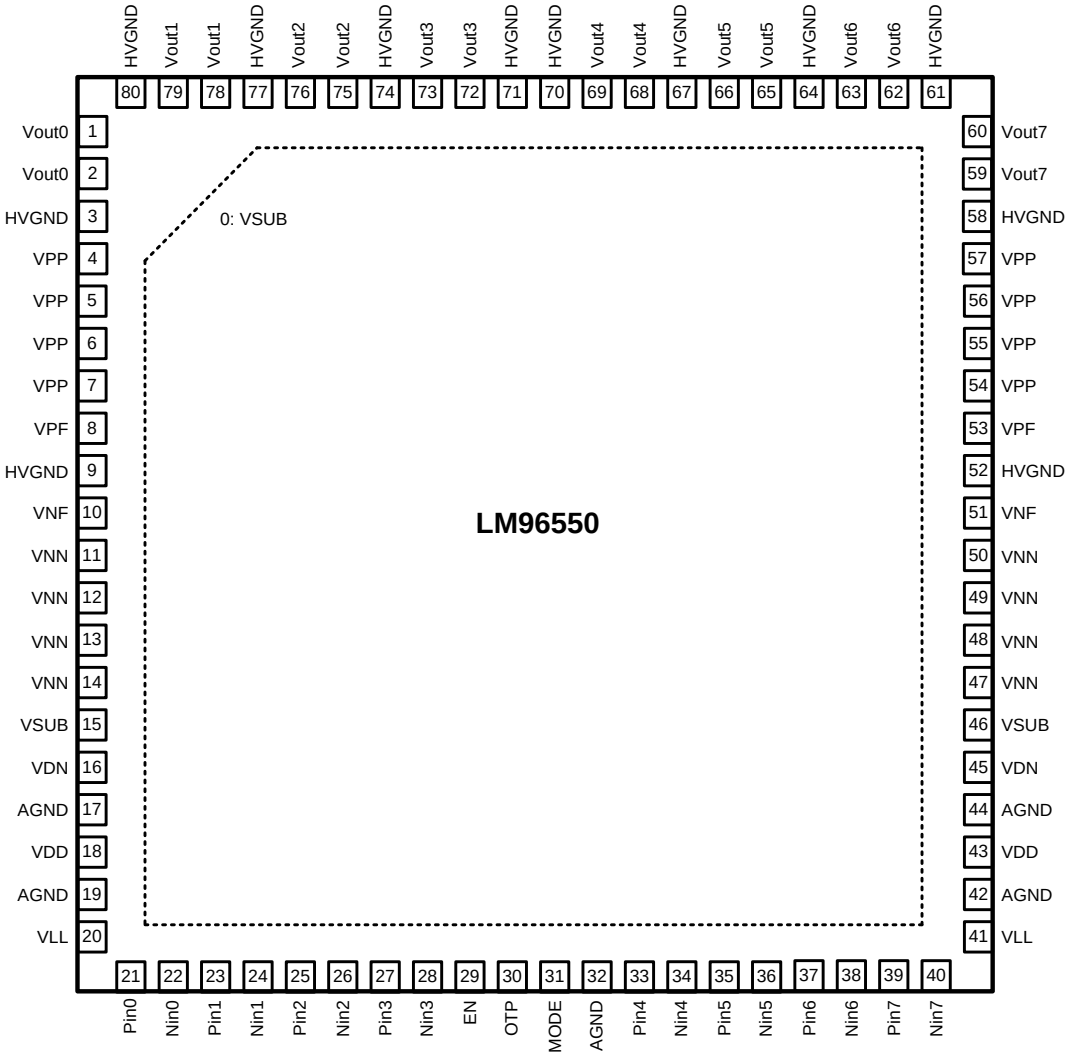


Figure 2. WQFN
Pin Diagram of LM96550

PIN DESCRIPTIONS

Pin No.	Name	Type	Function and Connection
21, 23, 25, 27, 33, 35, 37, 39	PIN n=0...7	Input	Logic control positive output channel P 1 = ON 0 = OFF
22, 24, 26, 28, 34, 36, 38, 40	NIN n=0...7	Input	Logic control negative output channel N 1 = ON 0 = OFF
59, 60	V_{OUT7}	Output	High voltage output of channels 0 to 7
62, 63	V_{OUT6}		
65, 66	V_{OUT5}		
68, 69	V_{OUT4}		
72, 73	V_{OUT3}		
75, 76	V_{OUT2}		
78, 79	V_{OUT1}		
1, 2	V_{OUT0}		
29	EN	Input	Chip power enable 1 = ON 0 = OFF
31	MODE	Input	Output current mode control 1 = Max Current 0 = Low Current
30	OTP	Output	Over-temperature indicating IC temp > 125°C 0 = Over-temperature 1 = Normal temperature This pin is open-drain.
4, 5, 6, 7, 54, 55, 56, 57	VPP	Power	Positive high voltage power supply (+3.3V to +50V)
11, 12, 13, 14, 47, 48, 49, 50	VNN	Power	Negative high voltage power supply (-3.3V to -50V)
8, 53	VPF	Power	Positive floating power supply (VPP -10V)
10, 51	VNF	Power	Negative floating power supply (VNN +10V)
18, 43	VDD	Power	Positive level-shifter supply voltage (+10V)
16, 45	VDN	Power	Negative level-shifter supply voltage (-10V)
20, 41	VLL	Power	Logic supply voltage. Hi voltage reference input (+2.5 to +5V)
0, 15, 46	VSUB	Power	All VSUB pins must be connected to most negative potential of the IC. NOTE: The exposed thermal pad is connected to VSUB.
3, 9, 52, 58, 61, 64, 67, 70, 71, 74, 77, 80	HVGND	Ground	High voltage reference potential (0V)
17, 19, 32, 42, 44	AGND	Ground	Analog and Logic voltage reference input, logic ground (0V)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Maximum Junction Temperature (T_{JMAX})	+150°C
Storage Temperature Range	−40°C to +125°C
Supply Voltage (VDD)	–0.3V to +12V
Supply Voltage (VDN)	+0.3V and −12V
Supply Voltage (VPP)	–0.3V and +55V
Supply Voltage (VPF)	VPP −14V
Supply Voltage (VNN)	+0.3V and −55V
Supply Voltage (VNF)	VNN +14V
Supply Voltage (VSUB)	−65V
IO Supply Voltage (VLL)	−0.3V to +5.5V
Voltage at Logic Inputs	−0.3V to VLL +0.3V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured to be functional, but do not specify specific performance limits. For specifications and test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

OPERATING RATINGS

Operation Junction Temperature		0°C to + 70°C
VPP, −VNN; High-voltage supply		+3.3V to +50V
VPF, −VNF; Floating supply		VPP −10V
VDD, −VDN; Level-shift supply		+9V to 11V
VLL, Logic Supply		+2.4V to +5.3V
VSUB, Substrate bias supply		must be most negative supply
Package Thermal Resistance (θ_{JA})		19.7°C/W
ESD Tolerance	Human Body Model	2kV
	Machine Model	150V
	Charge Device Model	750V

ANALOG CHARACTERISTICS

Unless otherwise stated, the following conditions apply
VLL = +3.3V, VPP = −VNN = 50V, VPF = −VNF = VPP-10V, VDD = −VDN = 10V, VSUB = −55V, R_L = 2 KΩ, T_A = 25°C, Mode = LO, EN = HI, Fin=5MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{OUT}	Output Frequency Range	R_L = 100Ω	1		15	MHz
	Output Voltage Range		-48.5		+48.5	V
	Output Current	2% Duty Cycle		2		A
	Output Current	100% Duty Cycle, Mode=HI		0.6		
HD2	Second harmonic distortion	R_L = 100Ω || C_L = 330pF (See (1))		-40		dBc
R_{ON}	Output ON Resistance	100 mA		7	11	Ω
	Output clamp	Positive or Negative pulse		2		A

(1) VNF = -42V, VPF = 38V

ANALOG CHARACTERISTICS (continued)

Unless otherwise stated, the following conditions apply
VLL = +3.3V, VPP = −VNN = 50V, VPF = −VNF = VPP-10V, VDD = −VDN = 10V, VSUB = −55V, R_L = 2 KΩ, T_A = 25°C, Mode = LO, EN = HI, Fin=5MHz

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	Power Supply Current	Pin = Nin = 0	VPP		0.7	3	mA
			VNN		0.5	4.5	
			VDD		8	13	
			VDN		4	7	
			VLL		25	50	µA
			VSUB		1.2	6	mA
			VPF		0.1	1.5	
			VNF		0.1	1.5	
		En = 0	VPP		0.7	3	mA
			VNN		0.5	4.5	
			VDD		0.4	2.7	
			VDN		0.1	2.2	
			VLL		25	50	µA
			VSUB		1.2	6	mA
			VPF		0.1	1.5	
			VNF		0.1	1.5	
OPT	Over Temperature Protection				125		°C
σ_{OTP}	OTP sigma				3.0		°C
$Hsys_{OTP}$	OTP hysteresis				5.5		°C

AC AND TIMING CHARACTERISTICS

Unless otherwise stated, the following conditions apply.
VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, VPF = −VNF = 40V, C_L = 330pF, R_L = 100 Ω, T_A = 25°C, Fin=5MHz, Mode=LO, EN=HI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	Output rise time	See (1)		18	26	ns
t_f	Output fall time			18	26	
t_E	Enable time			1		µs
t_{dr}	Delay time on inputs rise	See (1)		32	39	ns
t_{df}	Delay time on inputs fall			32	39	
$\lvert t_{dr} - t_{dr} \rvert$	Delay time mismatch	P-to-N See (1)(2)			3	
t_{dm}	Delay on mode change			1		µs

(1) VNF = -42V, VPF = 38V
(2) The delay time mismatch can be adjust to be less than 0.8ns with the LM96570 duty cycle control function.

DC CHARACTERISTICS

Unless otherwise stated, the following conditions apply.
VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, VPF = −VNF = 40V, T_A = 25°C,

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low Input “LO” threshold				1	V
V_{IH}	High Input “HI” threshold		2.3			V
I_{IN}	input current			1		µA

OVERVIEW

The LM96550 pulser provides an 8-channel transmit side solution for medical ultrasound applications suitable for integration into multi-channel (128/256 channel) systems. Its flexible, integrated ±50V pulser architecture enables low-power designs targeting portable systems. A complete system can be designed using TI's companion LM965XX chipset.

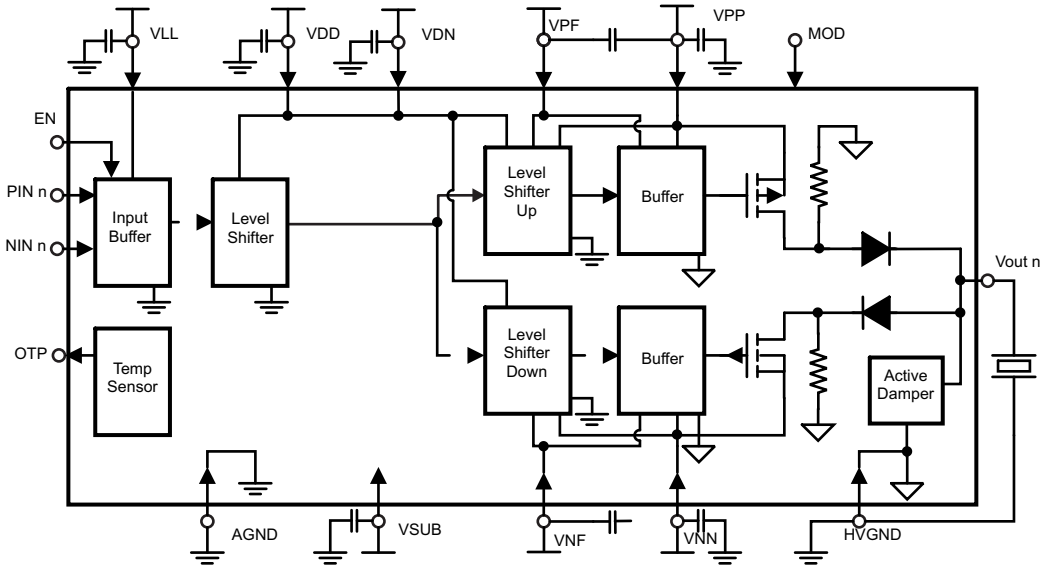


Figure 3. Block Diagram of High-Voltage Pulser Channel

A functional block diagram of the LM96550 is shown in Figure 3. It has an input buffer at its CMOS logic interface, which is powered by VLL (2.5 to 5.0V). When EN=HI, driving a channel's inputs (PIN n or NIN n) HI will result in a positive or negative pulse at the channel's output pin (V_{OUT} n), respectively. The output pins V_{OUT} are pulled to either the positive or negative supplies, VPP or VNN by power MOSFETs.

When PIN and NIN are both LO, Vout is actively clamped to GNDHI at 0V. This clamping reduces harmonic distortions compared to competing architectures that use bleeding resistors for implementing the return to zero of the output. **The user must avoid the condition in which PIN and NIN are both HI simultaneously, as this will damage the output stage!**

The impedance of the output stage can be controlled via the Mode-pin. When the Mode = HI as shown, only one output transistor pair drives the output resulting in a peak current of 600 mA at VPP = -VNN = 50V. When Mode=LO, a peak-current of 2A is achievable resulting in faster transients at the output. However, faster output transients can lead to significant overshoot of the output signal. This can be avoided using the lower drive current option.

Continuous-wave (CW) applications are supported for low power consumption down to VPP = -VNN = 3.3V with Mode =HI.

Internally, the CMOS logic input signals are level shifted to VDD = 10V and VDN = -10V for pulse transmission. The outputs of the level shifter drive the high-voltage P and N drivers that control the output power MOSFETs, which are supplied from the positive and negative rails VPP and VNN, respectively. The high-voltage rails are designed for a maximum of 50V; however, they can be operated down to 3.3V. The necessary gate-overdrive voltage levels for the output drivers are internally generated from the high-voltage rails.

Over-Temperature Protection (OTP) is implemented by continuously monitoring the on-chip temperature. The OTP output (open drain) pin goes LO when the chip temperature exceeds a critical level. Prior to this event, the user must ensure that the chip is powered down before fatal damage occurs. In addition to a primary software controlled safety shutdown, the OTP pin can be also be hard-wired to the EN pin as a secondary safety measure.

Timing Diagrams

RISE AND FALL TIME

The timing diagram shown in Figure 4 defines the rise and fall times tr and tf.

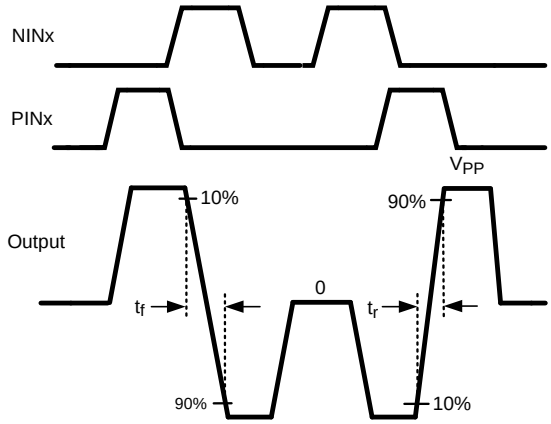


Figure 4. Timing Diagram Defining Rise and Fall Times tr and tf, respectively

INPUT TO OUTPUT DELAY

The timing diagram shown in Figure 5 defines the delays between the input and output signals.

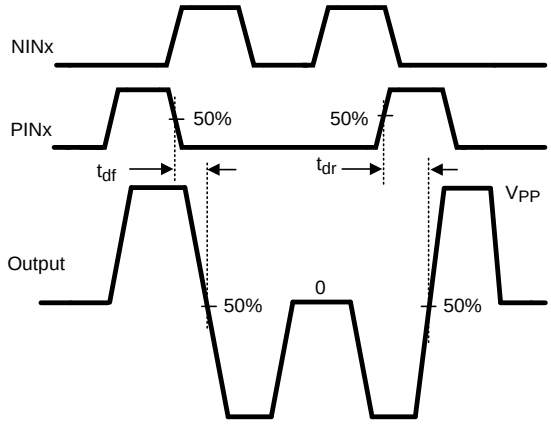


Figure 5. Timing Diagram Defining Input-to-Output Delays Times

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise stated, the following conditions apply.
VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, VPF = VPP-12V, VNF = VNN+8V, C_L = 330pF, R_L = 100Ω, T_A = 25°C, Fin=5MHz, Mode=LO, EN=HI

Return-to-Zero Rise Time (R_L = 2KΩ)

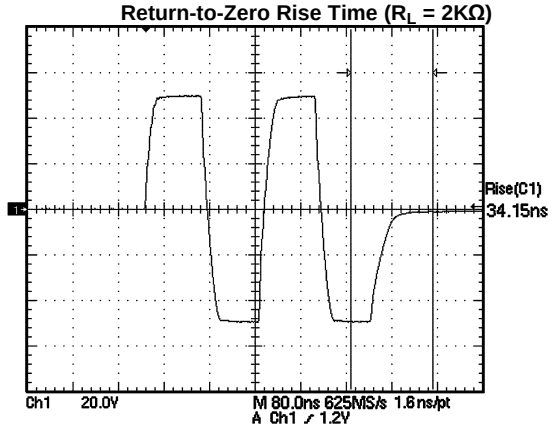


Figure 6.

Return-to-Zero Fall Time (R_L = 2KΩ)

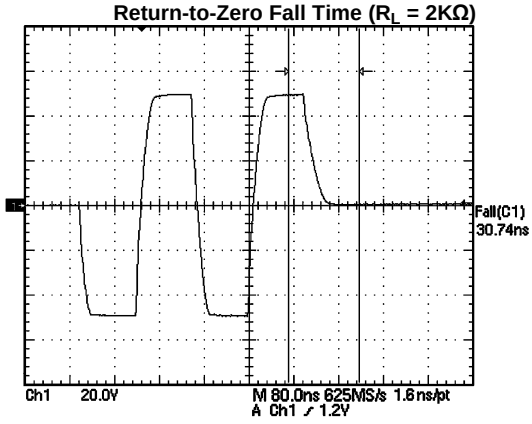


Figure 7.

Harmonic Distortion (8 pulses)

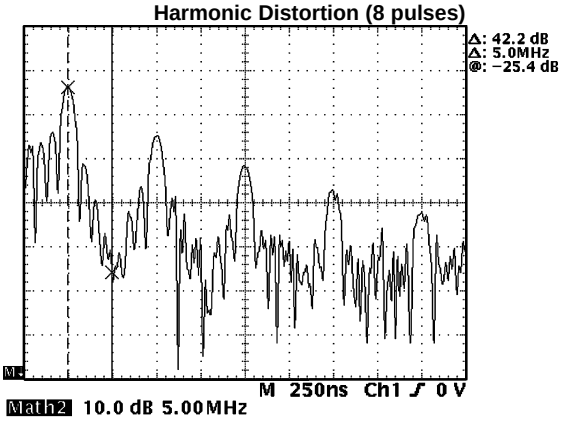


Figure 8.

Differential Input vs. Pulser Output Phase Noise(1)

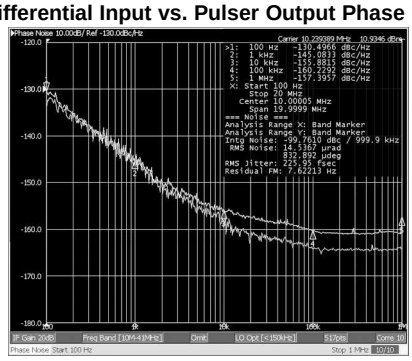


Figure 9.

Constant 5W Total Power (R_L = 300Ω)
100% CW mode, Mode=HI, VSUB=-10V, VPF=-VNF=VPP-10V

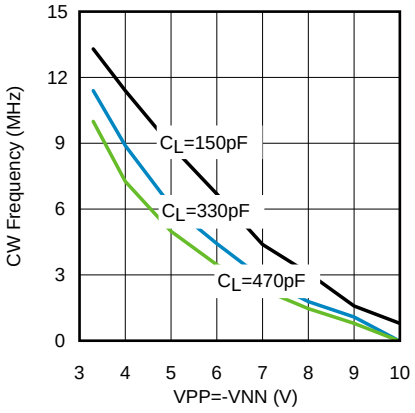


Figure 10.

Over Temperature Protection

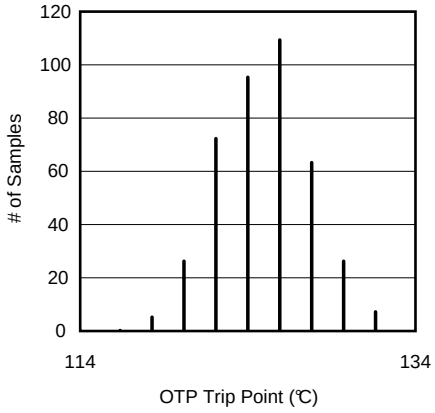


Figure 11.

(1) 10.24 MHz Differential Input signal from LMK04800 Evaluation board with 122.88 MHz Crystek CVHD-950 VCXO clock source. The LMK04800 clock output channel was configured with a divide value of 12 and LVCMOS outputs with opposite polarity.

FUNCTIONAL DESCRIPTION

Note that the case, PINn = NNn = HI is not allowed as it will damage the output transistors.

Logic inputs			Output
EN	PINn	NINn	Voutn
1	0	0	0V
1	1	0	VPP - 0.7V
1	0	1	VNN + 0.7V
1	1	1	**not allowed**
0	X	X	0V

APPLICATIONS INFORMATION

POWER-UP AND POWER-DOWN SEQUENCES

VSUB must always be the most negative supply, i.e., it must be equal to or more negative than the most negative supply, VNN or VDN. VPF ≥ VPP −14V AND VNF = ≤ VNN +14V at all times.

Power UP Sequence:

1. Turn ON VSUB, hold EN pin LO
2. Turn ON VLL
3. Turn ON VDD, VDN, VPP, VPF, VNN and VNF

Power DOWN Sequence:

1. Turn OFF VDD, VDN, VPP, VPF, VNN and VNF
2. Turn OFF VLL
3. Turn OFF VSUB

REVISION HISTORY

Changes from Revision E (May 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM96550SQX/NOPB	ACTIVE	WQFN	NKF	80	2000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR		LM96550SQ	Samples

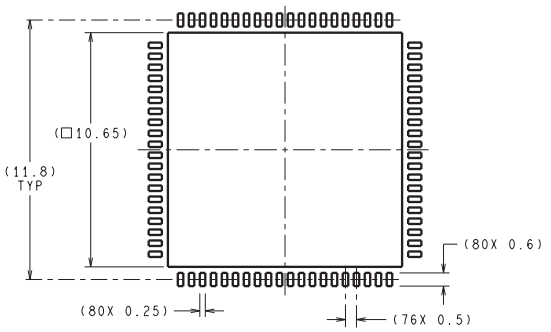
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

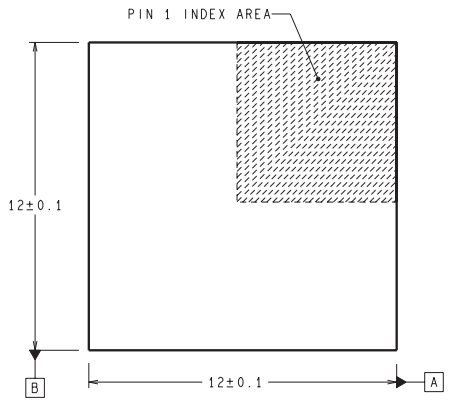
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

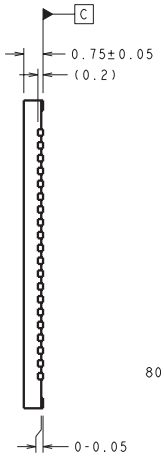
NKF0080A

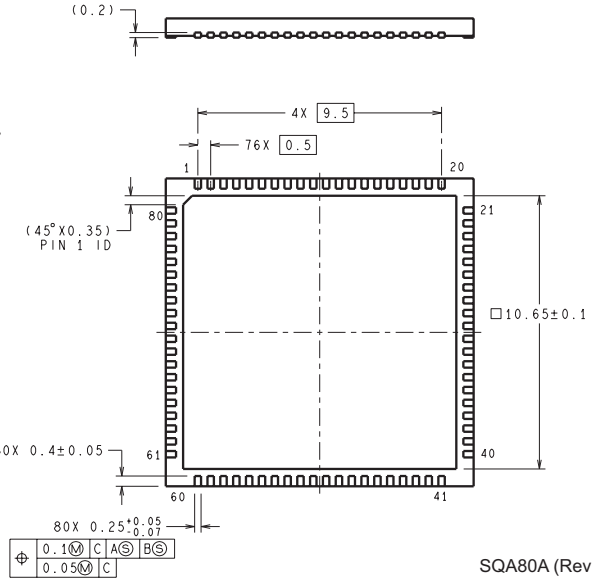


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SQA80A (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com