

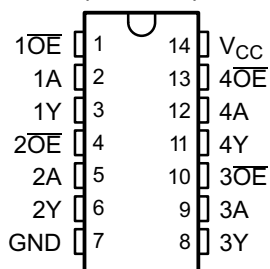
## QUADRUPLE 2-INPUT POSITIVE-NAND GATES

 Check for Samples: [SN54AHC125](#), [SN74AHC125](#)

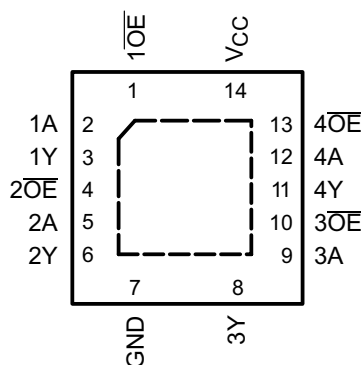
### FEATURES

- Operating Range 2-V to 5.5-V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

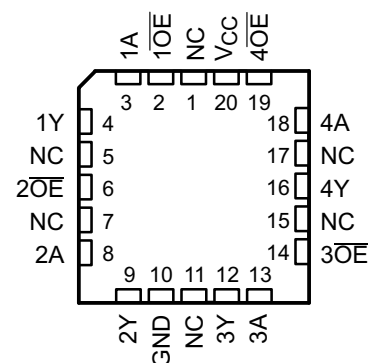
SN54AHC125 . . . J OR W PACKAGE  
SN74AHC125 . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74AHC125 . . . RGY PACKAGE  
(TOP VIEW)



SN54AHC125 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

### DESCRIPTION

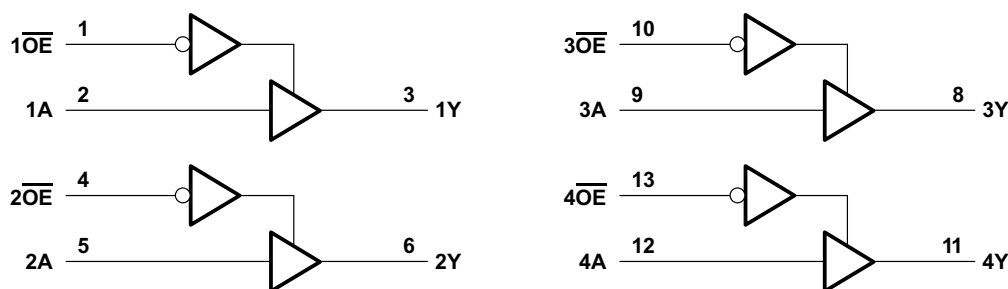
The 'AHC125 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high. When OE is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE  
(EACH BUFFER)**

INPUTS		OUTPUT
$\overline{\text{OE}}$	A	Y
L	H	H
L	L	L
H	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT
Supply voltage range, $V_{CC}$		-0.5 to 7	V
Input voltage range, $V_I$ <sup>(2)</sup>		-0.5 to 7	V
Output voltage range, $V_O$ <sup>(2)</sup>		-0.5 to $V_{CC} + 0.5$	V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		-20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )		$\pm 20$	mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )		$\pm 25$	mA
Continuous current through $V_{CC}$ or GND		$\pm 50$	mA
Package thermal impedance, $\theta_{JA}$ <sup>(3)</sup>	D package	86	°C/W
	DB package	96	
	DGV package	127	
	N package	80	
	NS package	76	
	PW package	113	
Storage temperature range, $T_{stg}$		-65 to 150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		SN54AHC125		SN74AHC125		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 3$ V	2.1	2.1		
		$V_{CC} = 5.5$ V	3.85	3.85		
$V_{IL}$	Low-level Input voltage	$V_{CC} = 2$ V		0.5	0.5	V
		$V_{CC} = 3$ V		0.9	0.9	
		$V_{CC} = 5.5$ V		1.65	1.65	
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V		-50	-50	mA
		$V_{CC} = 3.3$ V $\pm 0.3$ V		-4	-4	
		$V_{CC} = 5$ V $\pm 0.5$ V		-8	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V		50	50	mA
		$V_{CC} = 3.3$ V $\pm 0.3$ V		4	4	
		$V_{CC} = 5$ V $\pm 0.5$ V		8	8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3$ V $\pm 0.3$ V		100	100	ns/V
		$V_{CC} = 5$ V $\pm 0.5$ V		20	20	
$T_A$	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
						SN54AHC125		SN74AHC125		Recommended SN74AHC125		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	I <sub>OH</sub> = 4 mA	3 V			0.36		0.5		0.44		0.5	
	I <sub>OH</sub> = 8 mA	4.5 V			0.36		0.5		0.44		0.5	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(1)</sup>		±1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40		40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10				10			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
						SN54AHC125		SN74AHC125		Recommended SN74AHC125		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	5.6 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	1	9.5	ns
t <sub>PHL</sub>				5.6 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	1	9.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF	5.4 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	1	9.5	ns
t <sub>PZL</sub>				5.4 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5	1	9.5	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF	7.0 <sup>(1)</sup>	9.7 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	ns
t <sub>PLZ</sub>				7.0 <sup>(1)</sup>	9.7 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	8.1	11.5	1	13	1	13	1	13	ns
t <sub>PHL</sub>				8.1	11.5	1	13	1	13	1	13	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF	7.9	11.5	1	13	1	13	1	13	ns
t <sub>PZL</sub>				7.9	11.5	1	13	1	13	1	13	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF	9.5	13.2	1	15	1	15	1	15	ns
t <sub>PLZ</sub>				9.5	13.2	1	15	1	15	1	15	
tsk(o)	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		1.5 <sup>(2)</sup>				1.5			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
						Recommended						
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	3.8 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	ns
$t_{PHL}$				3.8 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	3.6 <sup>(1)</sup>	5.1 <sup>(1)</sup>	1 <sup>(1)</sup>	6 <sup>(1)</sup>	1	6	1	6	ns
$t_{PZL}$				3.6 <sup>(1)</sup>	5.1 <sup>(1)</sup>	1 <sup>(1)</sup>	6 <sup>(1)</sup>	1	6	1	6	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.6 <sup>(1)</sup>	6.8 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	ns
$t_{PLZ}$				4.6 <sup>(1)</sup>	6.8 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	8 <sup>(1)</sup>	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	1	8.5	1	8.5	ns
$t_{PHL}$				5.3	7.5	1	8.5	1	8.5	1	8.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	5.1	7.1	1	8	1	8	1	8	ns
$t_{PZL}$				5.1	7.1	1	8	1	8	1	8	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.1	8.8	1	10	1	10	1	10	ns
$t_{PLZ}$				6.1	8.8	1	10	1	10	1	10	
$t_{sk}(0)$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		1 <sup>(2)</sup>				1			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## NOISE CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER		SN74AHC125		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

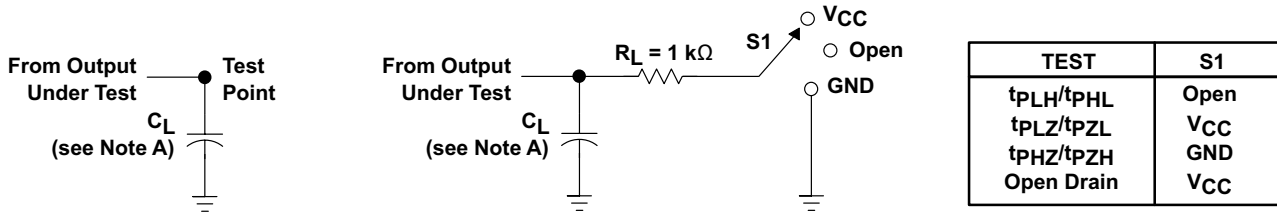
(1) Characteristics are for surface-mount packages only.

## OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

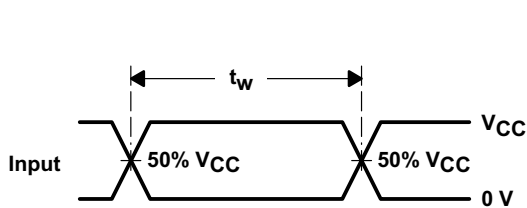
PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	9.5	pF

PARAMETER MEASUREMENT INFORMATION

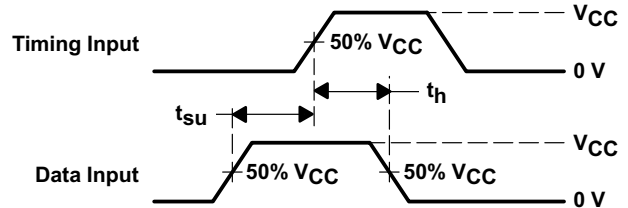


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

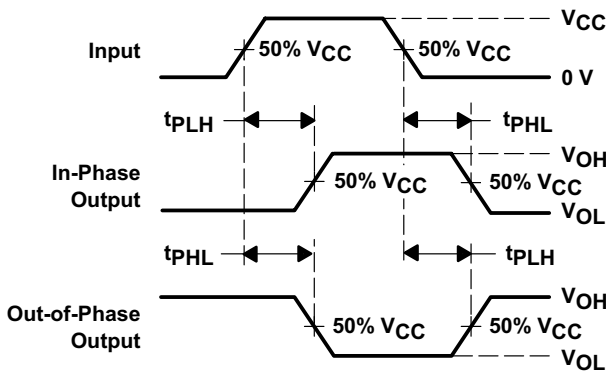
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



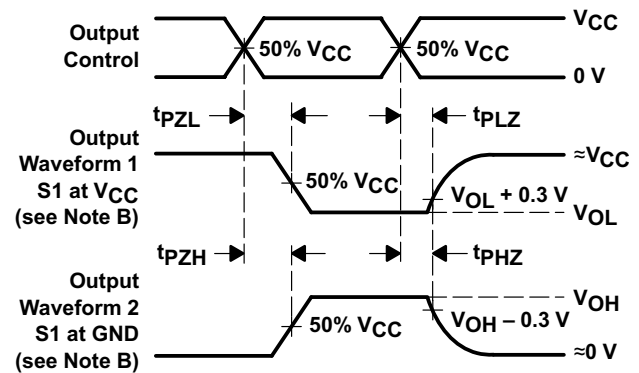
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## REVISION HISTORY

Changes from Revision J (December 1995) to Revision K	Page
• Changed document format from Quicksilver to DocZone. ....	1
• Extended operating temperature range to 125°C .....	2

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9686801Q2A SNJ54AHC 125FK	<a href="#">Samples</a>
5962-9686801QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686801QC A SNJ54AHC125J	<a href="#">Samples</a>
5962-9686801QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686801QD A SNJ54AHC125W	<a href="#">Samples</a>
SN74AHC125D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	<a href="#">Samples</a>
SN74AHC125DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 125		
SN74AHC125DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	<a href="#">Samples</a>
SN74AHC125DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	<a href="#">Samples</a>
SN74AHC125DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	<a href="#">Samples</a>
SN74AHC125DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	<a href="#">Samples</a>
SN74AHC125DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	<a href="#">Samples</a>
SN74AHC125DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	<a href="#">Samples</a>
SN74AHC125N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC125N	<a href="#">Samples</a>
SN74AHC125NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC125N	<a href="#">Samples</a>
SN74AHC125NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	<a href="#">Samples</a>
SN74AHC125NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	<a href="#">Samples</a>
SN74AHC125PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC125PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	<a href="#">Samples</a>
SN74AHC125PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
SN74AHC125PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	<a href="#">Samples</a>
SN74AHC125PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	<a href="#">Samples</a>
SN74AHC125PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	<a href="#">Samples</a>
SN74AHC125RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA125	<a href="#">Samples</a>
SN74AHC125RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA125	<a href="#">Samples</a>
SNJ54AHC125FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9686801Q2A SNJ54AHC 125FK	<a href="#">Samples</a>
SNJ54AHC125J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686801QC A SNJ54AHC125J	<a href="#">Samples</a>
SNJ54AHC125W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686801QD A SNJ54AHC125W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.



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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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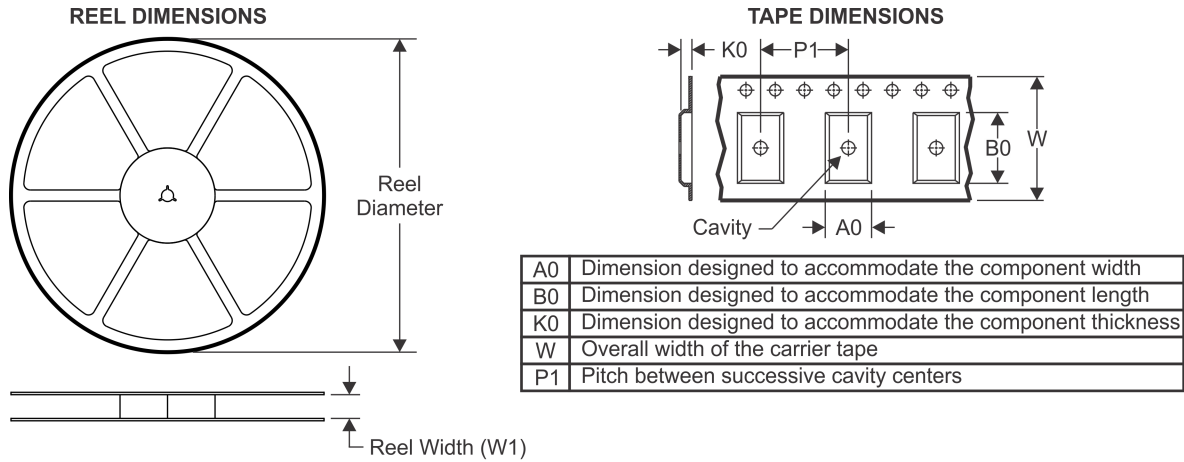
**OTHER QUALIFIED VERSIONS OF SN54AHC125, SN74AHC125 :**

- Catalog: [SN74AHC125](#)
- Automotive: [SN74AHC125-Q1](#), [SN74AHC125-Q1](#)
- Enhanced Product: [SN74AHC125-EP](#), [SN74AHC125-EP](#)
- Military: [SN54AHC125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC125DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC125DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AHC125DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74AHC125DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74AHC125DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AHC125NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AHC125PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AHC125RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



RGY (S-PVQFN-N14)

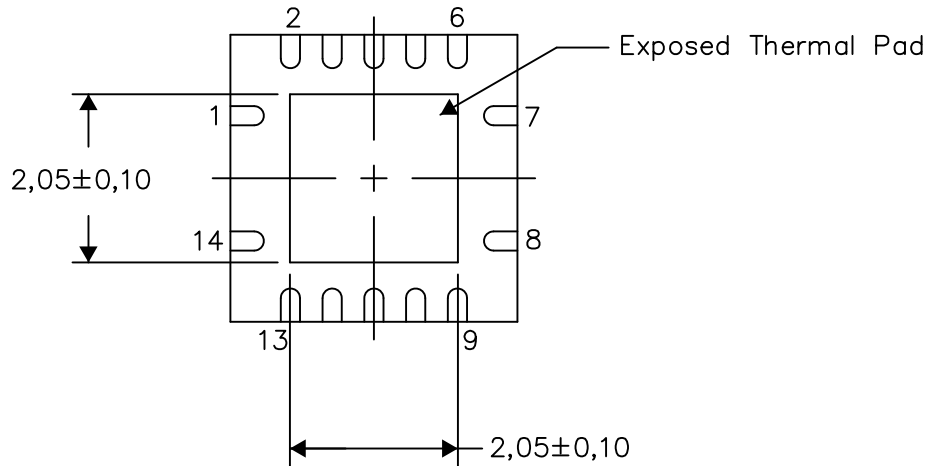
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

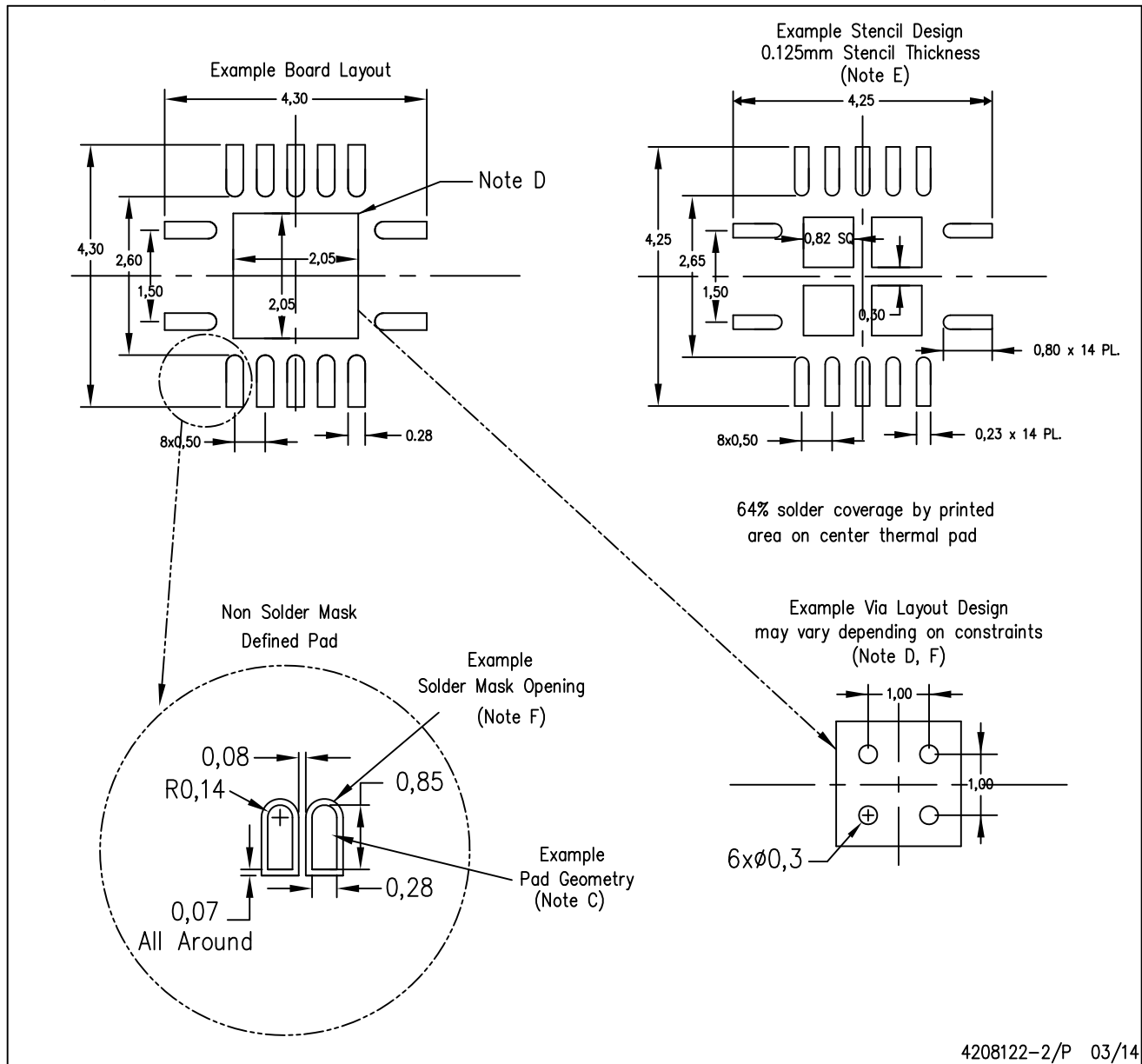
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

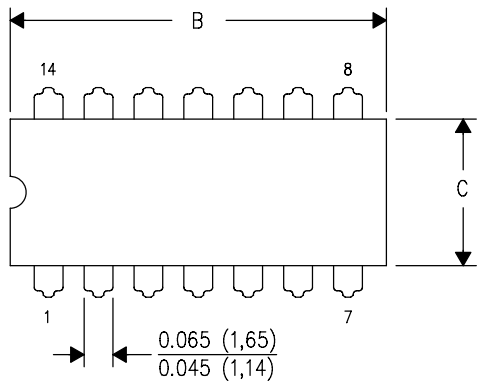


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

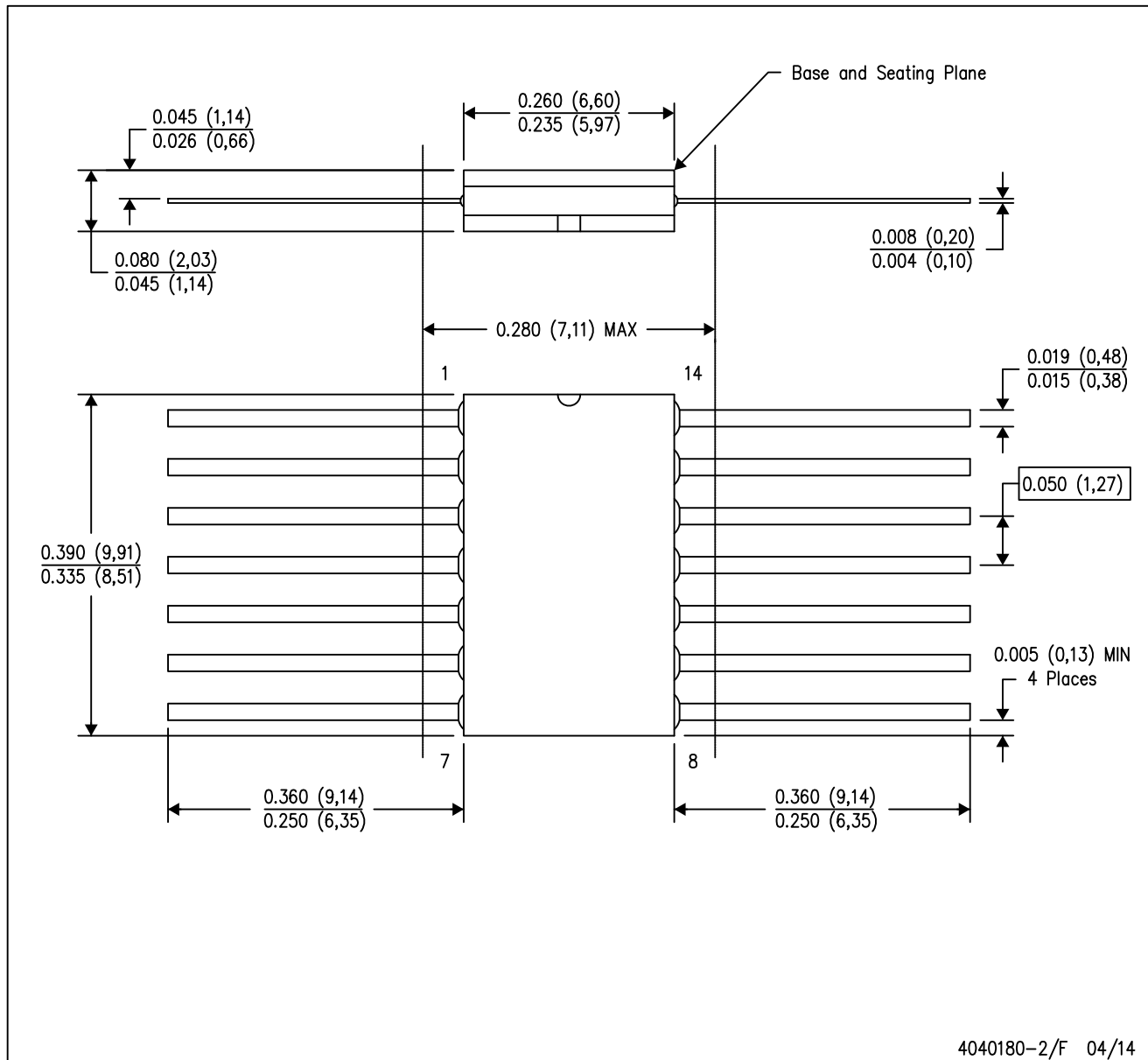


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

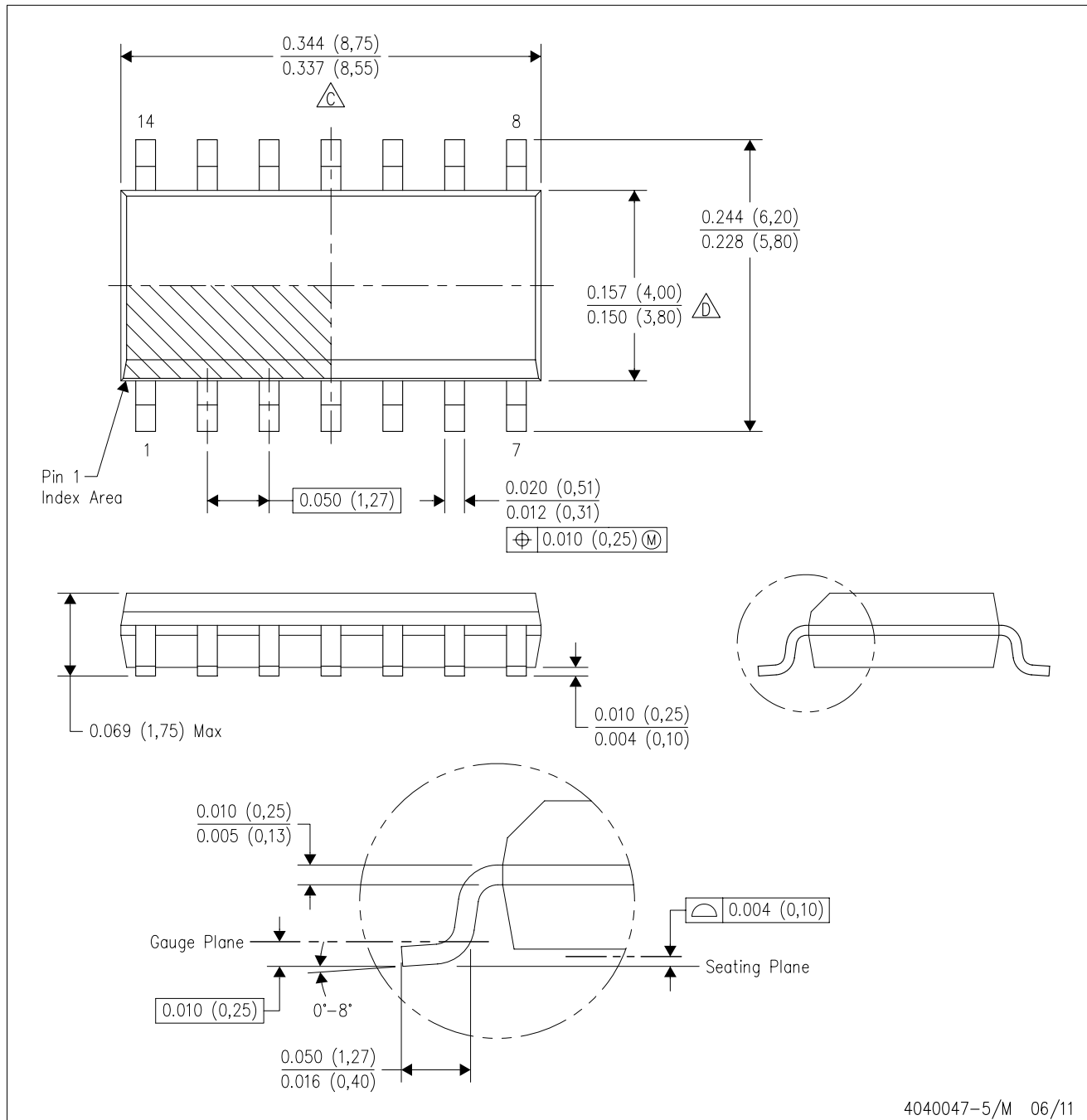


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

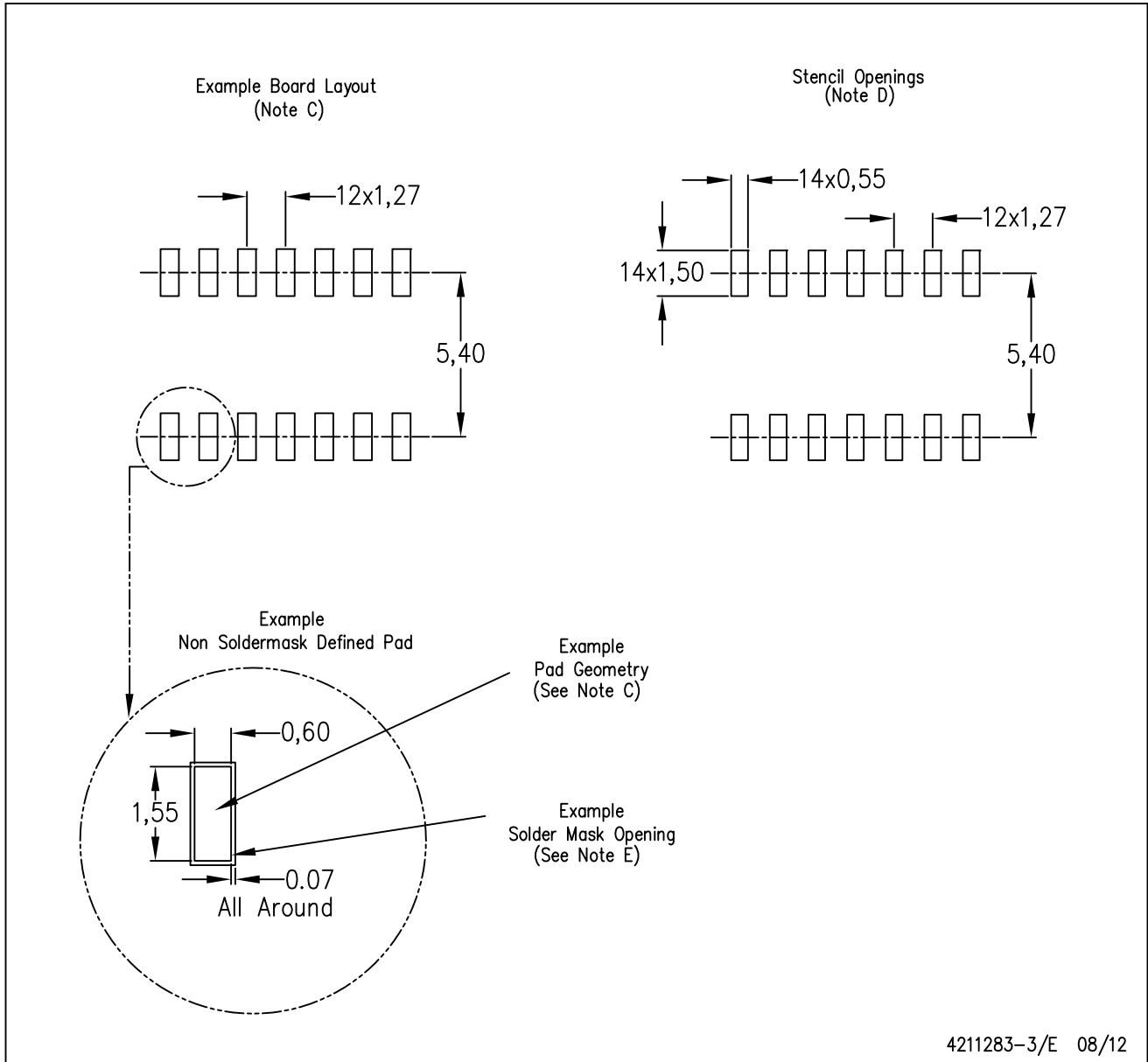
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

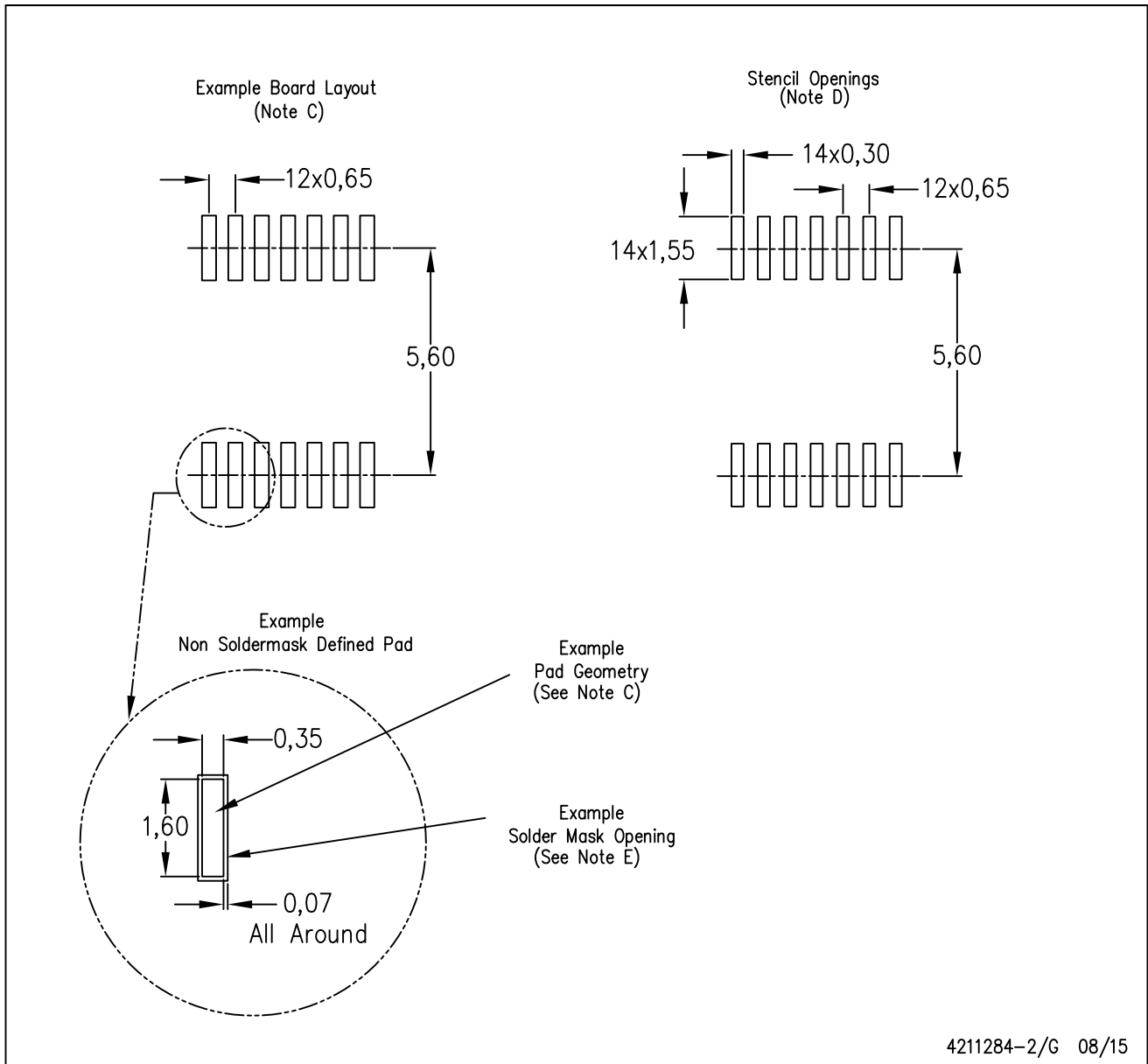


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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