



FDMC8010

N-Channel PowerTrench[®] MOSFET 30 V, 75 A, 1.3 mΩ

Features

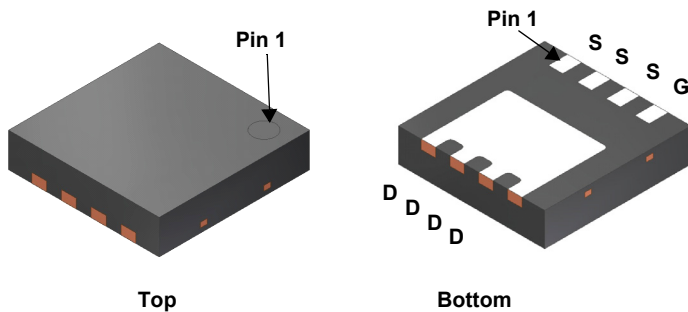
- Max $r_{DS(on)}$ = 1.3 mΩ at $V_{GS} = 10$ V, $I_D = 30$ A
- Max $r_{DS(on)}$ = 1.8 mΩ at $V_{GS} = 4.5$ V, $I_D = 25$ A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that has been especially tailored to minimize the on-state resistance. This device is well suited for applications where ultra low $r_{DS(on)}$ is required in small spaces such as High performance VRM, POL and Oring functions.

Applications

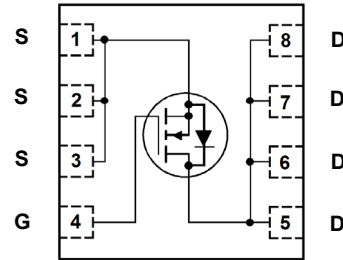
- DC - DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching
- Oring FET



Top

Bottom

Power 33



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|---|-------------|-------|
| V_{DS} | Drain to Source Voltage | 30 | V |
| V_{GS} | Gate to Source Voltage (Note 4) | ±20 | V |
| I_D | Drain Current -Continuous (Package limited) $T_C = 25$ °C | 75 | A |
| | -Continuous (Silicon limited) $T_C = 25$ °C | 166 | |
| | -Continuous $T_A = 25$ °C (Note 1a) | 30 | |
| | -Pulsed | 120 | |
| E_{AS} | Single Pulse Avalanche Energy (Note 3) | 153 | mJ |
| P_D | Power Dissipation $T_C = 25$ °C | 54 | W |
| | Power Dissipation $T_A = 25$ °C (Note 1a) | 2.4 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|-----------------|---|-----|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 2.3 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 53 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|----------|----------|-----------|------------|------------|
| FDMC8010 | FDMC8010 | Power 33 | 13 " | 12 mm | 3000 units |

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|--|----|----|-----|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$ | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 1\text{ mA}$, referenced to 25°C | | 15 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$ | | | 100 | nA |

On Characteristics

| | | | | | | |
|--|--|--|-----|-----|-----|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 1\text{ mA}$ | 1.2 | 1.5 | 2.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 1\text{ mA}$, referenced to 25°C | | -5 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10\text{ V}, I_D = 30\text{ A}$ | | 0.9 | 1.3 | m Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$ | | 1.3 | 1.8 | |
| | | $V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125^\circ\text{C}$ | | 1.3 | 2 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{ V}, I_D = 30\text{ A}$ | | 188 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|-----|------|------|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$ | | 4405 | 5860 | pF |
| C_{oss} | Output Capacitance | | | 1570 | 2090 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 167 | 250 | pF |
| R_g | Gate Resistance | | 0.1 | 0.5 | 1.25 | Ω |

Switching Characteristics

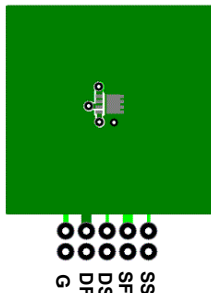
| | | | | | | | |
|--------------|-------------------------------|---|--|-----|-----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 15\text{ V}, I_D = 30\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$ | | 15 | 27 | ns | |
| t_r | Rise Time | | | 7.5 | 15 | ns | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 40 | 64 | ns | |
| t_f | Fall Time | | | 5.3 | 11 | ns | |
| Q_g | Total Gate Charge | | $V_{GS} = 0\text{ V to }10\text{ V}$ | | 67 | 94 | nC |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V to }4.5\text{ V}$ | $V_{DD} = 15\text{ V},$ $I_D = 30\text{ A}$ | | 32 | 45 | nC |
| Q_{gs} | Gate to Source Charge | | | | 10 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | | 9.5 | | nC |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|---------------------------------------|---|--|-----|-----|----|
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2) | | 0.6 | 1.2 | V |
| | | $V_{GS} = 0\text{ V}, I_S = 30\text{ A}$ (Note 2) | | 0.7 | 1.2 | |
| t_{rr} | Reverse Recovery Time | $I_F = 30\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | | 49 | 78 | ns |
| Q_{rr} | Reverse Recovery Charge | | | 29 | 46 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.

3. E_{AS} of 153 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 32\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 47\text{ A}$.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

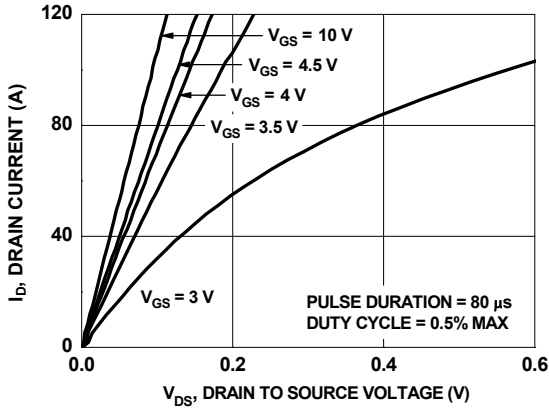


Figure 1. On Region Characteristics

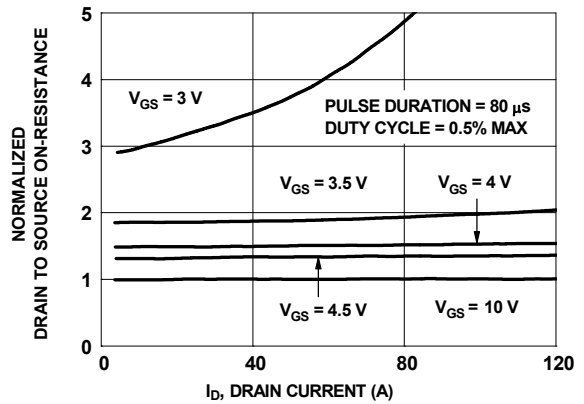


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

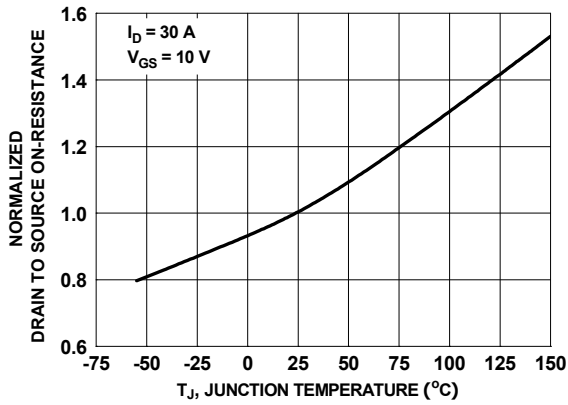


Figure 3. Normalized On Resistance vs Junction Temperature

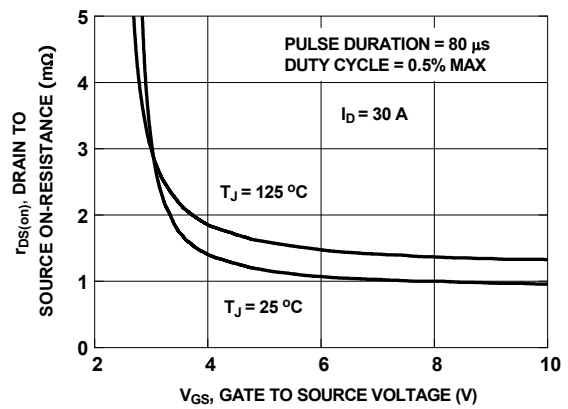


Figure 4. On-Resistance vs Gate to Source Voltage

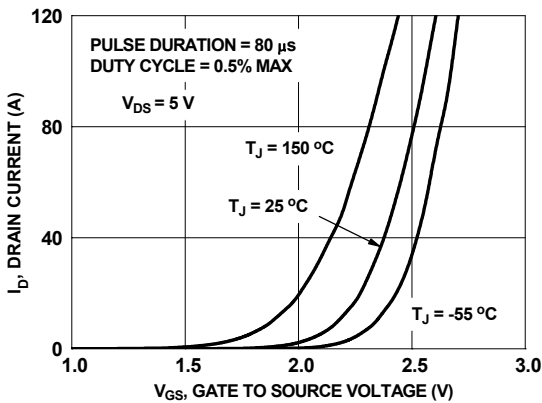


Figure 5. Transfer Characteristics

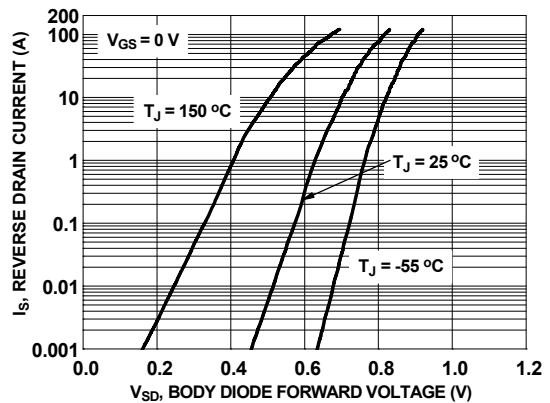


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

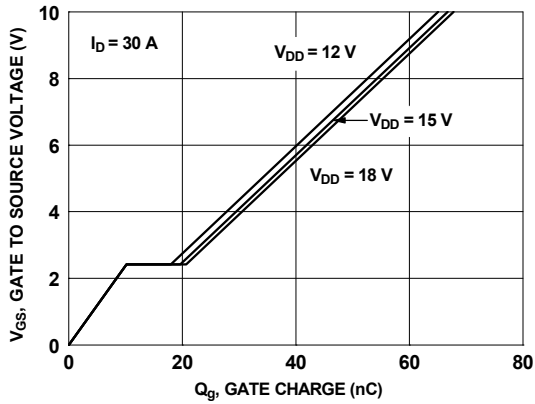


Figure 7. Gate Charge Characteristics

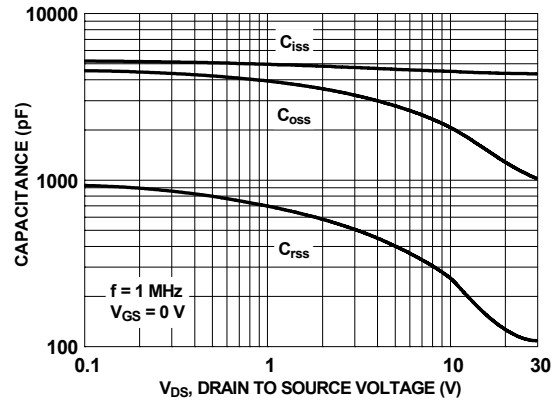


Figure 8. Capacitance vs Drain to Source Voltage

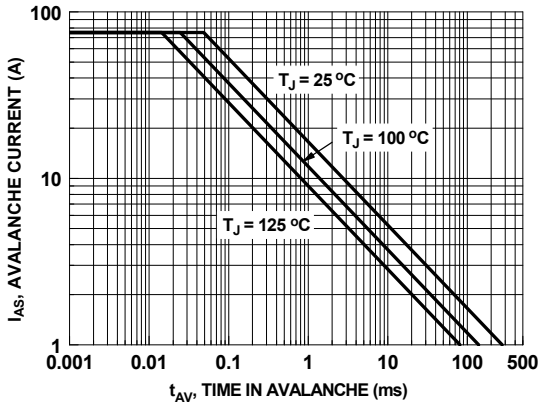


Figure 9. Unclamped Inductive Switching Capability

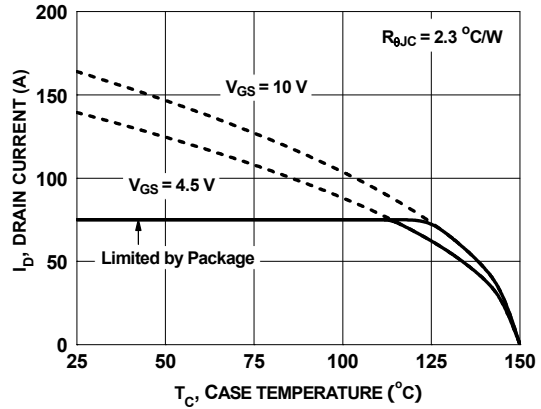


Figure 10. Maximum Continuous Drain Current vs Case Temperature

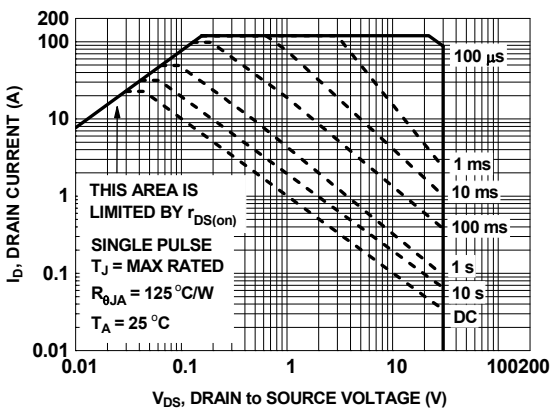


Figure 11. Forward Bias Safe Operating Area

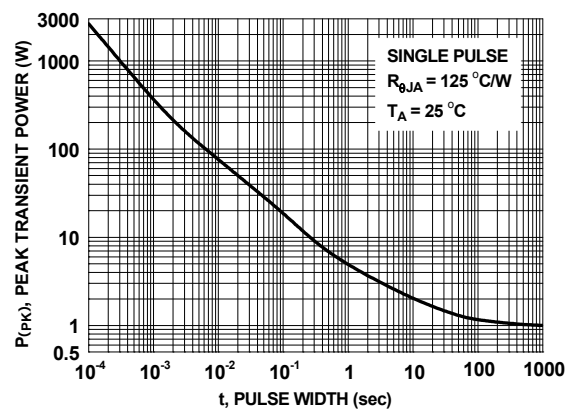


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

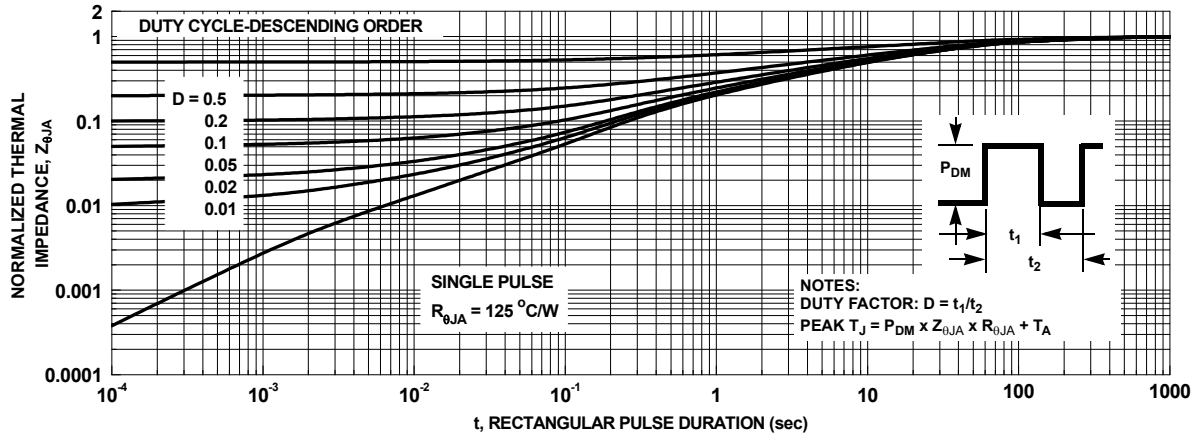
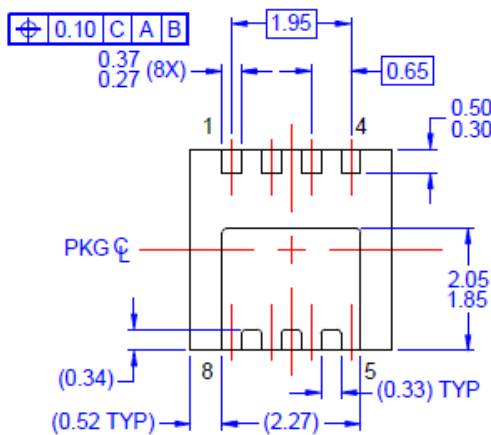
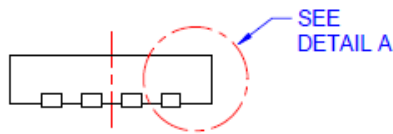
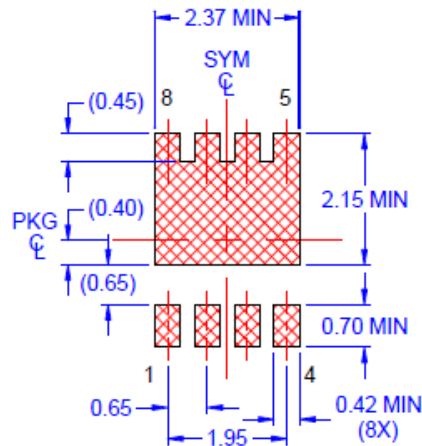
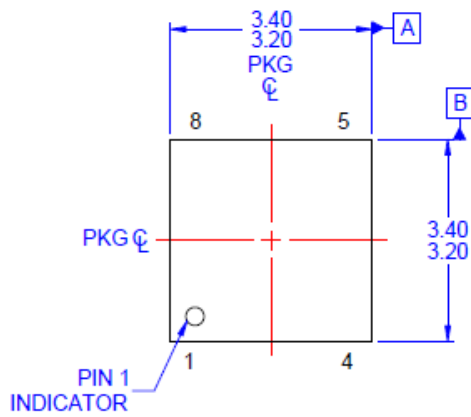


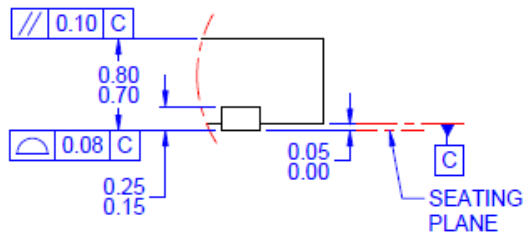
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08HREV1



DETAIL A
SCALE: 2X


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| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
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| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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Rev. I72

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