19-3632; Rev 2; 3/07

EVALUATION KIT AVAILABLE

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

MAX5877

General Description

The MAX5877 is an advanced 14-bit, 250Msps, dual digital-to-analog converter (DAC). This DAC meets the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from +3.3V and +1.8V supplies, this dual DAC offers exceptional dynamic performance such as 75dBc spurious-free dynamic range (SFDR) at f_{OUT} = 16MHz and supports update rates of 250Msps, with a power dissipation of only 287mW.

The MAX5877 utilizes a current-steering architecture that supports a 2mA to 20mA full-scale output current range, and allows a 0.1V_{P-P} to 1V_{P-P} differential output voltage swing. The device features an integrated +1.2V bandgap reference and control amplifier to ensure high-accuracy and low-noise performance. A separate reference input (REFIO) allows for the use of an external reference source for optimum flexibility and improved gain accuracy.

The clock inputs of the MAX5877 accept both LVDS and LVPECL-compatible voltage levels. The device features an interleaved data input that allows a single LVDS bus to support both DACs. The MAX5877 is available in a 68-pin QFN package with an exposed pad (EP) and is specified for the extended temperature range (-40°C to +85°C).

Refer to the MAX5876 and MAX5878 data sheets for pin-compatible 12-bit and 16-bit versions of the MAX5877, respectively. Refer to the MAX5874 data sheet for a CMOS-compatible version of the MAX5877.

Applications

Base Stations: Single/Multicarrier UMTS, CDMA, GSM

Communications: Fixed Broadband Wireless Access, Point-to-Point Microwave

Direct Digital Synthesis (DDS)

Cable Modem Termination Systems (CMTS)

Automated Test Equipment (ATE)

Instrumentation

Selector Guide

PART	RESOLUTION (BITS)	UPDATE RATE (Msps)	LOGIC INPUTS
MAX5873	12	200	CMOS
MAX5874	14	200	CMOS
MAX5875	16	200	CMOS
MAX5876	12	250	LVDS
MAX5877	14	250	LVDS
MAX5878	16	250	LVDS

Features

- **250Msps Output Update Rate**
- **Noise Spectral Density = -160dBFS/Hz at f_{OUT} = 16MHz**
- **Excellent SFDR and IMD Performance**
  - **SFDR = 75dBc at f_{OUT} = 16MHz (to Nyquist)**
  - **SFDR = 71dBc at f_{OUT} = 80MHz (to Nyquist)**
  - **IMD = -87dBc at f_{OUT} = 10MHz**
  - **IMD = -73dBc at f_{OUT} = 80MHz**
- **ACLR = 75dB at f_{OUT} = 61MHz**
- **2mA to 20mA Full-Scale Output Current**
- **LVDS-Compatible Digital and Clock Inputs**
- **On-Chip +1.20V Bandgap Reference**
- **Low 287mW Power Dissipation**
- **Compact 68-Pin QFN-EP Package (10mm x 10mm)**
- **Evaluation Kit Available (MAX5878EVKIT)**

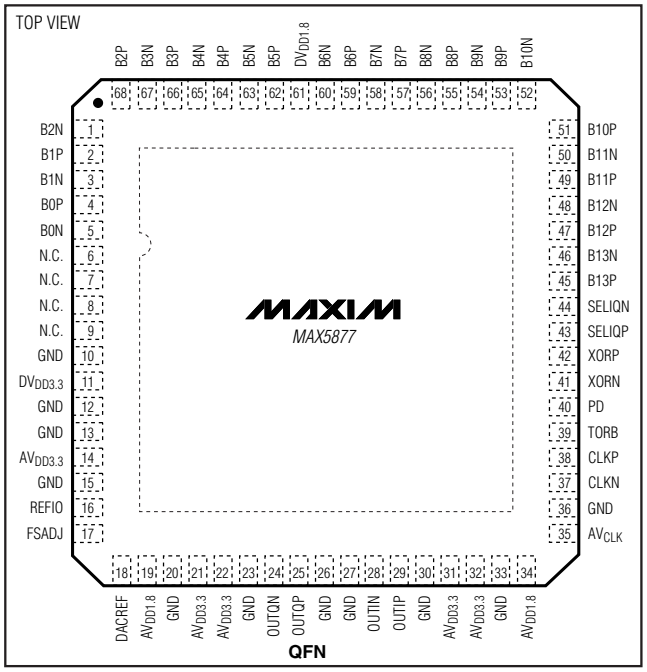
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5877EGK-D	-40°C to +85°C	68 QFN-EP*	G6800-4
MAX5877EGK+D	-40°C to +85°C	68 QFN-EP*	G6800-4

**EP = Exposed pad.*

+ = Lead-free package. D = Dry pack.

Pin Configuration



14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

ABSOLUTE MAXIMUM RATINGS

$AV_{DD1.8}$, $DV_{DD1.8}$ to GND, DACREF.....-0.3V to +2.16V
$AV_{DD3.3}$, $DV_{DD3.3}$, AV_{CLK} to GND, DACREF.....-0.3V to +3.9V
REFIO, FSADJ to
GND, DACREF.....-0.3V to ($AV_{DD3.3}$ + 0.3V)
OUTIP, OUTIN, OUTQP,
OUTQN to GND, DACREF.....-1V to ($AV_{DD3.3}$ + 0.3V)
CLKP, CLKN to GND, DACREF.....-0.3V to (AV_{CLK} + 0.3V)
B13P/B13N–B0P/B0N, XORN, XORP, SELIQN,
SELIQP to GND, DACREF .....-0.3V to ($DV_{DD1.8}$ + 0.3V)
TORB, PD to GND, DACREF .....-0.3V to ($DV_{DD3.3}$ + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
68-Pin QFN-EP
(derate 41.7mW/°C above +70°C) (Note 1).....3333.3mW
Thermal Resistance θ_{JA} (Note 1).....+24°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Thermal resistance based on a multilayer board with 4 x 4 via array in exposed paddle area.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = +3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = +1.8V, GND = 0, f_{CLK} = 2 x f_{DAC}, external reference V_{REFIO} = +1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution					14		Bits
Integral Nonlinearity	INL	Measured differentially			±0.5		LSB
Differential Nonlinearity	DNL	Measured differentially			±0.2		LSB
Offset Error	OS			-0.025	±0.001	+0.025	%FS
Offset-Drift Tempco					±10		ppm/°C
Full-Scale Gain Error	GE_{FS}	External reference		-4.6	-0.6	+4.6	%FS
Gain-Drift Tempco		Internal reference			±100		ppm/°C
		External reference			±50		
Full-Scale Output Current	I_{OUTFS}	(Note 3)		2		20	mA
Output Compliance		Single-ended		-0.5		+1.1	V
Output Resistance	R_{OUT}				1		MΩ
Output Capacitance	C_{OUT}				5		pF
DYNAMIC PERFORMANCE							
Clock Frequency	f_{CLK}			2		500	MHz
Output Update Rate	f_{DAC}	f_{DAC} = f_{CLK} / 2		1		250	Msps
Noise Spectral Density		f_{DAC} = 150MHz	f_{OUT} = 16MHz, -12dBFS		-160		dBFS/Hz
		f_{DAC} = 250MHz	f_{OUT} = 80MHz, -12dBFS		-157		

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = +3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = +1.8V, GND = 0, f_{CLK} = 2 x f_{DAC}, external reference V_{REFIO} = +1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{DAC} = 100MHz	f_{OUT} = 1MHz, 0dBFS		98		dBc
			f_{OUT} = 1MHz, -6dBFS		86		
			f_{OUT} = 1MHz, -12dBFS		78		
			f_{OUT} = 10MHz, -12dBFS		77		
			f_{OUT} = 30MHz, -12dBFS		78		
		f_{DAC} = 200MHz	f_{OUT} = 10MHz, -12dBFS		75		
			f_{OUT} = 16MHz, -12dBFS	66	75		
			f_{OUT} = 50MHz, -12dBFS		74		
			f_{OUT} = 80MHz, -12dBFS		71		
		f_{DAC} = 250MHz	f_{OUT} = 10MHz, -12dBFS		74		
			f_{OUT} = 50MHz, -12dBFS		72		
			f_{OUT} = 80MHz, -12dBFS		71		
			f_{OUT} = 100MHz, -12dBFS		68		
Spurious-Free Dynamic Range, 25MHz Bandwidth	SFDR	f_{DAC} = 150MHz	f_{OUT} = 16MHz, -12dBFS		80		dBc
Two-Tone IMD	TTIMD	f_{DAC} = 100MHz	f_{OUT1} = 9MHz, -7dBFS; f_{OUT2} = 10MHz, -7dBFS		-87		dBc
		f_{DAC} = 200MHz	f_{OUT1} = 79MHz, -7dBFS; f_{OUT2} = 80MHz, -7dBFS		-73		
Four-Tone IMD, 1MHz Frequency Spacing, GSM Model	FTIMD	f_{DAC} = 150MHz	f_{OUT} = 16MHz, -12dBFS		-94		dBc
Adjacent Channel Leakage Power Ratio 3.84MHz Bandwidth, W-CDMA Model	ACLR	f_{DAC} = 184.32MHz	f_{OUT} = 61.44MHz		75		dB
Output Bandwidth	BW_{-1dB}	(Note 4)			240		MHz
INTER-DAC CHARACTERISTICS							
Gain Matching	ΔGain	f_{OUT} = DC - 80MHz			±0.2		dB
		f_{OUT} = DC		-0.25	+0.01	+0.25	
Gain-Matching Tempco	ΔGain/°C				±20		ppm/°C
Phase Matching	ΔPhase	f_{OUT} = 60MHz			±0.25		Degrees
Phase-Matching Tempco	ΔPhase/°C	f_{OUT} = 60MHz			±0.002		Degrees/°C
Channel-to-Channel Crosstalk		f_{DAC} = 200Msps, f_{OUT} = 50MHz, 0dBFS			90		dB
REFERENCE							
Internal Reference Voltage Range	V_{REFIO}			1.14	1.2	1.26	V

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = +3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = +1.8V, GND = 0, f_{CLK} = 2 x f_{DAC}, external reference V_{REFIO} = +1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Input Compliance Range	$V_{REFIOCR}$		0.125		1.260	V
Reference Input Resistance	R_{REFIO}			10		kΩ
Reference Voltage Drift	TCO_{REF}			±25		ppm/°C
ANALOG OUTPUT TIMING (See Figure 4)						
Output Fall Time	t_{FALL}	90% to 10% (Note 5)		0.7		ns
Output Rise Time	t_{RISE}	10% to 90% (Note 5)		0.7		ns
Output-Voltage Settling Time	t_{SETTLE}	Output settles to 0.025% FS (Note 5)		14		ns
Output Propagation Delay	t_{PD}	Excluding data latency (Note 5)		1.1		ns
Glitch Impulse		Measured differentially		1		pV•s
Output Noise	n_{OUT}	I_{OUTFS} = 2mA		30		pA/√Hz
		I_{OUTFS} = 20mA		30		
TIMING CHARACTERISTICS						
Data to Clock Setup Time	t_{SETUP}	Referenced to rising edge of clock (Note 6)	-1.2			ns
Data to Clock Hold Time	t_{HOLD}	Referenced to rising edge of clock (Note 6)	2.0			ns
Data Latency		Latency to I output		9		Clock Cycles
		Latency to Q output		8		
Minimum Clock Pulse-Width High	t_{CH}	CLKP, CLKN		0.9		ns
Minimum Clock Pulse-Width Low	t_{CL}	CLKP, CLKN		0.9		ns
LVDS LOGIC INPUTS (B13P/B13N–B0P/B0N, XORN, XORP, SELIQN, SELIQP)						
Differential Input-Logic High	V_{IH}				100	mV
Differential Input-Logic Low	V_{IL}		-100			mV
Common-Mode Voltage Range	V_{CMR}		1.125		1.375	V
Differential Input Resistance	R_{IN}	(Note 7)		110		Ω
Input Capacitance	C_{IN}			2.5		pF
CMOS LOGIC INPUTS (PD, TORB)						
Input-Logic High	V_{IH}		0.7 x $DV_{DD3.3}$			V
Input-Logic Low	V_{IL}				0.3 x $DV_{DD3.3}$	V
Input Leakage Current	I_{IN}		-20	1	+20	µA
PD, TORB Internal Pulldown Resistance		V_{PD} = V_{TORB} = 3.3V		1.5		MΩ
Input Capacitance	C_{IN}			2.5		pF
CLOCK INPUTS (CLKP, CLKN)						
Differential Input Voltage Swing		Sine wave		> 1.5		V_{P-P}
		Square wave		> 0.5		

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = +3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = +1.8V, GND = 0, f_{CLK} = 2 x f_{DAC}, external reference V_{REFIO} = +1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Slew Rate	SR_{CLK}	(Note 8)		>100		V/µs
External Common-Mode Voltage Range	V_{COM}			AV_{CLK} / 2 ±0.3		V
Input Resistance	R_{CLK}			5		kΩ
Input Capacitance	C_{CLK}			2.5		pF
POWER SUPPLIES						
Analog Supply Voltage Range	$AV_{DD3.3}$		3.135	3.3	3.465	V
	$AV_{DD1.8}$		1.710	1.8	1.890	
Digital Supply Voltage Range	$DV_{DD3.3}$		3.135	3.3	3.465	V
	$DV_{DD1.8}$		1.710	1.8	1.890	
Clock Supply Voltage Range	AV_{CLK}		3.135	3.3	3.465	V
Analog Supply Current	$I_{AVDD3.3}$ + I_{AVCLK}	f_{DAC} = 250Msps, f_{OUT} = 16MHz		52	58	mA
		Power-down		1		µA
	$I_{AVDD1.8}$	f_{DAC} = 250Msps, f_{OUT} = 16MHz		30	36	mA
		Power-down		1		µA
Digital Supply Current	$I_{DVDD3.3}$	f_{DAC} = 250Msps, f_{OUT} = 16MHz		0.2	1	mA
		Power-down		1		µA
	$I_{DVDD1.8}$	f_{DAC} = 250Msps, f_{OUT} = 16MHz		34	40	mA
		Power-down		4		µA
Power Dissipation	P_{DISS}	f_{DAC} = 250Msps, f_{OUT} = 16MHz		287	331	mW
		Power-down		16		µW
Power-Supply Rejection Ratio	PSRR	$AV_{DD3.3}$ = AV_{CLK} = $DV_{DD3.3}$ = +3.3V ±5% (Notes 8, 9)	-0.1		+0.1	%FS/V

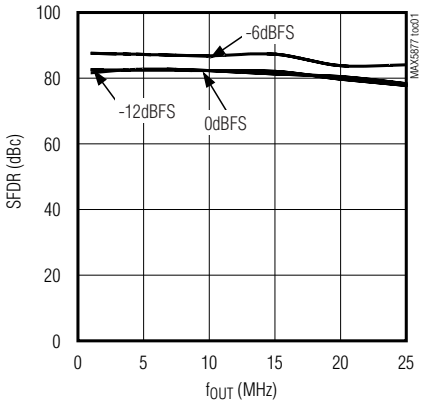
Note 2: Specifications at T_A ≥ +25°C are guaranteed by production testing. Specifications at T_A < +25°C are guaranteed by design.
Note 3: Nominal full-scale current I_{OUTFS} = 32 x I_{REF}.
Note 4: This parameter does not include update-rate-dependent effects of sin(x)/x filtering inherent in the MAX5877.
Note 5: Parameter measured single-ended into a 50Ω termination resistor.
Note 6: Not production tested. Guaranteed by design.
Note 7: No termination resistance between XORP and XORN.
Note 8: A differential clock input slew rate of > 100V/µs is required to achieve the specified dynamic performance.
Note 9: Parameter defined as the change in midscale output caused by a ±5% variation in the nominal supply voltage.

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

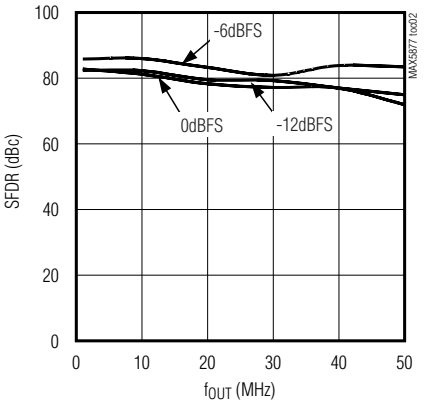
Typical Operating Characteristics

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = +3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = +1.8V, external reference, V_{REFIO} = +1.25V, R_L = 50Ω double-terminated, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.)

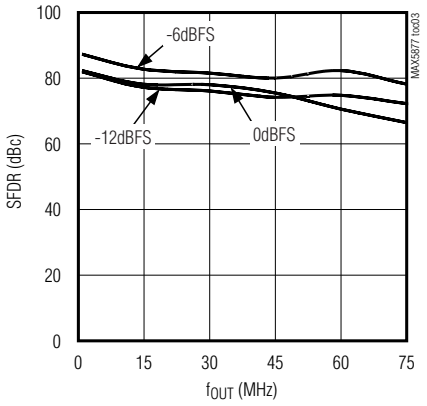
SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 50Msps)



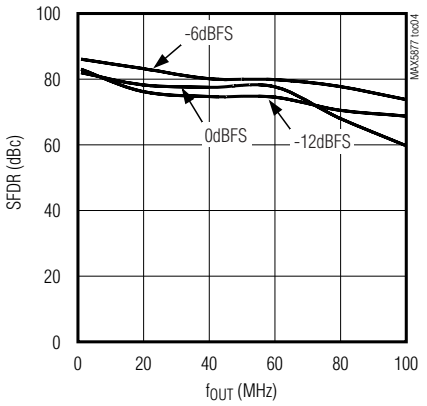
SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 100Msps)



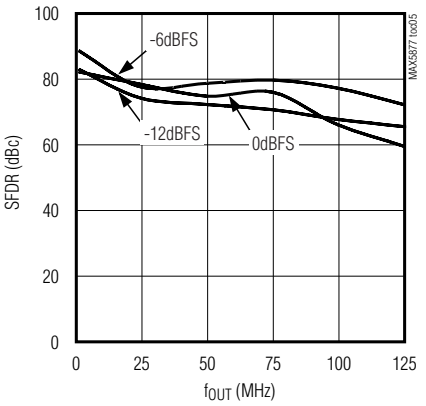
SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 150Msps)



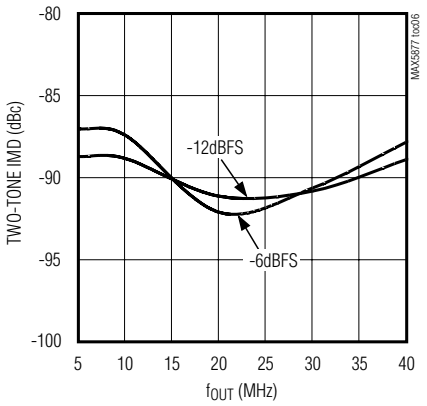
SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 200Msps)



SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 250Msps)



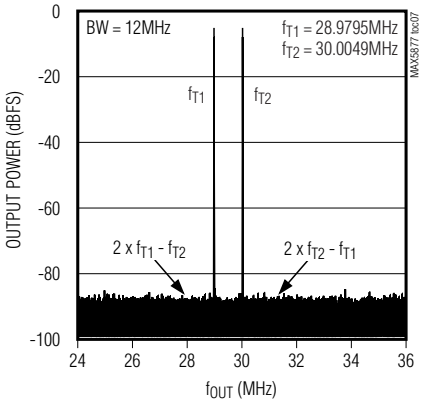
TWO-TONE IMD vs. OUTPUT FREQUENCY (1MHz CARRIER SPACING, f_{DAC} = 100Msps)



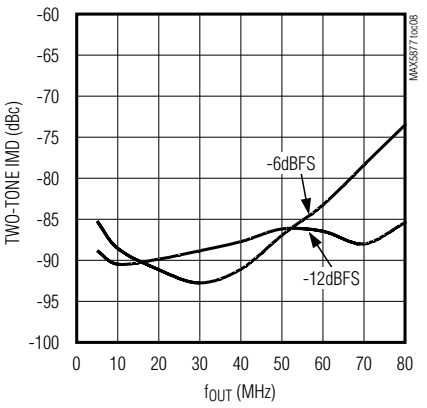
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = +3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = +1.8V, external reference, V_{REFIO} = +1.25V, R_L = 50Ω double-terminated, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.)

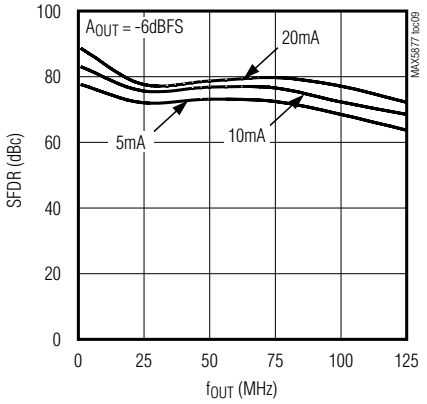
TWO-TONE INTERMODULATION DISTORTION (f_{DAC} = 100Msps)



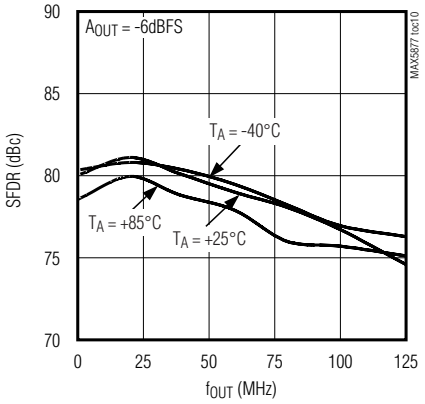
TWO-TONE IMD vs. OUTPUT FREQUENCY (1MHz CARRIER SPACING, f_{DAC} = 200Msps)



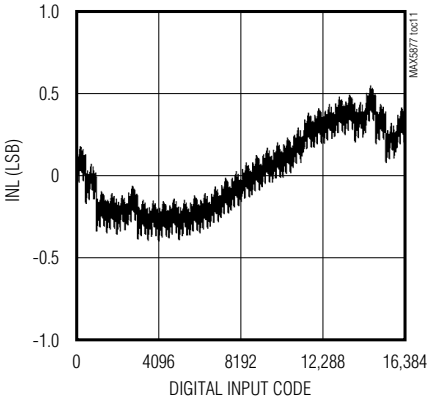
SFDR vs. FULL-SCALE OUTPUT CURRENT (f_{DAC} = 250Msps)



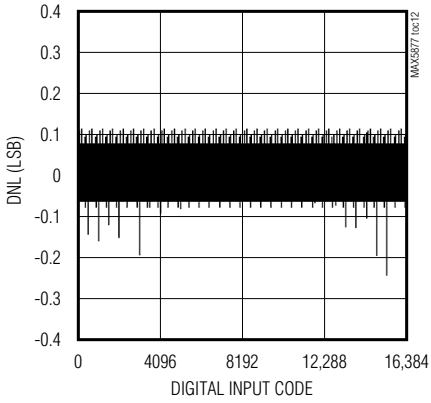
SFDR vs. TEMPERATURE (f_{DAC} = 250Msps)



INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE

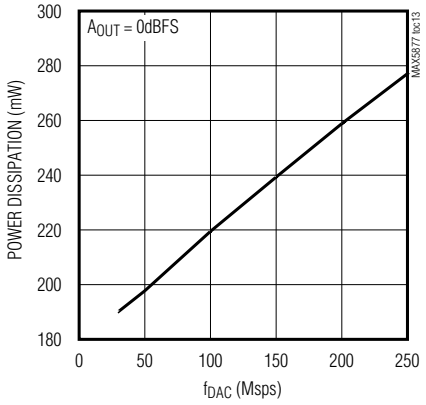


14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

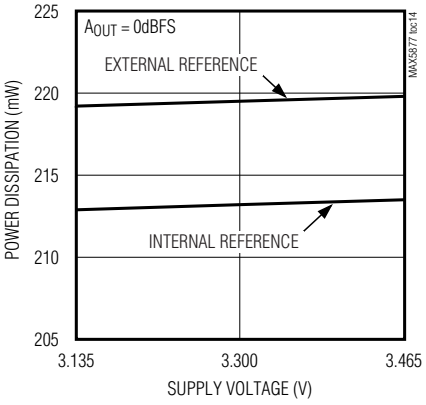
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = +3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = +1.8V, external reference, V_{REFIO} = +1.25V, R_L = 50Ω double-terminated, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.)

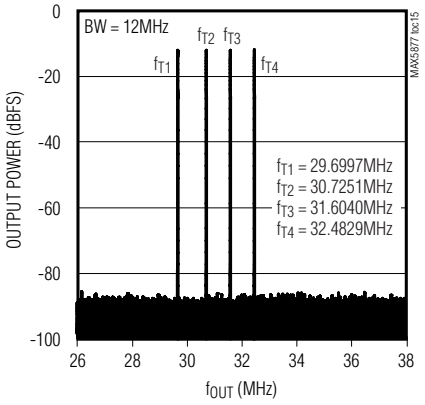
POWER DISSIPATION vs. DAC UPDATE RATE (f_{OUT} = 10MHz)



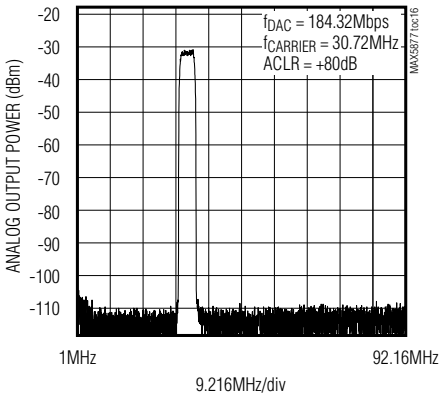
POWER DISSIPATION vs. SUPPLY VOLTAGE (f_{DAC} = 100Msps, f_{OUT} = 10MHz)



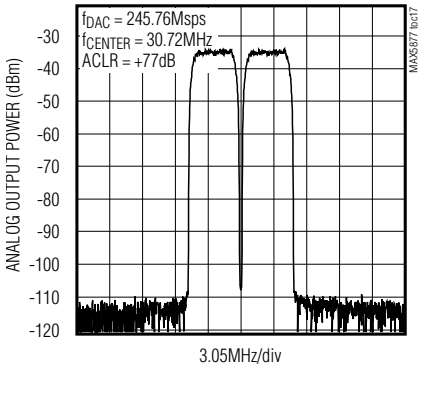
FOUR-TONE POWER RATIO PLOT (f_{DAC} = 150MHz)



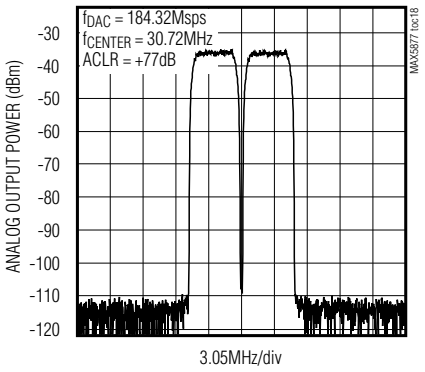
ACLR FOR WCDMA MODULATION, SINGLE-CARRIER ACLR



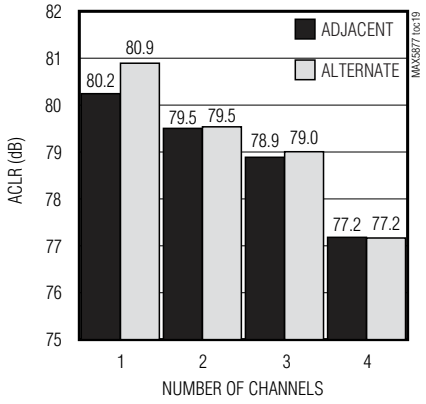
ACLR FOR WCDMA MODULATION TWO-CARRIER ACLR



ACLR FOR WCDMA MODULATION TWO-CARRIER ACLR



WCDMA BASEBAND ACLR (f_{DAC} = 245.76Msps)



Pin Description

PIN	NAME	FUNCTION
1	B2N	Complementary Data Bit 2
2	B1P	Data Bit 1
3	B1N	Complementary Data Bit 1
4	B0P	Data Bit 0 (LSB)
5	B0N	Complementary Data Bit 0 (LSB)
6–9	N.C.	No Connection. Leave floating or connect to GND.
10, 12, 13, 15, 20, 23, 26, 27, 30, 33, 36	GND	Ground
11	$DV_{DD3.3}$	Digital Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1µF capacitor to GND.
14, 21, 22, 31, 32	$AV_{DD3.3}$	Analog Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass each pin with a 0.1µF capacitor to GND.
16	REFIO	Reference I/O. Output of the internal 1.2V precision bandgap reference. Bypass with a 1µF capacitor to GND. REFIO can be driven with an external reference source. See Table 1.
17	FSADJ	Full-Scale Adjust Input. This input sets the full-scale output current of the DAC. For a 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. See Table 1.
18	DACREF	Current-Set Resistor Return Path. Internally connected to GND. **Do not use as an external ground connection.**
19, 34	$AV_{DD1.8}$	Analog Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass each pin with a 0.1µF capacitor to GND.
24	OUTQN	Complementary Q-DAC Output. Negative terminal for current output.
25	OUTQP	Q-DAC Output. Positive terminal for current output.
28	OUTIN	Complementary I-DAC Output. Negative terminal for current output.
29	OUTIP	I-DAC Output. Positive terminal for current output.
35	AV_{CLK}	Clock Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1µF capacitor to GND.
37	CLKN	Complementary Converter Clock Input. Negative input terminal for LVDS/LVPECL-compatible differential converter clock. Internally biased to AV_{CLK} / 2.
38	CLKP	Converter Clock Input. Positive input terminal for LVDS/LVPECL-compatible differential converter clock. Internally biased to AV_{CLK} / 2.
39	TORB	Two's-Complement/Binary Select Input. Set TORB to a CMOS-logic-high level to indicate a two's-complement input format. Set TORB to a CMOS-logic-low level to indicate an offset binary input format. TORB has an internal pulldown resistor.

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

Pin Description (continued)

PIN	NAME	FUNCTION
40	PD	Power-Down Input. Set PD to a CMOS-logic-high level to force the DAC into power-down mode. Set PD to a CMOS-logic-low level for normal operation. PD has an internal pulldown resistor.
41	XORN	Complementary LVDS DAC Exclusive-OR Select Input. Set XORN high and XORP low to allow the data stream to pass unchanged to the DAC input. Set XORN low and XORP high to invert the DAC input data. If unused, connect XORN to $DV_{DD1.8}$.
42	XORP	LVDS DAC Exclusive-OR Select Input. Set XORN high and XORP low to allow the data stream to pass unchanged to the DAC input. Set XORN low and XORP high to invert the DAC input data. If unused, connect XORP to GND.
43	SELIQP	LVDS DAC Select Input. Set SELIQN low and SELIQP high to direct data to the I-DAC outputs. Set SELIQP low and SELIQN high to direct data to the Q-DAC outputs.
44	SELIQN	Complementary LVDS DAC Select Input. Set SELIQN low and SELIQP high to direct data to the I-DAC outputs. Set SELIQP low and SELIQN high to direct data to the Q-DAC outputs.
45	B13P	Data Bit 13 (MSB)
46	B13N	Complementary Data Bit 13 (MSB)
47	B12P	Data Bit 12
48	B12N	Complementary Data Bit 12
49	B11P	Data Bit 11
50	B11N	Complementary Data Bit 11
51	B10P	Data Bit 10
52	B10N	Complementary Data Bit 10
53	B9P	Data Bit 9
54	B9N	Complementary Data Bit 9
55	B8P	Data Bit 8
56	B8N	Complementary Data Bit 8
57	B7P	Data Bit 7
58	B7N	Complementary Data Bit 7
59	B6P	Data Bit 6
60	B6N	Complementary Data Bit 6
61	$DV_{DD1.8}$	Digital Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass with a 0.1µF capacitor to GND.
62	B5P	Data Bit 5
63	B5N	Complementary Data Bit 5
64	B4P	Data Bit 4
65	B4N	Complementary Data Bit 4
66	B3P	Data Bit 3
67	B3N	Complementary Data Bit 3
68	B2P	Data Bit 2
—	EP	Exposed Pad. Must be connected to GND through a low-impedance path.

Detailed Description

Architecture

The MAX5877 high-performance, 14-bit, dual current-steering DAC (Figure 1) operates with DAC update rates up to 250Msps. The converter consists of input registers and a demultiplexer for single-port operation, followed by a current-steering array. During operation, the input data registers demultiplex the single-port data bus. The current-steering array generates differential full-scale currents in the 2mA to 20mA range. An internal current-switching network, in combination with external 50Ω termination resistors, converts the differential output currents into dual differential output voltages with a 0.1V to 1V peak-to-peak output voltage range. An integrated +1.2V bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale output range.

Reference Architecture and Operation

The MAX5877 supports operation with the internal +1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source. REFIO also serves as a reference output when the DAC operates in internal reference mode. For stable operation with the internal reference, decouple REFIO to GND with a 1µF capacitor. Due to its limited output drive capability, buffer REFIO with an external amplifier when driving large external loads.

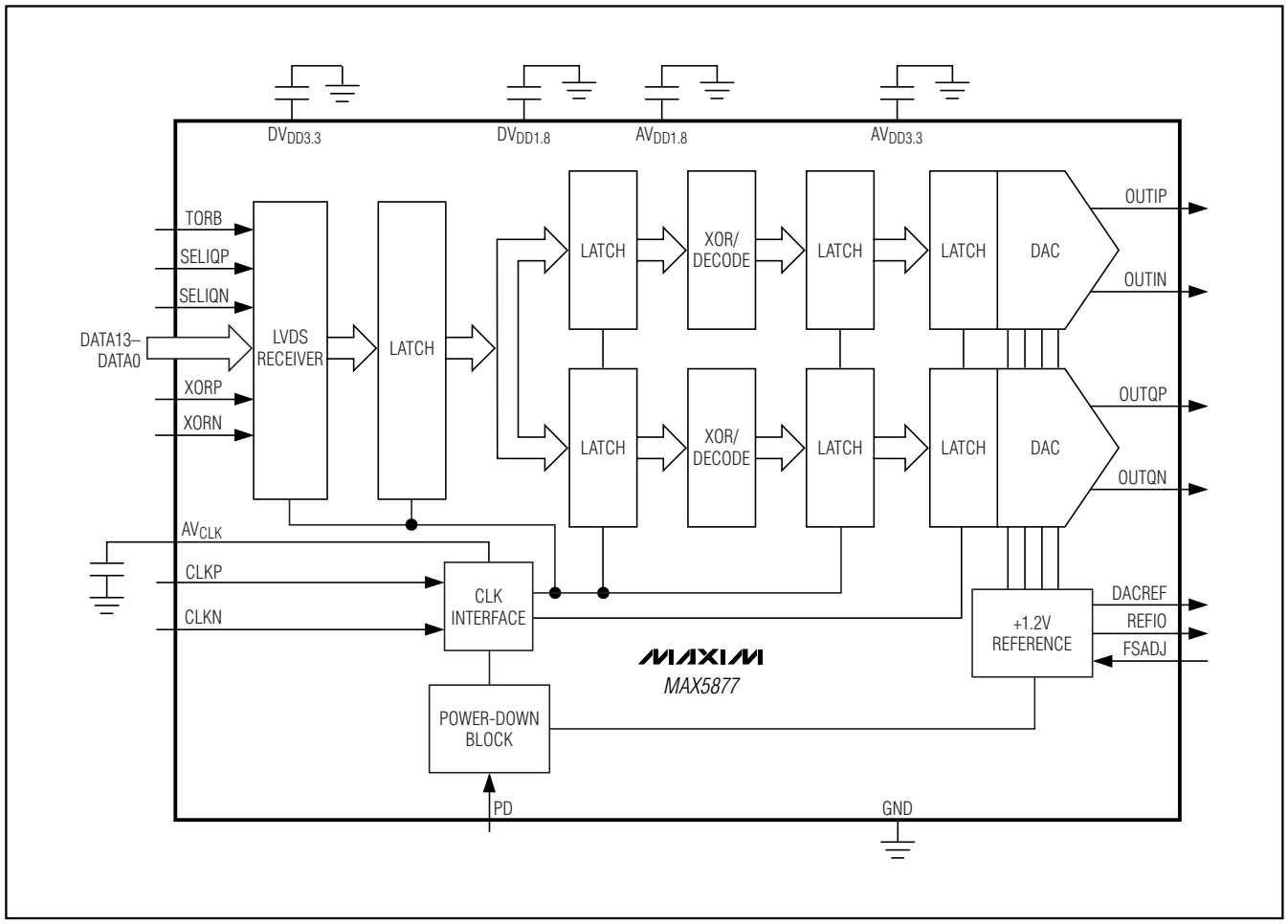


Figure 1. MAX5877 High-Performance, 14-Bit, Dual Current-Steering DAC

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

The MAX5877's reference circuit (Figure 2) employs a control amplifier to regulate the full-scale current I_{OUTFS} for the differential current outputs of the DAC. Calculate the full-scale output current as follows:

$$I_{OUTFS} = 32 \times \frac{V_{REFIO}}{R_{SET}} \times \left(1 - \frac{1}{2^{14}}\right)$$

where I_{OUTFS} is the full-scale output current of the DAC. R_{SET} (located between FSADJ and DACREF) determines the amplifier's full-scale output current for the DAC. See Table 1 for a matrix of different I_{OUTFS} and R_{SET} selections.

Analog Outputs (OUTIP, OUTIN, OUTQP, OUTQN)

Each MAX5877 DAC outputs two complementary currents (OUTIP/N, OUTQP/N) that operate in a single-ended or differential configuration. A load resistor converts these two output currents into complementary single-ended output voltages. A transformer or a differential amplifier configuration converts the differential voltage existing between OUTIP (OUTQP) and OUTIN (OUTQN) to a single-ended voltage. If not using a transformer, the recommended termination from the output is a 25Ω termination resistor to ground and a 50Ω resistor between the outputs.

To generate a single-ended output, select OUTIP (or OUTQP) as the output and connect OUTIN (or OUTQN) to GND. SFDR degrades with single-ended operation or increased output swing. Figure 3 displays a simplified diagram of the internal output structure of the MAX5877.

Clock Inputs (CLKP, CLKN)

The MAX5877 features flexible differential clock inputs (CLKP, CLKN) operating from a separate supply (AV_{CLK}) to achieve optimum jitter performance. Drive the differential clock inputs from a single-ended or a differential clock source. For single-ended operation, drive CLKP with a logic source and bypass CLKN to GND with a 0.1µF capacitor.

CLKP and CLKN are internally biased to AV_{CLK} / 2. This facilitates the AC-coupling of clock sources directly to the device without external resistors to define the DC level. The dynamic input resistance from CLKP and CLKN to ground is 5kΩ.

Table 1. I_{OUTFS} and R_{SET} Selection Matrix Based on a Typical +1.200V Reference Voltage

FULL-SCALE CURRENT I_{OUTFS} (mA)	R_{SET} (kΩ)	
	CALCULATED	1% EIA STD
2	19.2	19.1
5	7.68	7.5
10	3.84	3.83
15	2.56	2.55
20	1.92	1.91

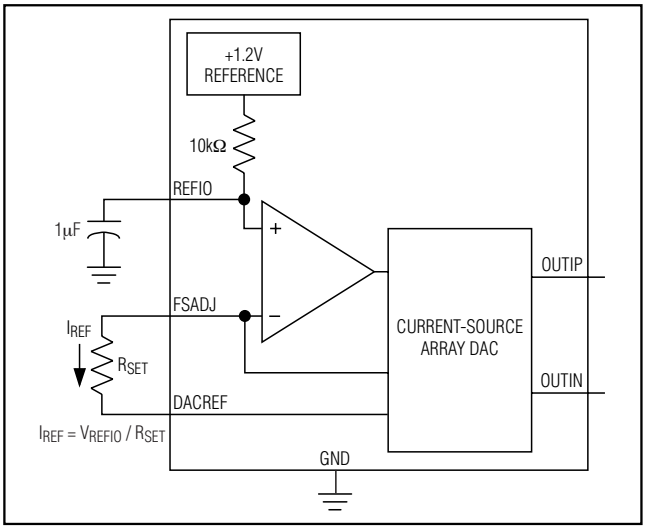


Figure 2. Reference Architecture, Internal Reference Configuration

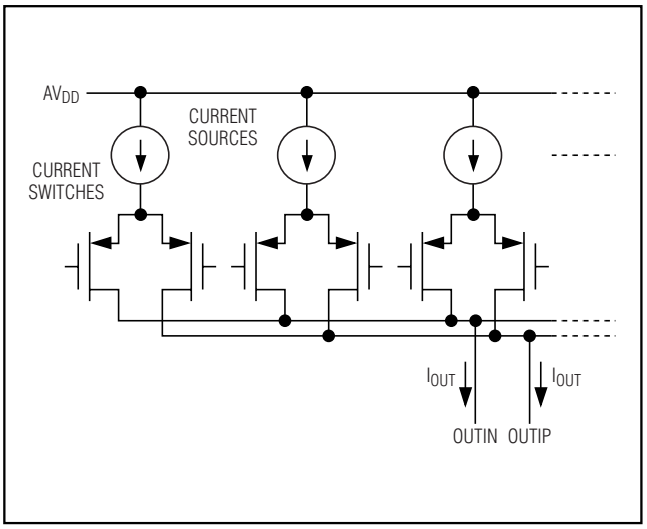


Figure 3. Simplified Analog Output Structure

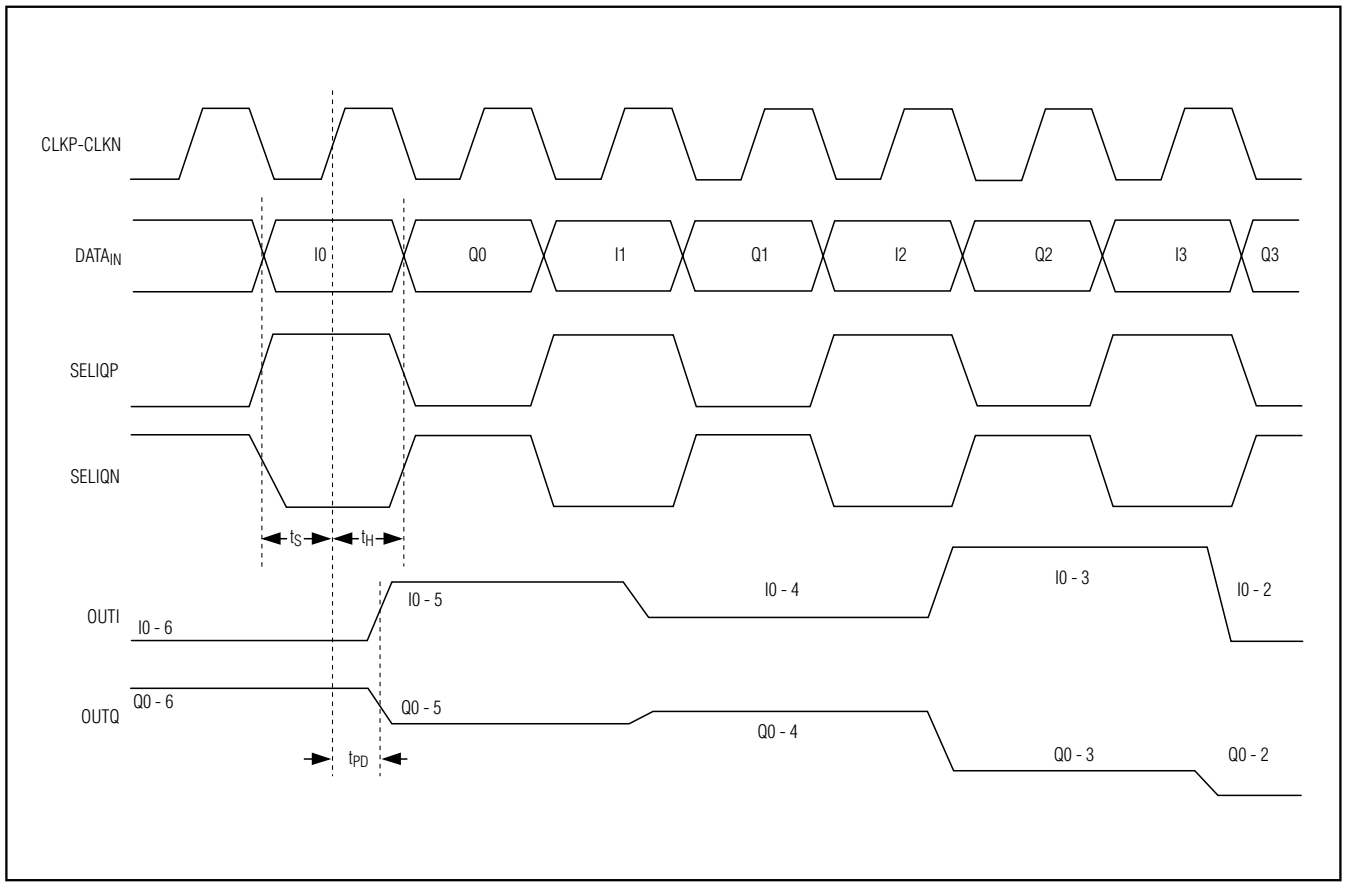


Figure 4. Timing Diagram

Data Timing Relationship

Figure 4 displays the timing relationship between digital LVDS data, clock, and output signals. The MAX5877 features a 2.0ns hold, a -1.2ns setup, and a 1.1ns propagation delay time. A nine (eight)-clock-cycle latency exists between CLKP/CLKN and OUTIP/OUTIN (OUTQP/OUTQN).

LVDS-Compatible Digital Inputs (B13P/B13N–B0P/B0N, XORP, XORN, SELIQP, SELIQN)

The MAX5877 latches B13P/N–B0P/N, XORP/N, and SELIQP/N data on the rising edge of the clock. A logic-high signal on SELIQP and a logic-low signal on SELIQN directs data onto the I-DAC inputs. A logic-low signal on SELIQP and a logic-high signal on SELIQN directs data onto the Q-DAC inputs.

The MAX5877 features LVDS receivers on the bus input interface with internal 110Ω termination resistors. See Figure 5. XORP and XORN are not internally terminated. These LVDS inputs (B13P/N–B0P/N) allow for a low differential voltage swing with low constant power consumption. A 1.25V common-mode level and 250mV differential input swing can be applied to the B13P/N–B0P/N, XORP/N, and SELIQP/N inputs.

The MAX5877 includes LVDS-compatible exclusive-OR inputs (XORP, XORN). Input data (all bits) is compared with the bits applied to XORP and XORN through exclusive-OR gates. Setting XORP high and XORN low inverts the input data. Setting XORP low and XORN high leaves the input data noninverted. By applying a previously encoded pseudo-random bit stream to the data input and applying decoding to XORP/XORN, the digital input data can be decorrelated from the DAC output, allowing for the troubleshooting of possible spurious or harmonic distortion degradation due to digital feedthrough on the printed circuit board (PCB). If XOR functionality is not required, connect XORP to GND and XORN to $DV_{DD1.8}$.

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

Table 2. DAC Output Code Table

DIGITAL INPUT CODE		OUT_P	OUT_N
OFFSET BINARY	TWO'S COMPLEMENT		
00 0000 0000 0000	10 0000 0000 0000	0	I_{OUTFS}
01 1111 1111 1111	00 0000 0000 0000	I_{OUTFS} / 2	I_{OUTFS} / 2
11 1111 1111 1111	01 1111 1111 1111	I_{OUTFS}	0

CMOS-Compatible Digital Inputs

Input Data Format Select (TORB)

The TORB input selects between two's-complement or offset binary digital input data. Set TORB to a CMOS-logic-high level to indicate a two's-complement input format. Set TORB to a CMOS-logic-low level to indicate an offset binary input format.

Power-Down Operation (PD)

The MAX5877 also features an active-high power-down mode that reduces the DAC's digital current consumption from 34mA to less than 5µA and the analog current consumption from 82mA to less than 2µA. Set PD high to power down the MAX5877. Set PD low for normal operation.

When powered down, the MAX5877 reduces the overall power consumption to less than 16µW. The MAX5877 requires 10ms to wake up from power-down and enter a fully operational state. The PD integrated pulldown resistor activates the MAX5877 if PD is left floating.

Applications Information

CLK Interface

The MAX5877 features a flexible differential clock input (CLKP, CLKN) with a separate supply (AV_{CLK}) to achieve optimum jitter performance. Use an ultra-low jitter clock to achieve the required noise density. Clock jitter must be less than $0.5ps_{RMS}$ for meeting the specified noise density. For that reason, the CLKP/CLKN input source must be designed carefully. The differential clock (CLKN and CLKP) input can be driven from a single-ended or a differential clock source. Differential clock drive is required to achieve the best dynamic performance from the DAC. For single-ended operation, drive CLKP with a low noise source and bypass CLKN to GND with a 0.1µF capacitor.

Figure 6 shows a convenient and quick way to apply a differential signal created from a single-ended source (e.g., HP 8662A signal generator) and a wideband transformer. Alternatively, these inputs can be driven from a CMOS-compatible clock source; however, it is recommended to use sinewave or AC-coupled differential ECL/PECL or LVDS drive for best dynamic performance.

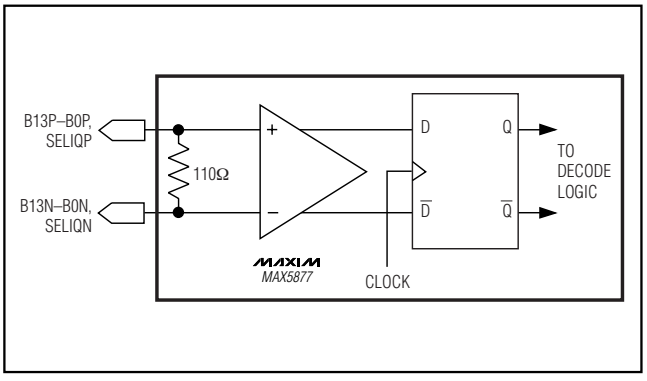


Figure 5. Simplified LVDS-Compatible Digital Input Structure

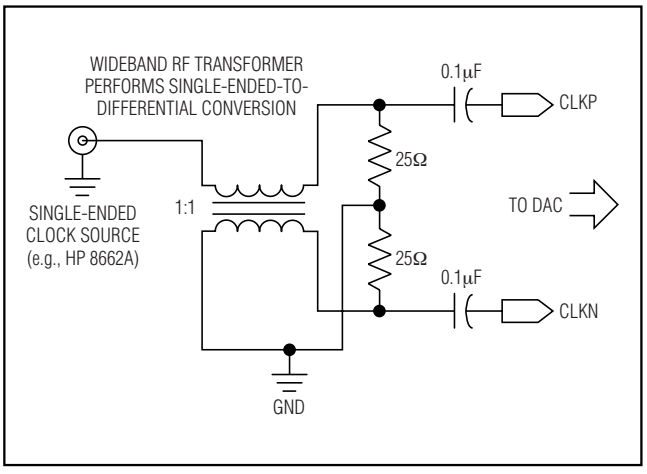


Figure 6. Differential Clock-Signal Generation

Differential-to-Single-Ended Conversion Using a Wideband RF Transformer

Use a pair of transformers (Figure 7) or a differential amplifier configuration to convert the differential voltage existing between OUTIP/OUTQP and OUTIN/OUTQN to a single-ended voltage. Optimize the dynamic performance by using a differential transformer-coupled output and limit the output power to < 0dBm full scale. Pay close attention to the transformer core saturation characteristics when selecting a transformer for the MAX5877. Transformer core saturation can introduce strong 2nd-order harmonic distortion especially at low output frequencies and high signal amplitudes. For best results, center tap the transformer to ground. When not using a transformer, terminate each DAC output to ground with a 25Ω resistor. Additionally, place a 50Ω resistor between the outputs (Figure 8).

For a single-ended unipolar output, select OUTIP (OUTQP) as the output and ground OUTIN (OUTQN). Driving the MAX5877 single-ended is not recommended since additional noise and distortion will be added.

The distortion performance of the DAC depends on the load impedance. The MAX5877 is optimized for 50Ω differential double termination. It can be used with a transformer output as shown in Figure 7 or just one 25Ω resistor from each output to ground and one 50Ω resistor between the outputs (Figure 8). This produces a full-scale output power of up to -2dBm, depending on the output current setting. Higher termination impedance can be used at the cost of degraded distortion performance and increased output noise voltage.

Grounding, Bypassing, and Power-Supply Considerations

Grounding and power-supply decoupling can strongly influence the MAX5877 performance. Unwanted digital crosstalk couples through the input, reference, power supply, and ground connections, and affects dynamic performance. High-speed, high-frequency applications require closely followed proper grounding and power-supply decoupling. These techniques reduce EMI and internal crosstalk that can significantly affect the MAX5877 dynamic performance.

Use a multilayer PCB with separate ground and power-supply planes. Run high-speed signals on lines directly above the ground plane. Keep digital signals as far away from sensitive analog inputs and outputs, reference input sense lines, and clock inputs as practical. Use a controlled-impedance, symmetric, differential design of data input, clock input, and the analog output lines to minimize 2nd-order harmonic distortion and noise components, thus optimizing the DAC's dynamic performance. Keep digital signal paths short and run lengths matched to avoid propagation delay and data skew mismatches.

The MAX5877 requires five separate power-supply inputs for analog ($AV_{DD1.8}$ and $AV_{DD3.3}$), digital ($DV_{DD1.8}$ and $DV_{DD3.3}$), and clock (AV_{CLK}) circuitry. All power-supply pins must be connected to their proper supply. Decouple each AV_{DD}, DV_{DD}, and AV_{CLK} input pin with a separate 0.1µF capacitor as close to the device as possible with the shortest possible connection to the ground plane (Figure 9). Minimize the analog and digital load capacitances for optimized operation. Decouple all three power-supply voltages at the point they enter the PCB with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

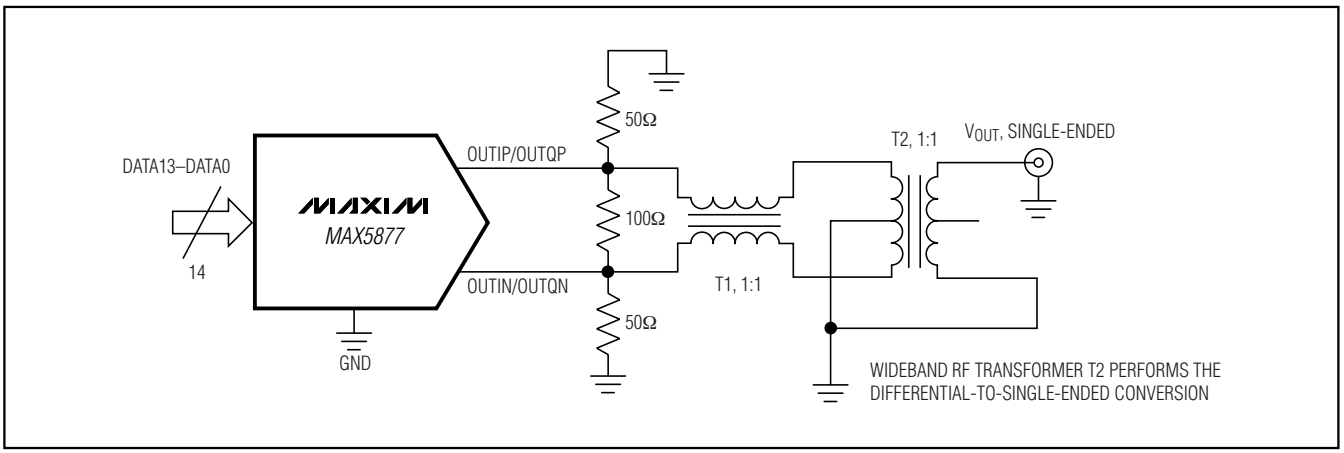


Figure 7. Differential-to-Single-Ended Conversion Using a Wideband RF Transformer

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

The analog and digital power-supply inputs $AV_{DD3.3}$, AV_{CLK}, and $DV_{DD3.3}$ allow a +3.135V to +3.465V supply voltage range. The analog and digital power-supply inputs $AV_{DD1.8}$ and $DV_{DD1.8}$ allow a +1.71V to +1.89V supply voltage range.

The MAX5877 is packaged in a 68-pin QFN-EP package, providing greater design flexibility and optimized DAC AC performance. The EP enables the use of necessary grounding techniques to ensure highest performance operation. Thermal efficiency is not the key factor, since the MAX5877 features low-power operation. The exposed pad ensures a minimum inductance ground connection between the DAC and the PCB's ground layer.

The data converter die attaches to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PCB side of the package. This allows for a solid attachment of the package to the PCB with standard infrared reflow (IR) soldering techniques. A specially created land pattern on the PCB, matching the size of the EP (6mm x 6mm), ensures the proper attachment and grounding of the DAC (refer to the MAX5878 EV kit). Designing vias into the land area and implementing large ground planes in the PCB design allow for the highest performance operation of the DAC. Use an array of at least 4 x 4 vias (≤ 0.3mm diameter per via hole and 1.2mm pitch between via holes) for this 68-pin QFN-EP package. **Connect the MAX5877 exposed paddle to GND.** Vias connect the land pattern to internal or external copper planes to spread heat. Use as many vias as possible to the ground plane to minimize inductance.

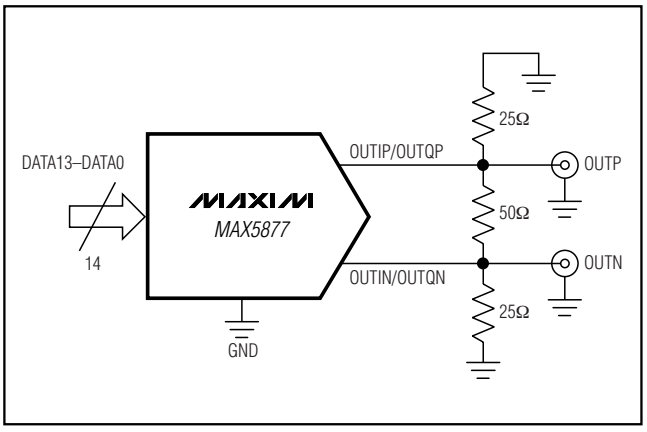


Figure 8. Differential Output Configuration

Static Performance Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from either a best straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees a monotonic transfer function.

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

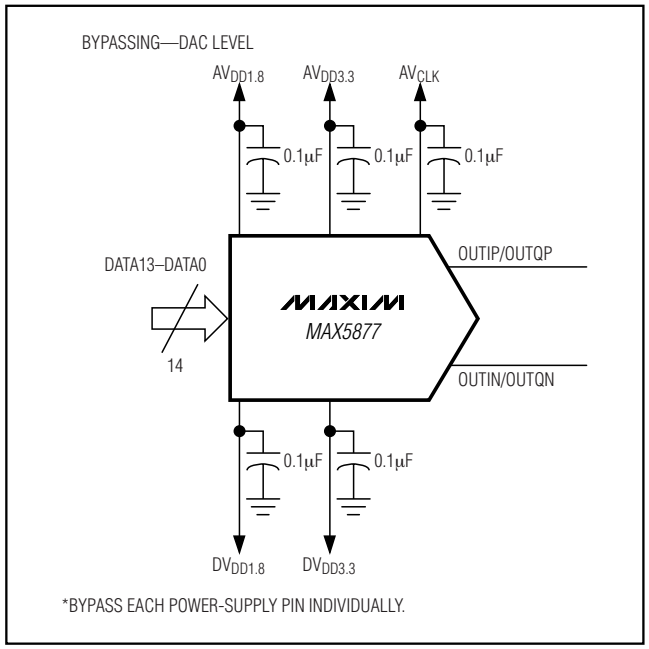


Figure 9. Recommended Power-Supply Decoupling and Bypassing Circuitry

Dynamic Performance Parameter Definitions

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog output (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum can be derived from the DAC's resolution (N bits):

$$SNR_{dB} = 6.02_{dB} \times N + 1.76_{dB}$$

However, noise sources such as thermal noise, reference noise, clock jitter, etc., affect the ideal reading; therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

Noise Spectral Density

The DAC output noise floor is the sum of the quantization noise and the output amplifier noise (thermal and shot noise). Noise spectral density is the noise power in 1Hz bandwidth, specified in dBFS/Hz.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of their next-largest distortion component. SFDR is usually measured in dBc and with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

Two-/Four-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD product(s) to either output tone.

Adjacent Channel Leakage Power Ratio (ACLR)

Commonly used in combination with wideband code-division multiple-access (W-CDMA), ACLR reflects the leakage power ratio in dB between the measured power within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

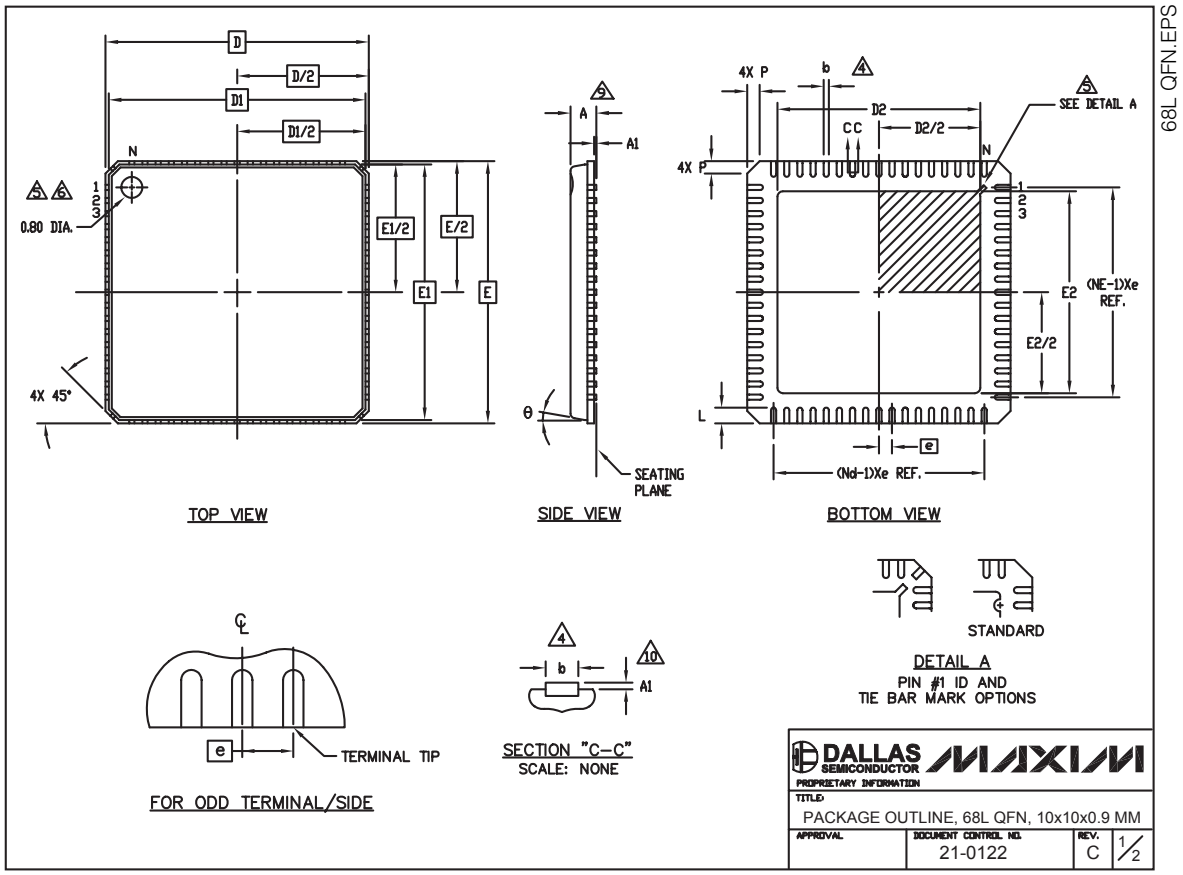
Glitch Impulse

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011...111 to 100...000. The glitch impulse is found by integrating the voltage of the glitch at the midscale transition over time. The glitch impulse is usually specified in pV•s.

14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



14-Bit, 250Msps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.65	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0122	C	1/2

Revision History

Pages changed at Rev 2: 1, 2, 3, 5, 13, 15, 16, 18

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com