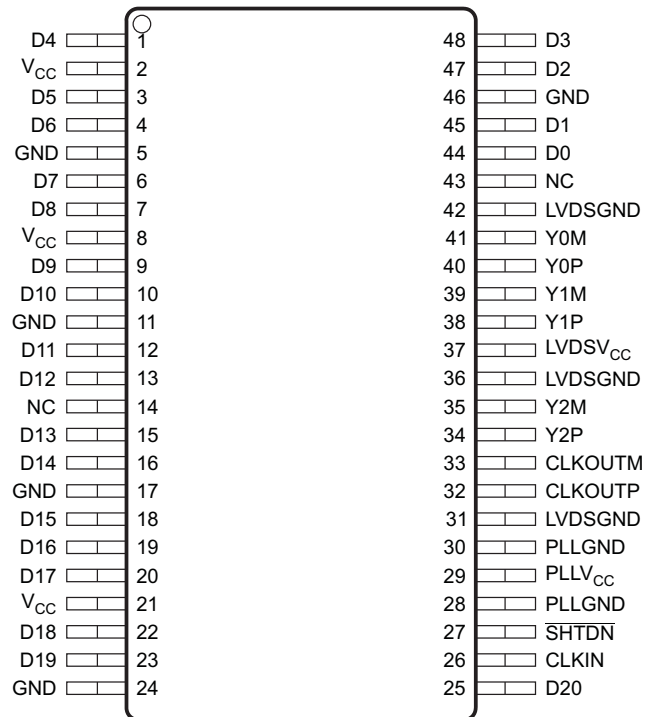# FLATLINK™ TRANSMITTERS

FEATURES

- **21:3 Data Channel Compression at up to 163 Million Bytes per Second Throughput**
- **Suited for SVGA, XGA, or SXGA Data Transmission From Controller to Display With Very Low EMI**
- **21 Data Channels Plus Clock-In Low-Voltage TTL and 3 Data Channels Plus Clock-Out Low-Voltage Differential**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant Data Inputs**
- **ESD Protection Exceeds 6 kV**
- **SN75LVDS84 Has Falling-Clock Edge-Triggered Inputs**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range:**
  - **31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C561**

DGG PACKAGE
(TOP VIEW)

D4	1	48	D3
V$_{CC}$	2	47	D2
D5	3	46	GND
D6	4	45	D1
GND	5	44	D0
D7	6	43	NC
D8	7	42	LVDSGND
V$_{CC}$	8	41	Y0M
D9	9	40	Y0P
D10	10	39	Y1M
GND	11	38	Y1P
D11	12	37	LVDSV$_{CC}$
D12	13	36	LVDSGND
NC	14	35	Y2M
D13	15	34	Y2P
D14	16	33	CLKOUTM
GND	17	32	CLKOUTP
D15	18	31	LVDSGND
D16	19	30	PLLGND
D17	20	29	PLLV$_{CC}$
V$_{CC}$	21	28	PLLGND
D18	22	27	$\overline{\text{SHTDN}}$
D19	23	26	CLKIN
GND	24	25	D20

NC - Not Connected

P0052-02

DESCRIPTION

The SN75LVDS84 FlatLink™ transmitter contains three 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit. These functions allow 21 bits of single-ended low-voltage TTL (LVTTL) data to be synchronously transmitted over three balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82 or SN75LVDS86.

When transmitting, data bits D0–D20 are each loaded into registers of the SN75LVDS84 on the falling edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times and then used to unload the data registers in 7-bit slices and serially. The three serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

AVAILABLE OPTIONS[1]

LATCHING CLOCK EDGE
FALLING
SN75LVDS84DGG
SN75LVDS84DGGR

(1) The R suffix indicates taped and reeled packaging.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FlatLink is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

DESCRIPTION (CONTINUED)

The SN75LVDS84 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only possible user intervention is the use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN75LVDS84 is characterized for operation over ambient free-air temperatures of 0°C to 70°C.

FUNCTIONAL BLOCK DIAGRAM

B0274-01

Product Folder Link(s) :*SN75LVDS84*
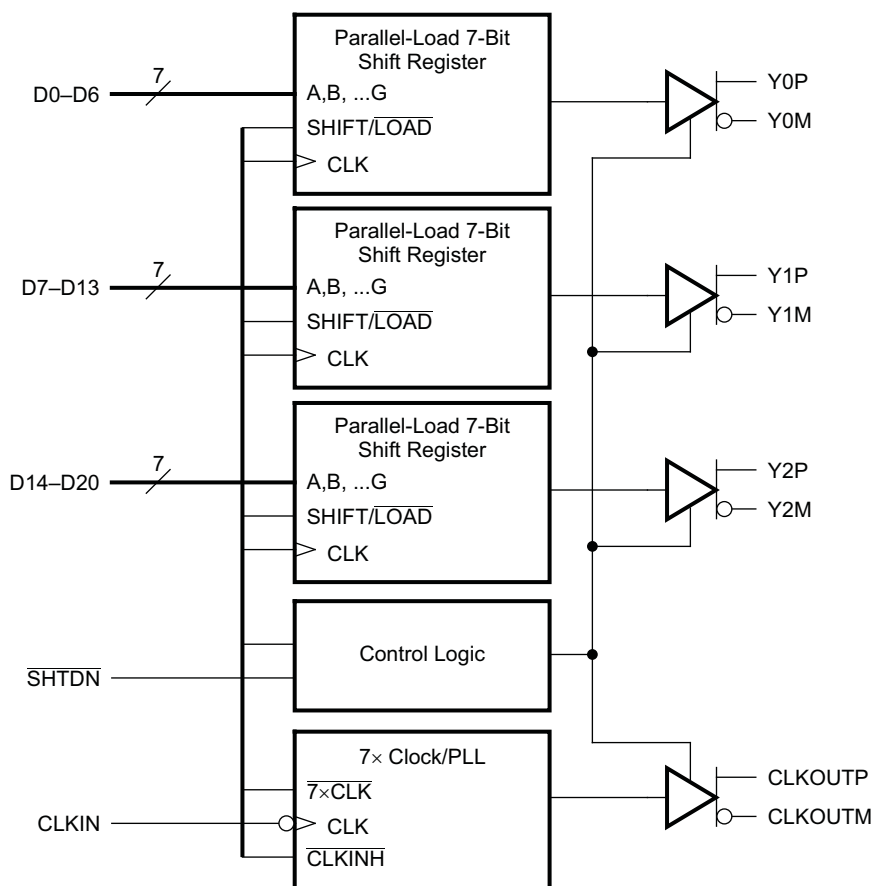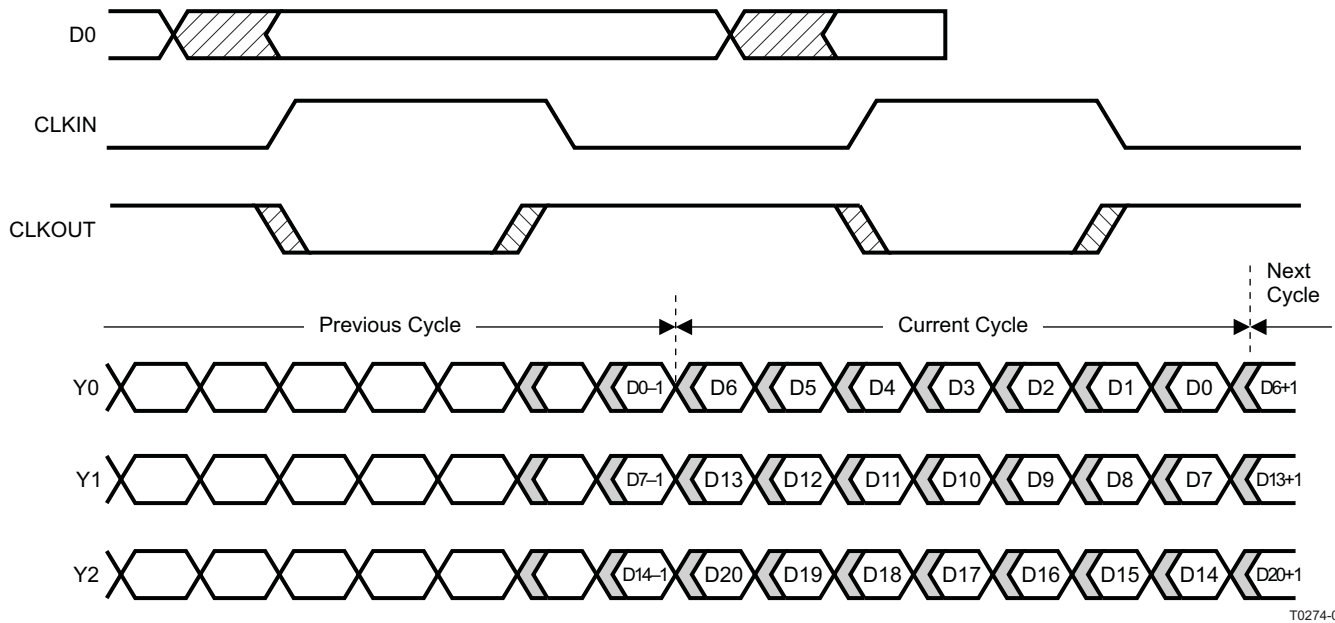
Figure 1. Load and Shift Timing Sequences

SCHEMATICS OF INPUT AND OUTPUT
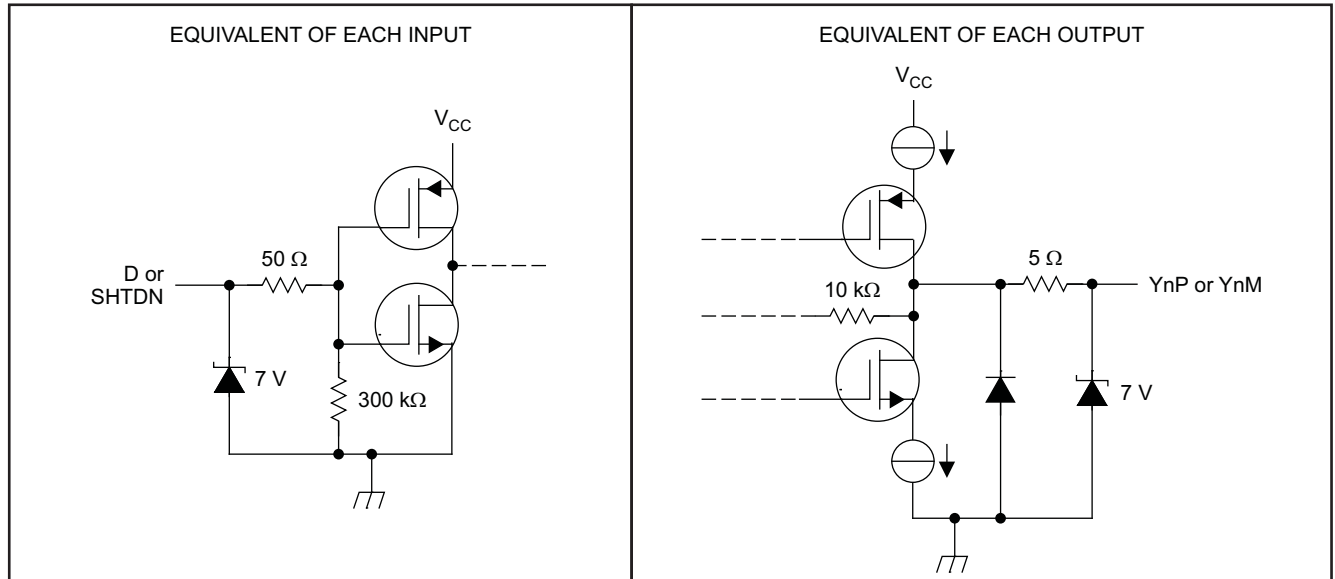
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

		VALUE	UNIT
V_{CC}	Supply voltage range[2]	−0.5 to 4	V
V_O	Output voltage range (all terminals)	−0.5 to V_{CC} + 0.5	V
V_I	Input voltage range (all terminals)	−0.5 to 5.5	
	Continuous total power dissipation	See Dissipation Rating Table	
T_{stg}	Storage temperature range	−6 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the GND terminals.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR[1] ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	1316 mW	13.1 mW/°C	726 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
Z_L	Differential load impedance	90		132	Ω
T_A	Operating free-air temperature	0		70	°C

TIMING REQUIREMENTS

	PARAMETER	MIN	TYP	MAX	UNIT
t_c	Input clock period	14.7		32.4	ns
t_w	Pulse duration, high-level input clock	$0.4\ t_c$		$0.6\ t_c$	ns
t_t	Transition time, input signal			5	ns
t_{su}	Setup time, data, D0–D27 valid before CLKIN↓ (See Figure 2)	3			ns
t_h	Hold time, data, D0–D27 valid after CLKIN↓ (See Figure 2)	1.5			ns

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT}	Input threshold voltagee			1.4		V
$|V_{OD}|$	Differential steady-state output voltage magnitude		247		454	mV
$\Delta|V_{OD}|$	Change in the steady-state differential output voltage magnitude between opposite binary states	R_L = 100 Ω, See Figure 3			50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			80	150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$			20	μA
I_{IL}	Low-level input current	$V_{IL} = 0$			±10	μA
I_{OS}	Short-circuit output current	$V_{O(Yn)} = 0$			±24	mA
		$V_{OD} = 0$			±12	mA
I_{OZ}	High-impedance output current	$V_O = 0$ to V_{CC}			±10	μA
$I_{CC(AVG)}$	Quiescent supply current (average)	Disabled, all inputs at GND			280	μA
		Enabled, R_L = 100 Ω (4 places), gray-scale pattern (see Figure 4), V_{CC} = 3.3 V, t_c = 15.38 ns		68	80	mA
		Enabled, R_L = 100 Ω, (4 places), worst-case pattern (see Figure 5), t_c = 15.38 ns		75	100	mA
C_I	Input capacitance			3		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{d0}	Delay time, CLKOUT↑ to serial bit position 0	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps[2], See Figure 6	−0.2	0	0.2	ns
t_{d1}	Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_c - 0.2$		$\frac{1}{7}t_c + 0.2$	ns
t_{d2}	Delay time, CLKOUT↑ to serial bit position 2		$\frac{2}{7}t_c - 0.2$		$\frac{2}{7}t_c + 0.2$	ns
t_{d3}	Delay time, CLKOUT↑ to serial bit position 3		$\frac{3}{7}t_c - 0.2$		$\frac{3}{7}t_c + 0.2$	ns
t_{d4}	Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_c - 0.2$		$\frac{4}{7}t_c + 0.2$	ns
t_{d5}	Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_c - 0.2$		$\frac{5}{7}t_c + 0.2$	ns
t_{d6}	Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_c - 0.2$		$\frac{6}{7}t_c + 0.2$	ns
$t_{sk(o)}$	Output skew, $t_n - \frac{n}{7}t_c$		−0.2		0.2	ns
t_{d7}	Delay time, CLKIN↓ to CLKOUT↑	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps[2], see Figure 6		4.2		ns
$\Delta t_{c(o)}$	Cycle time, output clock jitter[3]	t_c = 15.38 + 0.75 sin (2π500E3t) ±0.05 ns, See Figure 7		±70		ps
		t_c = 15.38 + 0.75 sin (2π3E3t) ±0.05 ns, See Figure 7		±187		ps
t_w	Pulse duration, high-level output clock			$\frac{4}{7}t_c$		ns
t_t	Transition time, differential output voltage (t_r or t_f)	See Figure 3	260	700	1500	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)	See Figure 8		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state (CLKOUT low)	See Figure 9		250		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.

PARAMETER MEASUREMENT INFORMATION
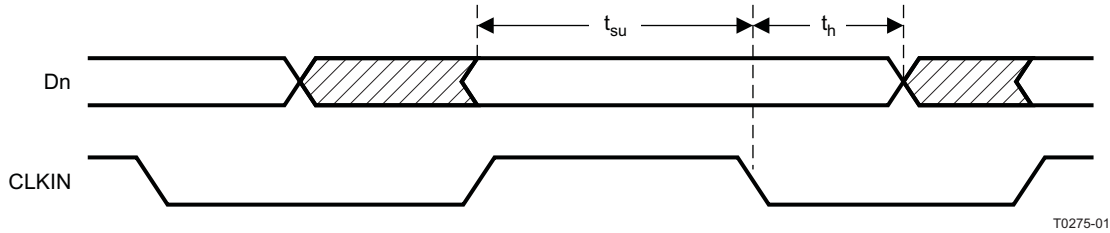
A.   All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Definition
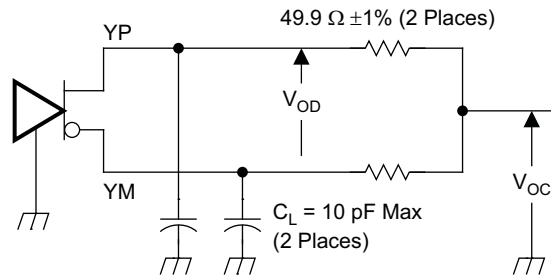
Note: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.

(a) Schematic
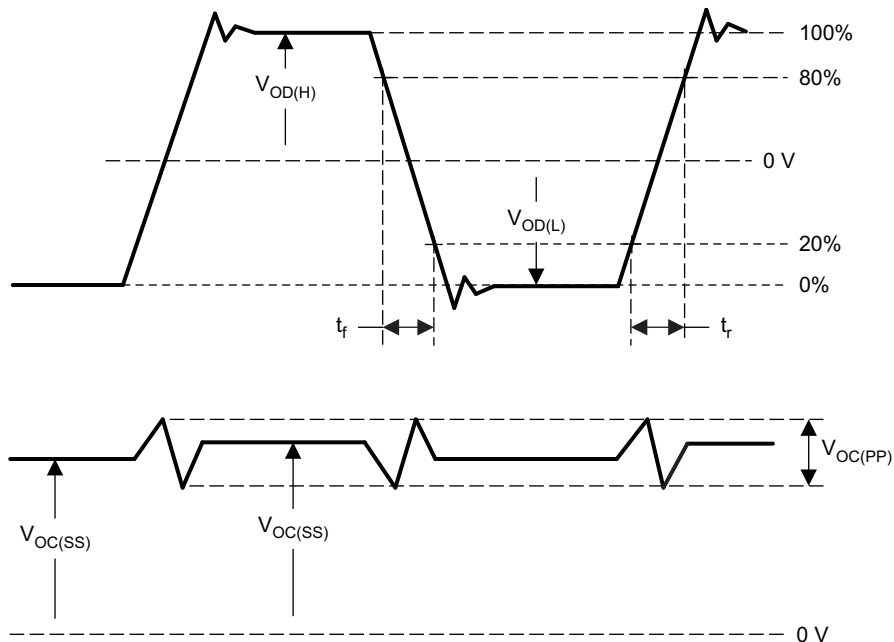
(b) Waveforms

Figure 3. Test Load and Voltage Definitions for LVDS Outputs

PARAMETER MEASUREMENT INFORMATION (continued)
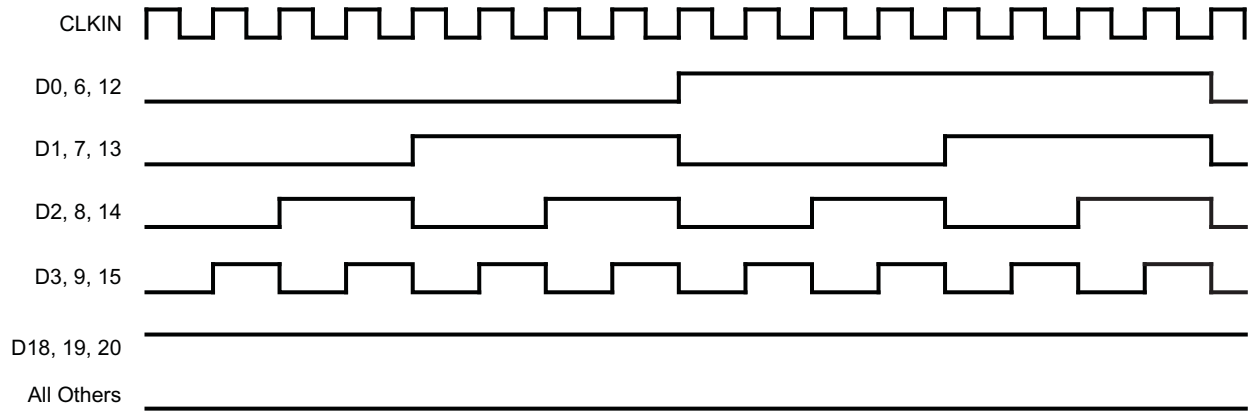
A.   The 16-grayscale test-pattern test device power consumption for a typical display pattern.

B. V_{IH} = 2 V and V_{IL} = 0.8 V

Figure 4. 16-Grayscale Test-Pattern Waveforms
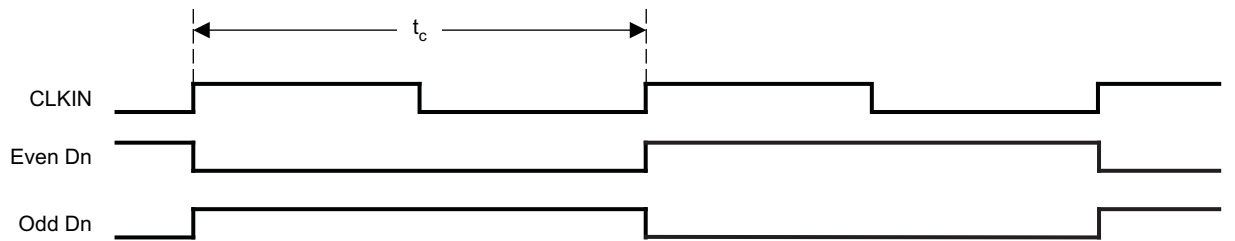
A.   The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

B. V_{IH} = 2 V and V_{IL} = 0.8 V

Figure 5. Worst-Case Test-Pattern Waveforms

Product Folder Link(s) :*SN75LVDS84*

PARAMETER MEASUREMENT INFORMATION (continued)
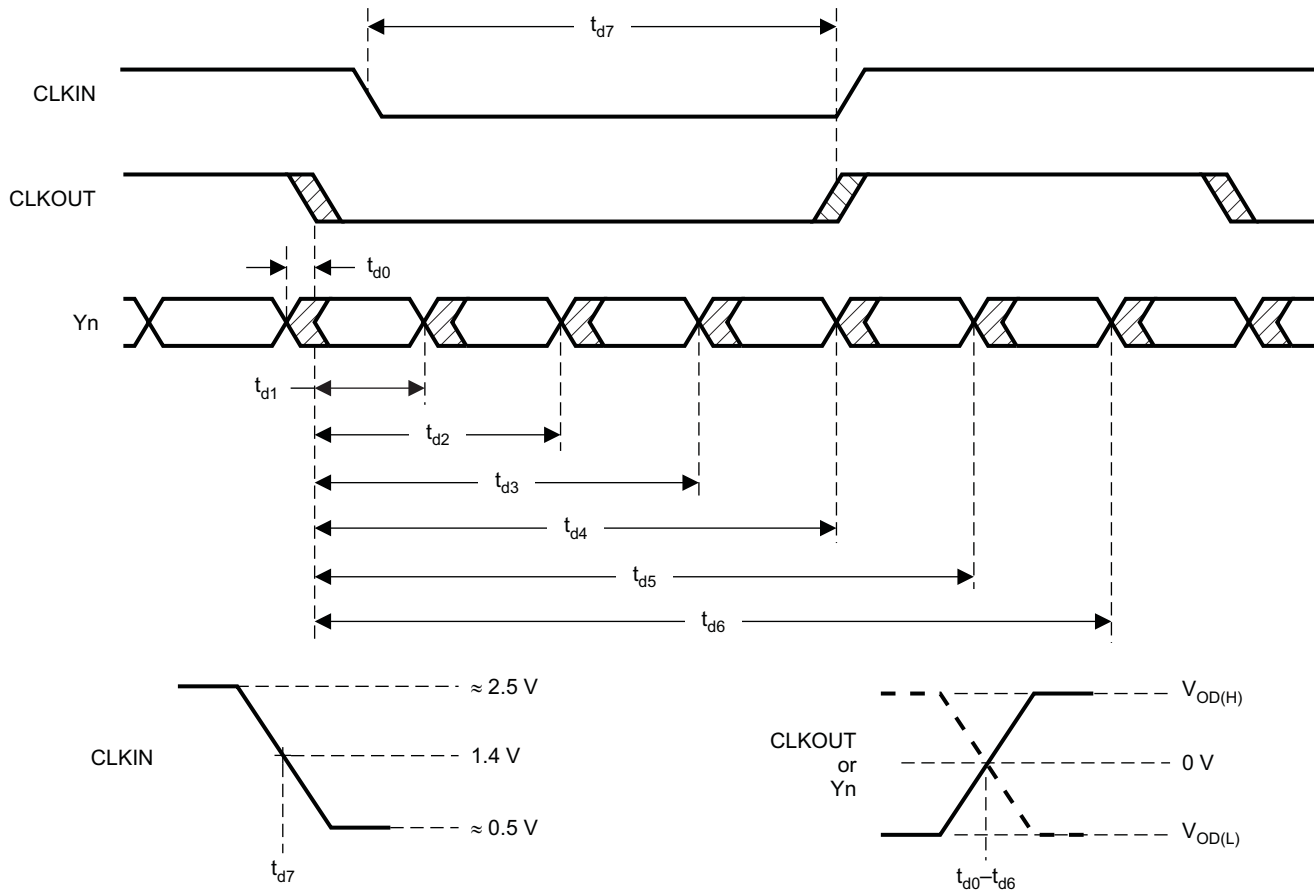
Figure 6. Timing Definitions
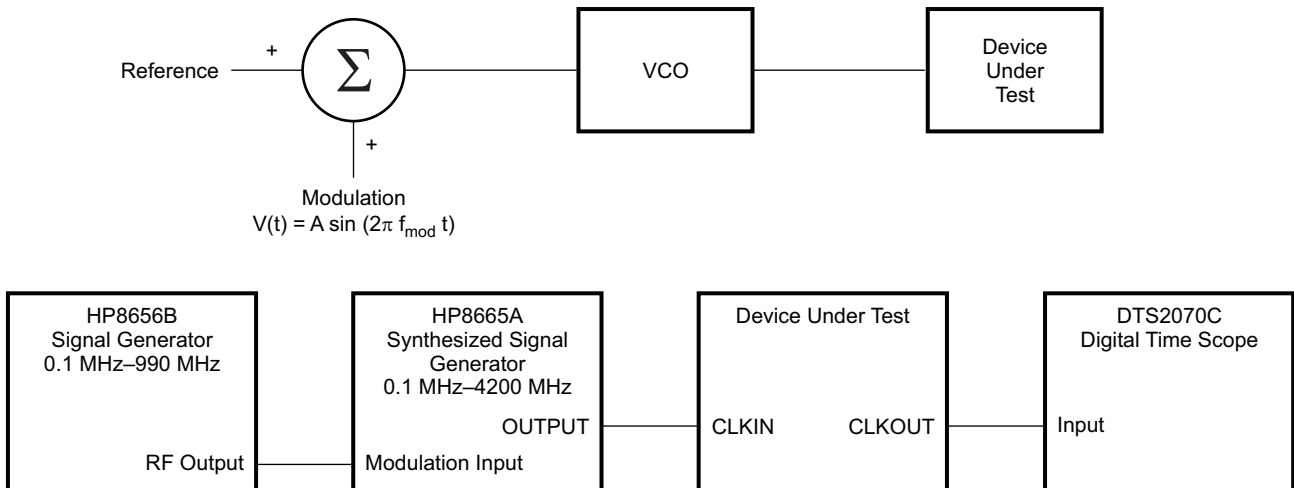
Figure 7. Clock Jitter Test Setup

TYPICAL CHARACTERISTICS
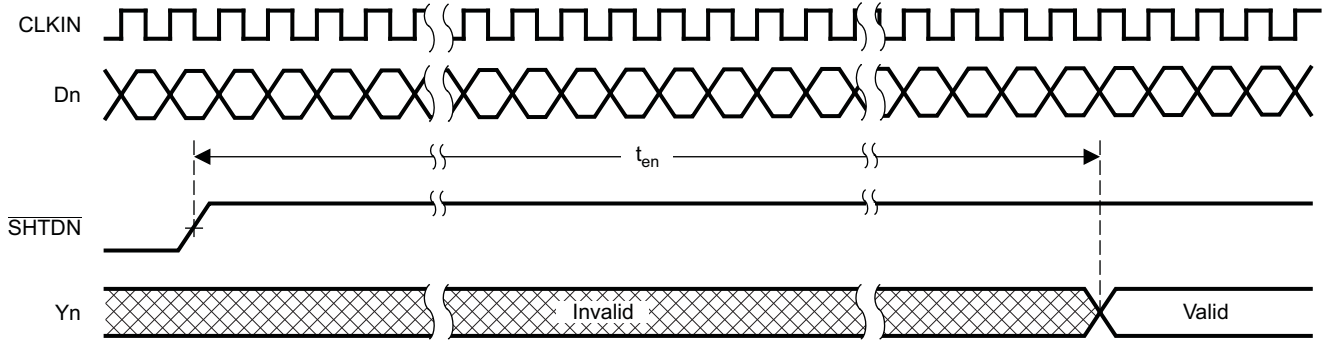
Figure 8. Enable Time Waveforms
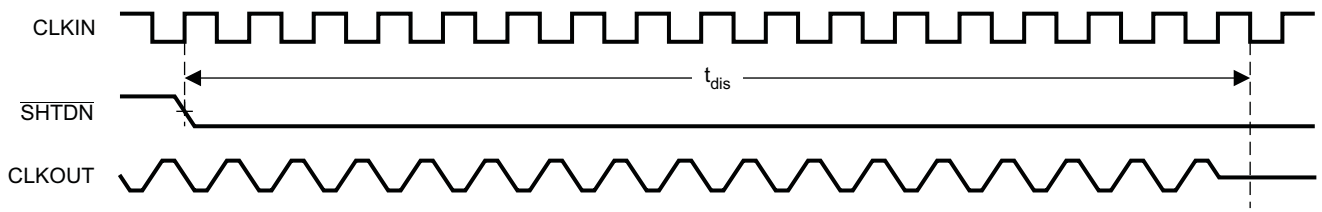
Figure 9. Disable Time Waveforms

AVERAGE SUPPLY CURRENT
vs
CLOCK FREQUENCY

Figure 10.

ZERO-TO-PEAK OUTPUT JITTER
vs
MODULATION FREQUENCY

Figure 11.

Product Folder Link(s) :*SN75LVDS84*
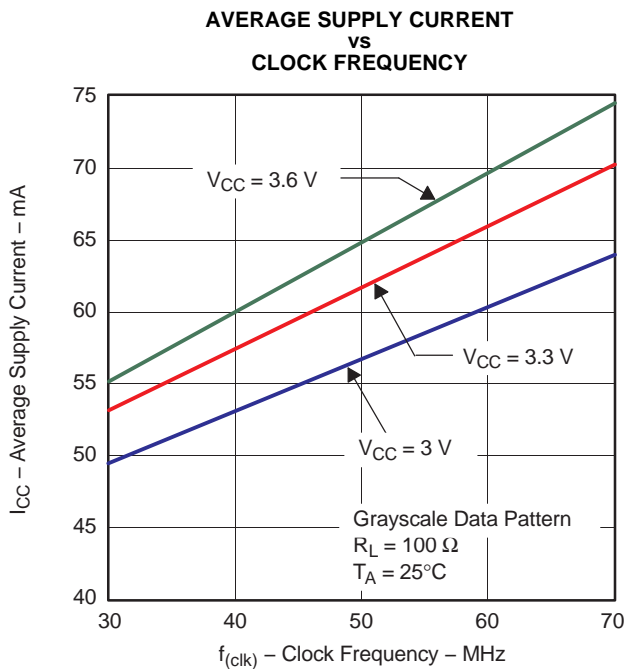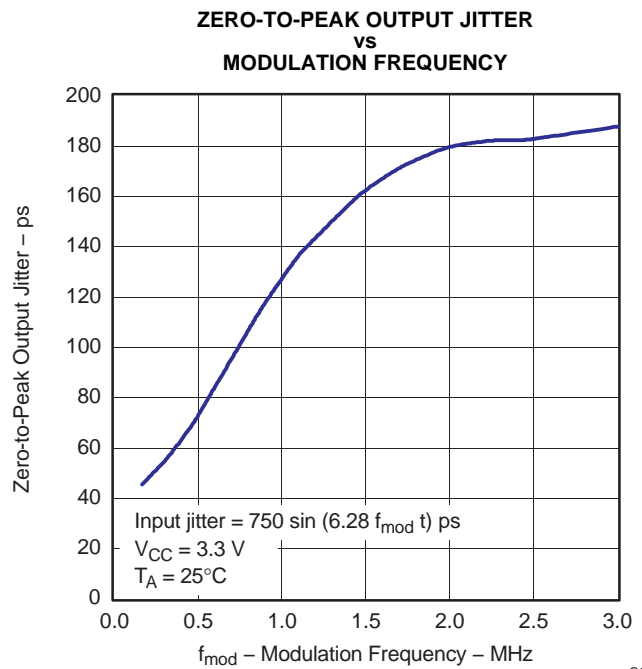
APPLICATION INFORMATION
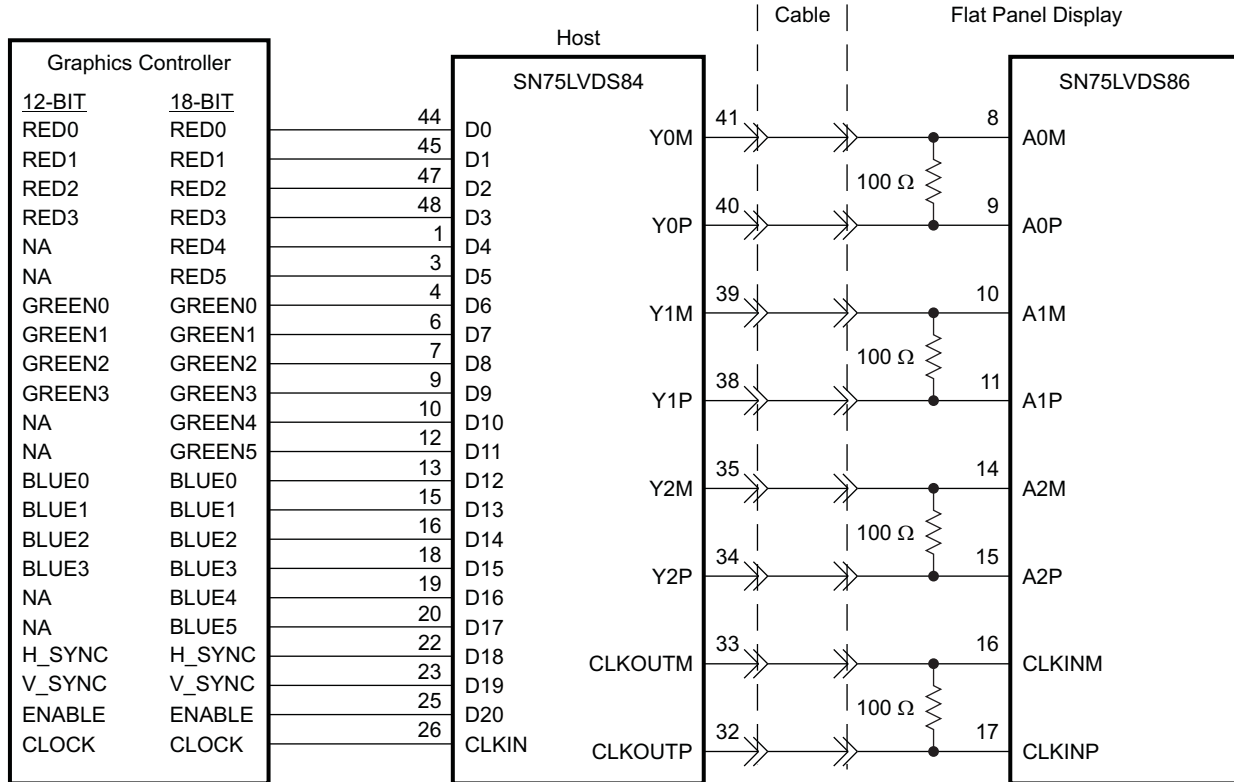
A. The five 100-Ω terminating resistors are recommended to be 0603 types.

B. NA – not applicable, these unused inputs should be left open.

Figure 12. Color Host to LCD Panel Application

Cable | Flat Panel Display

Host

Graphics Controller			SN75LVDS84		SN75LVDS82

12-BIT	18-BIT				
RED0	RED0	44	D0	Y0M 41 / 9	A0M
RED1	RED1	45	D1		100 Ω
RED2	RED2	47	D2		
RED3	RED3	48	D3	Y0P 40 / 10	A0P
NA	RED4	1	D4		
NA	RED5	3	D5		
GREEN0	GREEN0	4	D6	Y1M 39 / 11	A1M
GREEN1	GREEN1	6	D7		100 Ω
GREEN2	GREEN2	7	D8		
GREEN3	GREEN3	9	D9	Y1P 38 / 12	A1P
NA	GREEN4	10	D10		
NA	GREEN5	12	D11		
BLUE0	BLUE0	13	D12	Y2M 35 / 15	A2M
BLUE1	BLUE1	15	D13		100 Ω
BLUE2	BLUE2	16	D14		
BLUE3	BLUE3	18	D15	Y2P 34 / 16	A2P
NA	BLUE4	19	D16		
NA	BLUE5	20	D17		
H_SYNC	H_SYNC	22	D18	CLKOUTM 33	CLKINM
V_SYNC	V_SYNC	23	D19		100 Ω
ENABLE	ENABLE	25	D20		
CLOCK	CLOCK	26	CLKIN	CLKOUTP 32	CLKINP

A3M

100 Ω

A3P

B0277-01

A.   The four 100-Ω terminating resistors are recommended to be 0603 types.

B.   NA – not applicable, these unused inputs should be left open.

Figure 13. 18-Bit Color Host to 24-Bit LCD Display Panel Application
(See the FlatLink Designer's Guide (SLLA012) for more application information.)

Product Folder Link(s) :*SN75LVDS84*

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75LVDS84DGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS84DGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS84DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS84DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS
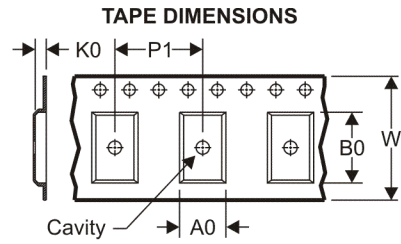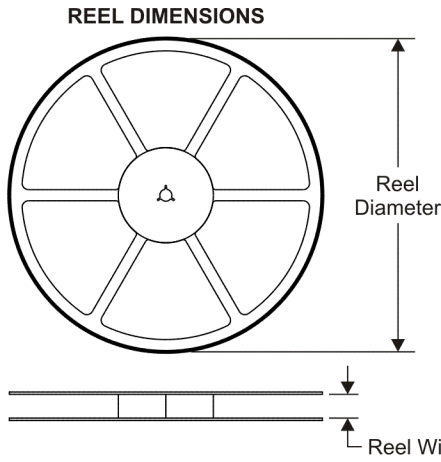
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

User Direction of Feed
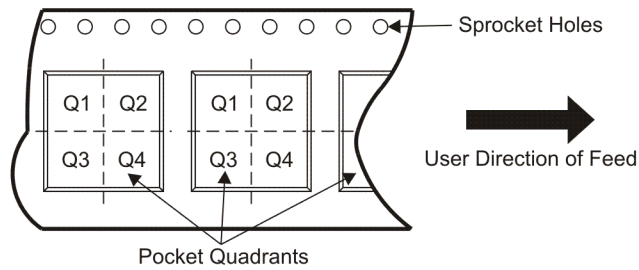
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS84DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS
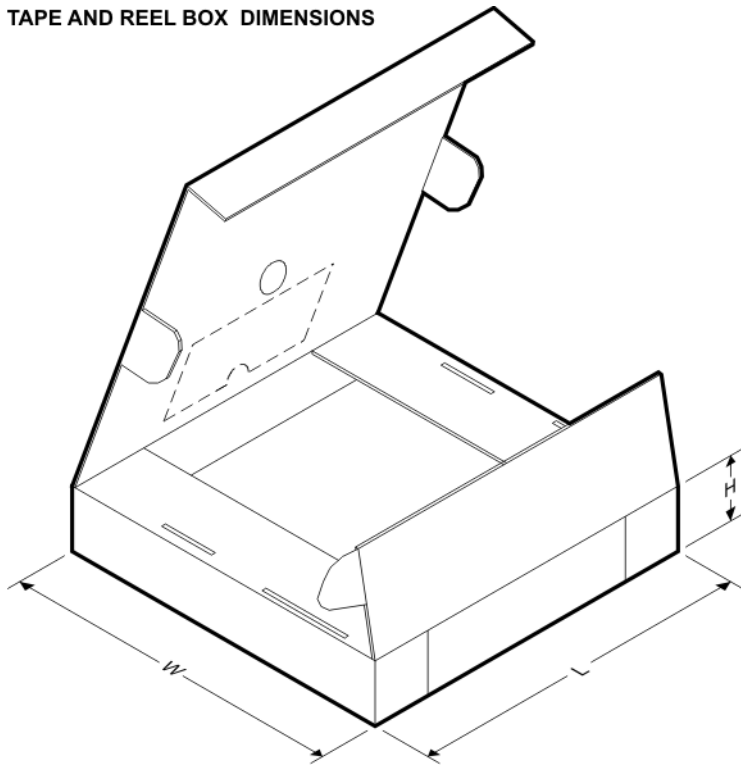
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS84DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

	PINS **	48	56	64
DIM				
A MAX		12,60	14,10	17,10
A MIN		12,40	13,90	16,90

4040078 / F 12/97
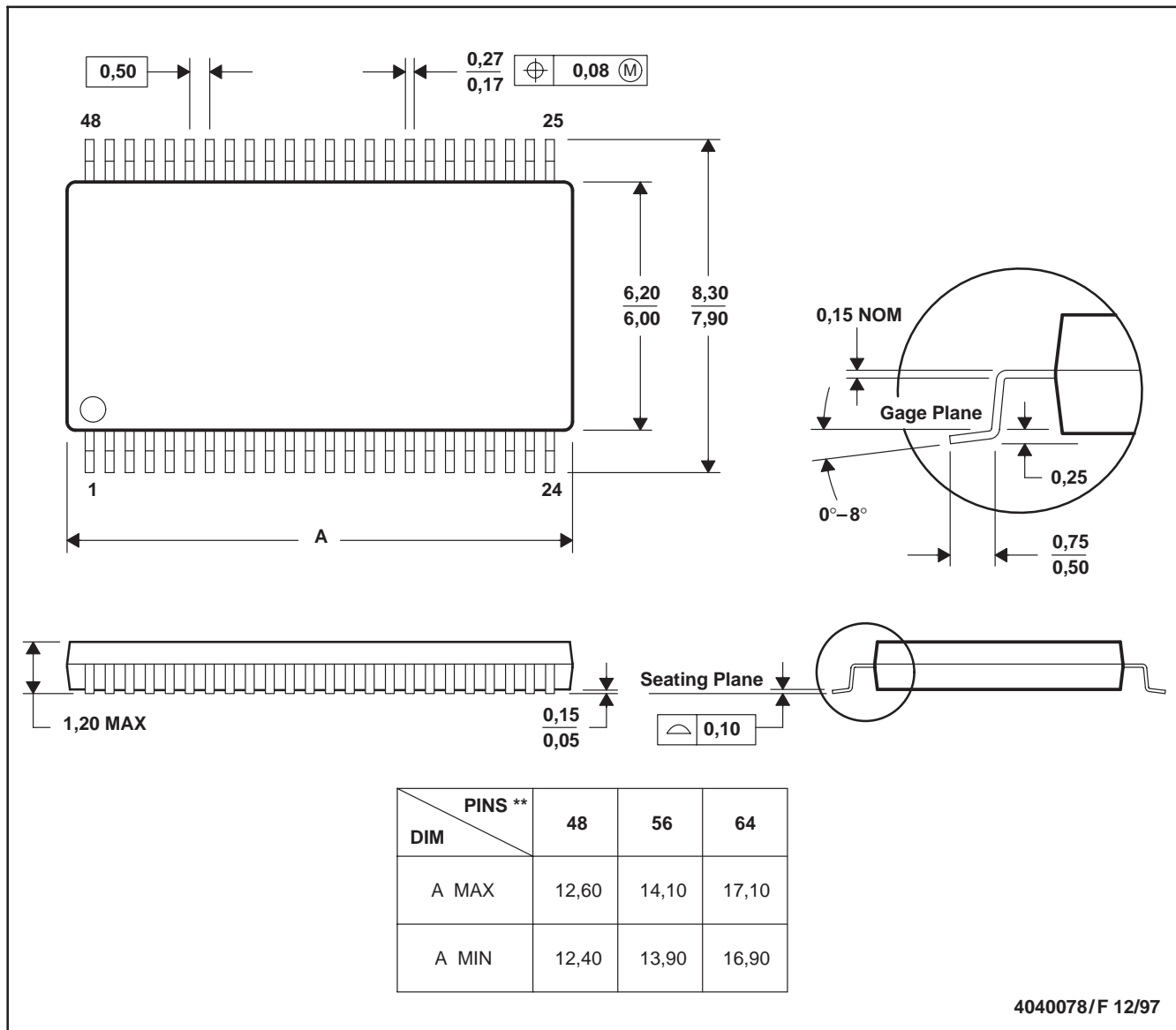
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

IMPORTANT NOTICE

AMEYA360
Components Supply Platform

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2Pai Semi	Ambarella	CanaanTek	Firstohm	GigaDevice	Vanguard Semiconductor

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