swissbit®

Product data sheet

Industrial SATA SSD 2.5''

X-55 Series

SATA II, high performance, high reliability
Endurance Managed NAND Flash

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X-55 Series – Industrial SATA Solid State Drive 2.5" 30GB to 480GB

1 Feature summary

- Form factor:
  - 2.5-inch SATA Solid State Drive (SSD)
  - 100mm x 70mm x 9.2mm
  - 7+15 pin (SATA+power) locking/latching SATA connector
- Interface:
  - SATA Rev 2.6 – 3Gbit/s (1.5Gbit/s compatible)
- Feature connector for
  - Quick erase and write protect input
  - Device activity and quick erase output (LED)
  - Ground pin
- Optional various secure erase/sanitize/purge methods (hardware and software triggered)
- Highly-integrated memory controller
  - Max. UDMA6 supported
  - Max. PIO mode 4, MDMA2 supported
  - Endurance Managed NAND Flash (EM-MLC)
  - Hardware BCH-code ECC (40 Bit correction per 2 sectors)
  - Fix drive configuration
- Low-power CMOS technology
- 5.0V ± 10% power supply
- Low Power, less than 1W (idle) / 3.5 W (operation) / 0.7W slumber average current
- No mechanical noise
- Wear Leveling: active wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Mechanical robustness (MIL-STD810)
- High reliability
  - Endurance Managed MLC NAND Flash technology (EM-MLC)
  - Data retention 5 years
  - StaticDataRefresh and EarlyRetirement Technologies for data refresh
  - MTBF ≥ 2,000,000 hours
  - Number of connector insertions/removals: >1,000 cycles
- High performance
  - Up to 300MB/s burst transfer rate in SATA II – 3.0Gb/sec
  - Sustained Read / Write Performance: up to 240MB/s / 160MB/s
  - 4KB Read / Write IOPS: up to 14500 / 3100
  - Access time <0.2ms
  - TRIM and NCQ support
- Available densities
  - 30GB up to 480GB (EM-MLC)
- S.M.A.R.T. with extended information
- HPA, security feature set, 48bit feature set
- internal temperature sensor (current, minimum, maximum)
- Operation systems: Microsoft Windows8, 7, Vista, XP (all 32/64bit), Linux, Apple MacOS X, Embedded versions, RTOS
- Firmware update possible
- 2 Operating Temperature ranges
  - Commercial Temperature range 0 … +70°C
  - Industrial Temperature range -40 … +85°C
- Life Cycle Management
- Controlled BOM
- RoHS, China-RoHS, REACH compatible, WEEE,CE, FCC compliant

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3 Order Information

The X-55 Series part numbers (with EM-MLC NAND Flash) are listed below for different temperature ranges.

3.1 Current standard part numbers, commercial temperature grade

FIX / SATA II/ UDMA6, MDMA2, PIO4, commercial

Density	Part Number
30GB	SFSA030GQ1BJ2TO-C-LB-216-STD
60GB	SFSA060GQ1BJ4TO-C-LB-216-STD
120GB	SFSA120GQ1BJ8TO-C-LB-216-STD
240GB	SFSA240GQ1BJ4TO-C-OC-216-STD
480GB	SFSA480GQ1BJ8TO-C-OC-216-STD

Table 1: Commercial temperature product list

3.2 Current standard part numbers, industrial temperature grade

FIX / SATA II/ UDMA6, MDMA2, PIO4, industrial

Density	Part Number
30GB	SFSA030GQ1BJ2TO-I-LB-216-STD
60GB	SFSA060GQ1BJ4TO-I-LB-216-STD
120GB	SFSA120GQ1BJ8TO-I-LB-216-STD
240GB	SFSA240GQ1BJ4TO-I-OC-216-STD
480GB	SFSA480GQ1BJ8TO-I-OC-216-STD

Table 2: Industrial temperature product list

3.3 General standard part numbers

FIX / SATA II/ UDMA6, MDMA2, PIO4

Density	Part Number
30GB	SFSA030GQxBJ2TO-t-LB-2y6-ccc
60GB	SFSA060GQxBJ4TO-t-LB-2y6-ccc
120GB	SFSA120GQxBJ8TO-t-LB-2y6-ccc
240GB	SFSA240GQxBJ4TO-t-OC-2y6-ccc
480GB	SFSA480GQxBJ8TO-t-OC-2y6-ccc

Table 3: General product list

x= depends on product generation, y= depends on firmware generation
t= C for commercial temperature; I for industrial temperature
ccc=STD for standard SSDs; STC for conformal coated SSDs

3.4 Offered OEM options

- Customer specified drive size and drive geometry (C/H/S – cylinder/head/sector)
- Customer specified drive ID (Strings)
- Preload service (also drive images with any file system)
- Conformal coating (part number suffix "–STC")
- Erase input at feature connector
- Various Enhanced Secure Erase / Sanitize / Purge algorithms hardware and software
  - DoD5220.22-M
  - NSA (Manual 130-2)
  - USA AF AFFSSI 5020
  - USA Army 380-19
  - USA Navy NAVSO P-5239-26
  - IREC (IRIG) 106
  - NSA 9-12
- 3.3V optional on request
- ...

4 Product Specification

The Solid State Drive (SSD) is a small form factor (2.5'') non-volatile memory drive which provides high capacity data storage. It has a standard combined connector with SATA and power/control part. The SSD works at a supply voltage of 5V.
The drive with the SATA interface operates in Mode 2.0 (1.5 or 3.0 Gb/s burst).
The drive has an internal **intelligent controller** that manages interface protocols, data storage and retrieval as well as hardware BCH-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware BCH-code ECC allows to detect and correct **40 random bits per 1024 data bytes**.
The SSD has Early Weak Block Retirement Detection and data shaping for higher data reliability.
The drive has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The SSD has hardware and software write protection, and hardware and software security erase function with different military erase algorithms.
The specification has been realized and approved by the ATA/ATAPI-8 specification.
The system highlights are shown in Table 4 ...Table 12.

Related Documentation

- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-8)
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994

4.1 Physical description

The SSD contains a flash controller and Flash memory modules. The controller interfaces with a host system allowing data to be written to and read from the Flash memory modules.
The SSD is offered in a 2.5'' size package with a standard SATA connector.
The SSD has 4 screw holes at the side and 4 at the bottom side.

Figure 5 and Figure 6 (page 45) show SSD dimensions and connector location.

4.2 System Performance

Table 4: System Performance (measured)

System Performance		Typ.	Unit
Data transfer Rate (SATA burst (1.5 or 3.0Gb/s))		150 or 300	MB/s
Sequential Read	30GB	234	MB/s
	60GB	238	
	120GB	237	
	240GB	237	
	480GB	237	
Sequential Write	30GB	42	
	60GB	84	
	120GB	151	
	240GB	151	
	480GB	156	
Random Read 4kB	30GB	13550	IOPS
	60GB	14350	
	120GB	14560	
	240GB	14690	
	480GB	14840	
Random Write 4kB	30GB	1120	
	60GB	1800	
	120GB	2490	
	240GB	3010	
	480GB	2500	

All values refer to Toshiba Flash chips (see part number) with SATA 3.0Gbit/s. Sustained Speed depends on flash type and number, file/cluster size, and burst speed.

MB/s = 1,000,000 byte/s. Measured with CrystalDiskMark 3.0.2 on Windows 7, NTFS, 5x500MB, QD=32, 500MB

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage	4.5V to 5.5V *)

*) SSD reset below 4.2V

Table 6: Current consumption @5V *)

Current Consumption (mA) typ/max	partial/ slumber	Idle Mode	Read	Write	QErase	Overwrite	Unit
30GB	100/120	170/190	260/290	280/400	230	250	mA
60GB	100/120	170/190	270/300	380/530	300	320	
120GB	120/140	170/190	280/310	490/630	380	490	
240GB	120/140	170/190	290/320	510/650	400	510	
480GB	120/140	170/190	320/340	550/700	430	530	

*) All values are typical at 25° C and nominal supply voltage and refer to SATAII sequential performance test random pattern.
Due to simultaneous flash erase operations current bursts of up to 2000mA can occur for a few milliseconds. The voltage at the connector must be kept always above 4.2V. Otherwise the SSD performs a reset.

4.3.2 Recommended Storage Conditions

Table 7: Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-55°C to 95°C *)
Industrial Storage Temperature	-55°C to 95°C *)

*) Storage Temperatures above 40°C can reduce the data retention

4.3.3 Shock, Vibration, and Humidity

Table 8: Shock, Vibration, and Humidity

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	MIL-STD810; 20G, 10-2000Hz Random
Shock	MIL-STD810; 2000G, 0.4ms; 50G 11ms

4.4 Physical Dimensions

Table 9: Physical Dimensions

Physical Dimensions		Unit
Length	100.1±0.2	mm
Width	69.85±0.2	
Thickness	9.2±0.2	
Weight (typ.)	80	g

4.5 Reliability

Table 10: System Reliability and Maintenance

Parameter	Value
MTBF (at 25°C)	≥ 2,000,000 hours
Insertions/Removals	> 1,000 (connector with latch)
Data Retention EM-MLC (JESD47)	5 years @ down to 90% average erase count (up to 3k PE cycles) 1 year @ down to 67% average erase count (up to 10k PE cycles) 3 month @ life end (30k PE cycles)

Data retention would be reduced by high temperature operation and storage.

4.6 Endurance (JESD219A)

Table 11: Measured Endurance values (TByte Written, JESD 219A specification)

Density (GB)	30	60	120	240	480
Client workload (TBW)	(~180)	420	870	2130	(~4000)
Enterprise workload (TBW)	90	310	670	2300	3100
Video streaming workload (TBW)	~950	~1900	~3800	~7600	~15200

JESD219A standard defines workloads for the endurance rating and endurance verification of SSD application classes. These workloads shall be used in conjunction with the Solid State Drive (SSD) Requirements and Endurance Test Method standard, JESD218. The TBW values are estimations, how many data can be written in the applications, until the number of program erase cycles of the flash cells are reached.
The video streaming workload is a mainly sequential write application.

4.7 Drive geometry / CHS parameter

Table 12: SSD density specification

Density	Default cylinders	Default heads	Default sectors	Sectors drive	Total addressable Bytes	Remark
30GB	16'383*)	16	63	58'626'288	30'016'659'456	IDEMA value
60GB	16'383*)	16	63	117'231'408	60'022'480'896	IDEMA value
120GB	16'383*)	16	63	234'441'648	120'034'123'776	IDEMA value
240GB	16'383*)	16	63	468'862'128	240'057'409'536	IDEMA value
480GB	16'383*)	16	63	937'703'088	480'103'981'056	IDEMA value

*) The CHS access is limited to about 8GB. Above 8GB, the drive must be addressed in LBA mode.

4.8 Temperature sensor

The SSD has an internal temperature sensor. The current temperature, minimum value, maximum value can be read out from S.M.A.R.T. information (Raw values of Attribute ID 194).

5 Electrical interface

5.1 SATA and Power connector description

The SSD is connected with a standard 7 pin SATA connector and a standard 15 pin SATA power connector.

The signal/pin assignments and descriptions are listed in Table 13

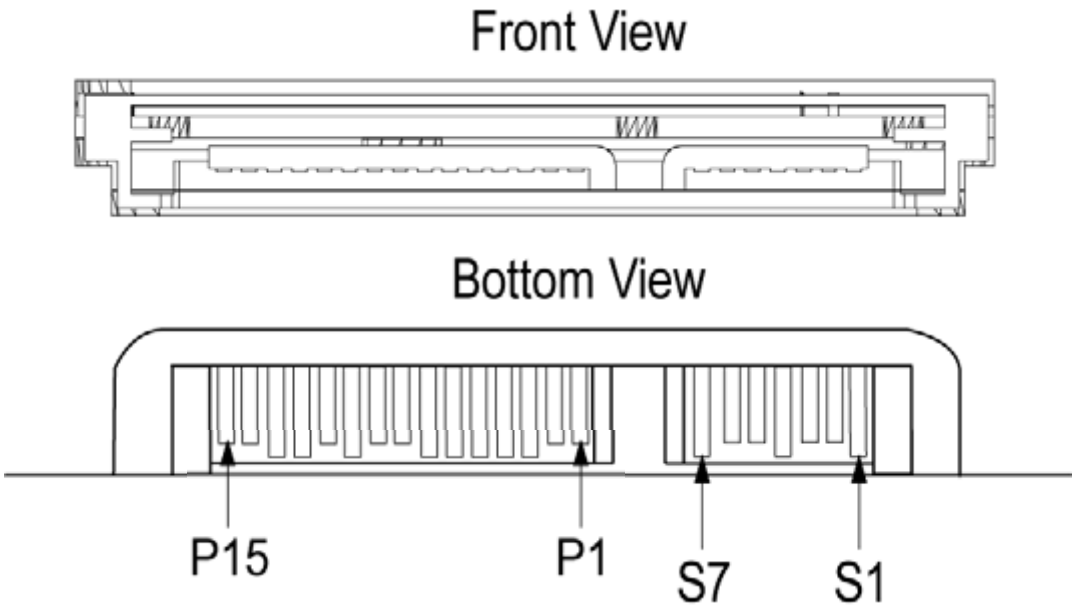


Figure 1: SATA and power connector

The signal/pin assignments and descriptions are listed in Table 13.

Table 13: Pin Assignment, name, and description

Pin	Signal Name	Description
S1	Ground	Signal Ground
S2	A+	+ Differential Receive signal
S3	A-	- Differential Receive signal
S4	Ground	Signal Ground
S5	B-	- Differential Transmit signal
S6	B+	+ Differential Transmit signal
S7	Ground	Signal Ground
P1...P3	3.3V	3.3V power (not used, optional on request)
P4...P6	Ground	Power Ground
P7...P9	5V	5V power
P10	Ground	Power Ground
P11	Device activity	Device activity, active low *)
P12	Ground	Power Ground
P13...P15	12V	12V power (not used)

*) driven low, no internal pull up resistor connected

5.2 Feature connector

Figure 2: SSD connector side with power, SATA and feature connector

The X-55 SSD has a 5-circuit feature connector beside the SATA connector for the extra function

- write protect
- hardware erase triggering

as well as for operation signalization

- device activity
- erase activity

This feature connector mates e.g. with the Molex connector (part number 5013300500)
with 5 wire to board terminals (part number 1513340000)

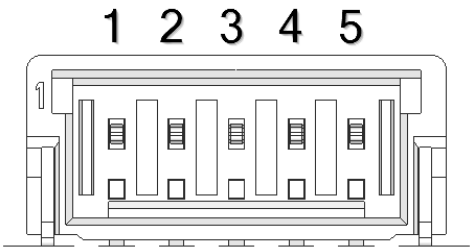
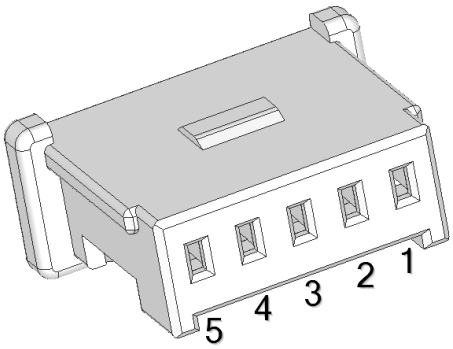
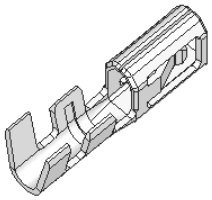


Figure 3: Feature connector at SSD



Mating cable connector



Wire to board terminal

Pin	function	usage
1	Write Protect input	Ground this pin for write protection
2	Ground	System level ground for 0 Volt reference level
3	Device activity output	Connect an LED to ground (serial resistor depending on color) LED is on at device activity by SATA access
4	Erase trigger input	If this pin is grounded for at least 0.8sec enhanced erase starts
5	Erase activity output	Connect an LED to ground (serial resistor depending on color) LED blinks, if erase is in progress

Erase (algorithm optional) can also be started with "Security Erase Unit" command (0xF1, 0xF3, 0xF4 command sequence)

5.3 Electrical Specification

5.3.1 Power supply

The standard SSD is supplied with 5V. (Optional 3.3V supply is possible on request.)

Table 14 and Table 15 define the DC Characteristics of the SSD. Unless otherwise stated, conditions are:

- Vcc = 5.0V ± 10%
- 0°C to +70°C

The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 15.

Table 14: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power (5V pins)	VCC	-0.3V to 6.5V
min operating voltage for operation (5V pins)	VCC	4.2V

Table 15: Input Power write and read

Mode	Maximum Average RMS Current	Conditions
SATA II (3.0Gb/s)	500mA*)	5V
SATA I (1.5Gb/s)	400mA*)	
Idle	190mA	

*) The SSD needs current peaks of >1A during some milliseconds.

The power supply must guarantee a voltage of 4.2V.

Below this voltage, the SSD performs a hardware reset.

5.3.2 Feature connector

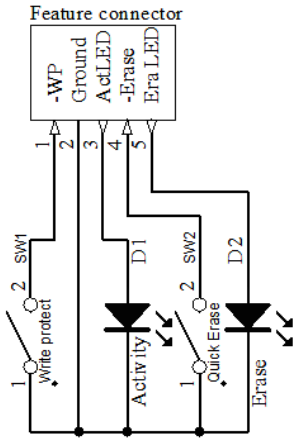


Figure 4: Suggested circuit for feature connector

LED outputs

- pin3 device activity
- pin5 erase activity

driven high (3.3V, active) and low (GND, idle)
13mA short current
LED can be connected directly to these pins to GND (pin2)

Inputs

- pin1 -write protect
- pin5 -erase trigger (if option supported)

these pins are low active
0.4mA short current
switches can be connected directly to these pins to GND (pin2)

6 ATA command description

This section provides information on the ATA commands supported by the SSD. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter, and then writing the command code to the register.

ATA Command Flow

DDMAI0: DMA_in State	This state is activated when the device receives a DMA data-in command or the transmission of one or more data FIS is required to complete the command. When in this state, the device shall prepare the data for transfer of a data FIS to the host.
Transition DDMAI0:1	When the device has the data ready to transfer a data FIS, the device shall transition to the DDMAI1: Send_data state. Transition DDMAI0:2 When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DDMAI2: Send_status state.
DDMAI1: Send_data	This state is activated when the device has the data ready to transfer a data FIS to the host. When in this state, the device shall request that the Transport layer transmit a data FIS containing the data. The device command layer shall request a Data FIS size of no more than 2,048 Dwords (8KB).
Transition DDMAI1:1	When the data FIS has been transferred, the device shall transition to the DMA0I0: DMA_in state.
DDMAI2: Send_status	This state is activated when the device has transferred all of the data requested by the command or has encountered an error that causes the command to abort before completing the transfer of the requested data. When in this state, the device shall request that the Transport layer transmit a Register FIS with the register content as described in the command description in the ATA/ATAPI-6 standard and the I bit set to one.
Transition DDMAI2:1	When the FIS has been transmitted, the device shall transition to the DI0: Device_idle state.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.
Table 16 summarizes the Drive command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 16: ATA Command Set[1]

Command	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5h or 98h					D	
Execute Drive Diagnostic	90h					D	
Flush cache	E7h					D	
Flush cache Ext	EAh					D	
Identify Drive	ECh					D	
Idle	E3h or 97h		Y			D	
Idle Immediate	E1h or 95h					D	
NOP	00h					D	
Read Buffer	E4h					D	
Read DMA	C8h		Y	Y	Y	Y	Y
Read DMA Ext	25h		YY			D	YY
Read FPDMA Queued	60h	Y	Y	Y	Y	D	Y
Read Multiple	C4h		Y	Y	Y	Y	Y
Read Multiple Ext	29h		YY			D	YY
Read native max address	F8h					D	
Read native max address Ext	27h					D	
Read Sector(s)	20h		Y	Y	Y	Y	Y
Read Sector(s) Ext 2)	24h		YY	YY	YY	D	YY
Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
Read Verify Sector(s) Ext	42h		YY	YY	YY	D	YY
Security Disable Password	F6h					D	
Security Erase Prepare	F3h					D	
Security Erase Unit	F4h					D	
Security Freeze Lock	F5h					D	
Security Set Password	F1h					D	
Security Unlock	F2h					D	
Set Features	EFh	Y				D	
Set max address (with set password)	F9h		Y	Y	Y	Y	Y
Set max address Ext	37h		YY	YY	YY	D	YY
Set Multiple Mode	C6h		Y			D	
Sleep	E6h or 99h					D	
S.M.A.R.T.	B0h	Y	Y		Y	D	
Standby	E2h or 96h					D	
Standby Immediate	E0h or 94h					D	
Write Buffer	E8h					D	
Write DMA	CAh		Y	Y	Y	Y	Y
Write DMA Ext	35h		YY	YY	YY	D	YY
Write DMA FUA Ext	3Dh		YY	YY	YY	D	YY
Write FPDMA Queued	61h		Y	Y	Y	D	Y
Write Multiple	C5h		Y	Y	Y	Y	Y
Write Multiple Ext	39h		YY	YY	YY	D	YY
Write Multiple FUA Ext	CEh		YY	YY	YY	D	YY
Write Sector(s)	30h		Y	Y	Y	Y	Y
Write Sector(s) Ext	34h		YY	YY	YY	D	YY

1. FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers,
   DH = Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use),
   Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the Drive and head parameters are used.
   YY – registers must be written twice for 48bit LBA commands
   D – only the Drive parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).
2. To read out the higher and lower byte of the 16bit registers bit7 of the Device Control Register (write to Alternate status register) must be set to 1 or 0, respectively.

for details look at the SATA-8 specification e.g. draft here:
http://www.t13.org/documents/UploadedDocuments/docs2007/D1699r4a-ATA8-ACS.pdf

6.1 Check Power Mode (98h or E5h)

This command checks the power mode.
Issuing the command while the Drive is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.
Issuing the command when the Drive is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.
Table 17 defines the byte sequence of the Check Power Mode command.

Table 17: Check Power Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h or E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.2 Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Drive.
The Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.
Table 18 defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 19 are returned in the Error Register at the end of the command.

Table 18: Execute Drive Diagnostic

Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 19: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error

6.3 Flush Cache (E7h)

This command causes the drive to complete writing data from its cache. The drive returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the drive does not support the Flush Cache command, the drive shall return command aborted.

Table 20: Flush Cache

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E7h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.4 Flush Cache Ext (EAh) 48bit LBA

This command causes the SSD to complete writing data from its volatile cache into non-volatile memory. The BSY bit shall remain set to one until all data has been successfully written or an error occurs. The SSD returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the SSD does not support the Flush Cache Ext command, the SSD shall return command aborted. See Table 21 for the DATA SET MANAGEMENT command inputs.

Table 21: Flush cache Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	EAh							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	nu	nu							
LBA Mid	nu	nu							
LBA Low	nu	nu							
SECTOR COUNT	nu	nu							
FEATURES	nu	nu							

An unrecoverable error encountered while writing data results in aborting the command and the Command Block registers contain the 48 –bit sector address of the sector where the first unrecoverable error occurred. Subsequent FLUSH CACHE EXT commands continue the process of flushing the cache starting with the first sector after the sector in error.
This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

6.5 Identify Device (ECh)

The Identify Device command enables the host to receive parameter information from the Drive. This command has the same protocol as the Read Sector(s) command. Table 22 defines the Identify Device command Byte sequence. All reserved bits or Words are zero. shows the definition of each field in the Identify Drive Information.

Table 22: Identify Device

Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 23: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	**0040h***	2	Standard Configuration FIX
1	3fffh	2	Default number of cylinders (obsolete)
2	c837h*	2	specific configuration
3	0010h*	2	Default number of heads (obsolete)
4	0000h*	2	(retired)
5	0240h*	2	(retired)
6	003fh	2	Default number of sectors per track (obsolete)
7-8	0000h	4	reserved for CompactFlash
9	0000h	2	(retired)
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0000h	2	(retired)
21	0000h	2	(retired)
22	0004h*	2	(obsolete)
23-26	**YYYY***	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	**YYYY***	40	Model number in ASCII (right justified ("SFSAxxxxQxBJxxx-x-xx-xxx-xxx")
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Trusted computing feature set options
49	**0F00h***	2	Capabilities with DMA, LBA, IORDY supported
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode 2 (obsolete)
52	0000h	2	(obsolete)
53	**0007h***	2	Field validity (Bytes 54-58, 64-70, 88)
54	3fffh*	2	Current numbers of cylinders (obsolete)
55	0010h*	2	Current numbers of heads (obsolete)
56	003fh*	2	Current sectors per track (obsolete)
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW) (obsolete)
59	0101h*	2	Multiple sector setting (can be changed by host).
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	(obsolete)
63	**0007h***	2	Multi-Word DMA transfer support and selection (can be changed by host).
64	0003h	2	Advanced PIO modes 3 and 4 supported
65	0078h*	2	Minimum Multi-Word DMA transfer cycle time per Word.
66	0078h*	2	Recommended Multi-Word DMA transfer cycle time.
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69-74	XXXXh	12	Reserved
75	001fh*	2	Maximum queue depth - 1
76	0306h*	2	SATA Capabilities (power management, NCQ, SATA I & II)
77	0000h	2	Reserved
78	0048h*	2	SATA Feature support
79	0040h*	2	SATA Features enabled (can be changed by host)
80-81	03f0h 0000h	4	ATA/ATAPI version 8,7,6,5; Minor 0
82 -84	742Bh* 7501h* 4020h*	6	Features/command sets supported
85-87	7429h* 3401h* 4020h*	6	Features/command sets enabled (can change in operation)
88	**407F***	2	UDMA Mode Supported 0,1,2,3,4,5,6 and Selected 6 (changes in operation)
89	0003*	2	Time for security erase unit completion (e.g. 6 minutes)
90-91	0000h*	4	Time for security and enhanced erase completion
92	**FFFE***	2	Master Password Revision Code
93-99	0000h*	14	Reserved
100-103	XXXXh	8	Total Number of User Addressable Sectors for the 48-bit Address feature set.
104	0000h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
105	0100h*	2	Reserved
106-127	00x0h	44	Reserved
128	0021h*	2	Security Status (changes in operation)
129-159	XXXXh	62	Vendor specific (e.g."Swissbit SSD")
160	0000h*	2	Reserved (Max. current (CFA power mode))
161-208	0000h	96	Reserved
209	4000h*	2	Alignment of logical blocks within a larger physical block
210-216	0000h*	14	Reserved
217	0001h	2	Nominal media rotation rate (→SSD)
218-254	0000h	74	Reserved
255	xxa5h*	2	Integrity word

* Standard values for full functionality, depending on configuration, can change in operation
XXXX Depending on drive capacity and drive geometry
YYYY Depending on drive configuration

6.5.1 Word 0: General Configuration

This field indicates the general characteristics of the device.
The default value for Word 0 is set to **0040Ah**.
Some operating systems require Bit 6 of Word 0 to be set to '1' (Non-removable device) to use the drive as the root storage device.

6.5.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.5.3 Word2: Specific Configuration

C837h: Device does not require SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE data is complete.

6.5.4 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.5.5 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.5.6 Word 7-8: Number of Sectors per Drive

This field contains the number of sectors per Drive. This double Word value is also the first invalid address in LBA translation mode.

6.5.7 Word 10-19: Memory Drive Serial Number

The contents of this field are right justified and padded without spaces (20h).

6.5.8 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

6.5.9 Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.5.10 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

6.5.11 Word 49: Capabilities

- Bit 13 Standby Timer: is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.

- Bit 11: IORDY Supported
  If bit 11 is set to 1 then this drive supports IORDY operation.
  If bit 11 is set to 0 then this drive may support IORDY operation.
- Bit 10: IORDY may be disabled
  If bit 10 is set to 1 then IODRDY may be disabled.
- Bit 9 LBA support: drive support LBA mode addressing.
- Bit 8 DMA Support: Read/Write DMA commands are supported.

6.5.12 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2). Bits 15-8: are set to 02H.

6.5.13 Word 53: Translation Parameter Valid

- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid
- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid
- Bit 2 shall be set to 1 indicating that word 88 is valid and reflects the supported UDMA

6.5.14 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.5.15 Word 57-58: Current Capacity

This field contains the product of the current cylinders, heads and sectors.

6.5.16 Word 59: Multiple Sector Setting

- Bits 15-9 are reserved and must be set to '0'.
- Bit 8 is set to '1', to indicate that the Multiple Sector Setting is valid.
- Bits 7-0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are '00h' or '01h'.

6.5.17 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Drive in LBA mode only.

6.5.18 Word 63: Multi-Word DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the drive to indicate the multiword DMA mode which is currently selected.
Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.
Selection of Multiword DMA modes 3 and above are specific to Drive are as described in Word 163.
Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the drive to indicate the Multiword DMA modes it is capable of supporting.
Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the drive supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the drive supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the Drive supports Multiword DMA modes 2, 1 and 0.
Support for Multiword DMA modes 3 and above are specific to Drive are reported in word 163 as described in Word 163.

6.5.19 Word 64: Advanced PIO transfer modes supported

This field is bit significant. Any number of bits may be set to '1' in this field by the drive to indicate the advanced PIO modes it is capable of supporting.

- Bits 7-2 are reserved for future advanced PIO modes.
- Bit 1 is set to '1', indicates that the Drive supports PIO mode 4.

- Bit 0 is set to '1' to indicate that the Drive supports PIO mode 3.

Support for PIO modes 5 and above are specific to Drive are reported in word 163 as described in Word 163.

6.5.20 Word 65: Minimum Multi-Word DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.5.21 Word 66: Recommended Multi-Word DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the Drive will need to negate the DMARQ signal during the transfer of a sector.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

6.5.22 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer without utilization of flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.5.23 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the Drive supports while performing data transfers while utilizing IORDY flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the Drive.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

6.5.24 Word 75: Queue depth

Bits (4:0) of word 75 indicate the maximum queue depth supported by the device. The queue depth includes all commands for which command acceptance has occurred and command completion has not occurred. The value in this field equals (maximum queue depth - 1), e.g., a value of zero indicates a queue depth of one, a value of 31 indicates a queue depth of 32. If bit 1 of word 83 is cleared to zero indicating that the device does not support READ/WRITE DMA QUEUED commands, or if bit 6 of word 76 is cleared to zero indicating that the device does not support READ/WRITE FPDMA commands, the value in this field shall be zero. Support of this word is mandatory if the TCQ feature set is supported.

6.5.25 Word 76: Serial ATA Capabilities

- Bit 15:11 Reserved
- Bit 10 1 = Supports Phy Event Counters
- Bit 9 1 = Supports receipt of host initiated power management requests
- Bit 8 1 = Supports native Command Queuing
- Bit 7:3 Reserved for future SATA signaling speed grades
- Bit 2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s)
- Bit 1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s)
- Bit 0 Shall be cleared to zero

6.5.26 Word 78: SATA Feature support

- Bit 15-7 Reserved
- Bit 6 1 = Supports software settings preservation
- Bit 5 1 = Supports asynchronous notification
- Bit 4 1 = Supports in-order data delivery
- Bit 3 1 = Device supports initiating interface power managment
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization
- Bit 1 1 = Supports non-zero buffer offsets
- Bit 0 Shall be cleared to zero

6.5.27 Word 79: SATA Features enabled

- Bit 15-7 Reserved
- Bit 6 1 = Supports software settings preservation enabled
- Bit 5 1 = Supports asynchronous notification enabled
- Bit 4 1 = Supports in-order data delivery enabled
- Bit 3 1 = Device supports initiating interface power managment enabled
- Bit 2 1 = Supports DMA Setup Auto-Activate optimization enabled
- Bit 1 1 = Supports non-zero buffer offsets enabled
- Bit 0 Shall be cleared to zero

6.5.28 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.
- If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
- Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.
- If bit 5 of word 82 is set to one, write cache is supported.
- If bit 6 of word 82 is set to one, look-ahead is supported.
- Bit 7 of word 82 shall be set to zero; release interrupt is not supported.
- Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.
- Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 82 shall be set to one; the Host Protected Area feature set is supported.
- Bit 11 of word 82 is obsolete.
- Bit 12 of word 82 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 82 shall be set to one; the Drive supports the Read Buffer command.
- Bit 14 of word 82 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 82 is obsolete.

- Bit 0 of word 83 shall be set to one; the Drive supports the Download Microcode command.
- Bit 1 of word 83 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.
- Bit 2 of word 83 shall be set to zero; the Drive does not support the CFA feature set.
- If bit 3 of word 83 is set to one, the Drive supports the Advanced Power Management feature set.
- Bit 4 of word 83 shall be set to zero; the Drive does not support the Removable Media Status feature set.

6.5.29 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.
- If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security
- Set Password command.
- Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
- If bit 5 of word 85 is set to one, write cache is enabled.
- If bit 6 of word 85 is set to one, look-ahead is enabled.
- Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
- Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.
- Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 85 is obsolete.
- Bit 12 of word 85 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 85 shall be set to one; the Drive supports the Read Buffer command.
- Bit 14 of word 85 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 85 is obsolete.
- Bit 0 of word 86 shall be set to one; the Drive supports the Download Microcode command.
- Bit 1 of word 86 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.
- If bit 2 of word 86 shall be set to zero, the Drive does not support the CFA feature set.
- If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
- Bit 4 of word 86 shall be set to zero; the Drive does not support the Removable Media Status feature set.

6.5.30 Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported. Word 88 shall return a value of 0 if the device does not support UDMA.

- Bit 15: Reserved
- Bit 14: 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
- Bit 13: 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
- Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
- Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
- Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
- Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
- Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
- Bit 7: Reserved
- Bit 6: 1 = Ultra DMA mode 6 and below are supported. Bits 0-5 shall be set to 1.
- Bit 5: 1 = Ultra DMA mode 5 and below are supported. Bits 0-4 shall be set to 1.
- Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.
- Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.
- Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.
- Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
- Bit 0: 1 = Ultra DMA mode 0 is supported

6.5.31 Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the SECURITY ERASE UNIT command to complete. Support of this word is mandatory if the Security feature set is supported.
Required Time=(Value*2) minutes

6.5.32 Word 92: Master Password Revision Code

Word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision is not supported. Support of this word is mandatory if the Security feature set is supported.

6.5.33 Words 100-103: Total Number of User Addressable Sectors for the 48-bit Address feature set

Words 100-103 contain a value that is one greater than the maximum LBA in user accessible space when the 48-bit Addressing feature set is supported. The maximum value that shall be placed in this field is 0000_FFFF_FFFF_FFFFh. Support of these words is mandatory if the 48-bit Address feature set is supported.

6.5.34 Word 128: Security status

Support of this word is mandatory if the Security feature set is supported.

Bit 8 of word 128 indicates the security level. If security mode is enabled and the security level is high, bit 8 shall be cleared to zero. If security mode is enabled and the security level is maximum, bit 8 shall be set to one. When security mode is disabled, bit 8 shall be cleared to zero.

Bit 5 of word 128 indicates the Enhanced security erase unit feature is supported. If bit 5 is set to one, the Enhanced security erase unit feature set is supported.

Bit 4 of word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are command aborted until a power-on reset or hardware reset.

Bit 3 of word 128 indicates security frozen. If bit 3 is set to one, the security is frozen.

Bit 2 of word 128 indicates security locked. If bit 2 is set to one, the security is locked.

Bit 1 of word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.

Bit 0 of word 128 indicates the Security Mode feature set supported. If bit 0 is set to one, security is supported.

6.5.35 Word 209: Alignment of logical blocks within a physical block

Word 209 shall report the location of LBA0 within the first physical sector of the media. This bit is valid if the bit 13 of word 106 is set to 1 indicating Device has multiple sector per physical sector.

6.5.36 Word 217: Nominal Media Rotation Rate

Word 217 indicates the nominal media rotation rate of the device. 0001h indicating a Non-rotating media (SSD).

6.6 Idle (97h or E3h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification. Table 24 defines the Byte sequence of the Idle command.

Table 24: Idle

Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h or E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Timer Count (5ms increments)							
FEATURES	nu							

6.7 Idle Immediate (95h or E1h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 25 defines the Idle Immediate command Byte sequence.

Table 25: Idle Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h or E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.8 NOP (00h)

This command always fails with the Drive returning command aborted. Table 26 defines the Byte sequence of the NOP command.

Table 26: NOP

Task File Register	7	6	5	4	3	2	1	0
COMMAND	00h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.9 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the Drive's sector buffer. This command has the same protocol as the Read Sector(s) command. Table 27 defines the Read Buffer command Byte sequence.

Table 27: Read buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.10 Read DMA (C8h)

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the Drive sets BSY, puts all or part of the sector of data in the buffer. The Drive is then permitted, although not required, to set DRQ, clear BSY. The Drive asserts DMAREQ while data is available to be transferred. The Drive asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Drive using DMA. While DMAREQ is asserted by the Drive, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

Table 28: Read DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.11 Read DMA Ext (25h) 48bit LBA

This command uses DMA mode to read from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the SSD sets BSY, puts all or part of the sector of data in the buffer. The SSD is then permitted, although not required, to set DRQ, clear BSY. The SSD asserts DMARQ while data is available to be transferred. The SSD asserts DMARQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the SSD using DMA. While DMARQ is asserted by the SSD, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.
At command completion, the Command Block Registers contain the LBA of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The amount of data transferred is indeterminate.
When a Read DMA Ext command is received by the SSD and 8 bit transfer mode has been enabled by the Set Features command, the SSD shall return the Aborted error.

Table 29: Read DMA Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	25h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	15:8	7:0							
FEATURES	nu	nu							

6.12 Read FPDMA Queued (60h) (if NCQ feature set supported)

This command is mandatory for devices implementing the NCQ feature set (see feature set reference).
This command requests that data to be transferred from the device to the host.
When the Forced Unit Access (FUA) bit is set to one the device shall retrieve the data from the SSD regardless of whether the device holds the requested information in its volatile cache. If the device holds a modified copy of the requested data as a result of having volatile cached writes, the modified data shall be written to the non-volatile media before being retrieved from the non-volatile media as part of this operation. When the FUA bit is cleared to zero the data shall be retrieved either from the device's non-volatile media or cache.

Table 30: Read FPDMA queued

Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	61h							
DRIVE/HEAD	-	FUA	1	nu	0	nu			
CYLINDER HI	LBA (47:40)	LBA23:16							
CYLINDER LOW	LBA (39:32)	LBA15:8							
SECTOR NUM	LBA (31:24)	LBA7:0							
SECTOR COUNT	nu	NCQ Tag					nu		
FEATURES	The number of logical sectors to be transferred. A value of 0000h indicates that 65,536 logical sectors are to be transferred.								

For further details see the ATA8 specification.

6.13 Read Multiple (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many

full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.
Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer.
Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Table 31 defines the Read Multiple command Byte sequence.

Table 31: Read Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C4h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.14 Read Multiple Ext (29h) 48bit LBA

The Read Multiple Ext command performs similarly to the Read Sectors Ext command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.
Command execution is identical to the Read Sectors Ext operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where n = (sector count) modulo (block count).
If the Read Multiple Ext command is attempted before the Set Multiple Mode command has been executed, or when Read Multiple Ext command is disabled, the Read Multiple Ext operation is rejected with an Aborted Command error. Disk errors encountered during a Read Multiple Ext command are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.
Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the sector specified in the Sector Number Register.
At command completion, the Command Block Registers contain the LBA of the last sector read.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The flawed data is pending in the sector buffer.
Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

Table 32: Read Multiple Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	29h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	15:8	7:0							
FEATURES	nu	nu							

Note: This specification requires that SSDs support a multiple block count of 1 and permits larger values to be supported.

6.15 Read Native max address (F8h)

The Read Native max address command reads the max native address of the drive. It is related to the Host protected Area feature set. Table 33 defines the Read max native address command Byte sequence.

Table 33: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F8h							
DRIVE/HEAD	nu	LBA	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.
The native drive size is given in Drive/Head, Cyl Hi, Cyl Low and Sector num register as LBA value.

6.16 Read Native max address Ext (27h)

The Read Native max address Ext command reads the max native address of the drive. It is related to the Host protected Area feature set and 48-bit address feature set. Table 34 defines the Read max native address command Byte sequence.

Table 34: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	27h							
DRIVE/HEAD	nu	LBA	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.
The native drive size is given in 16bit LBA High, Mid and Low register as 48bit LBA value.
To read out the higher and lower byte of the 16bit registers bit7 of the Device Control Register (HOB=High Order Bit, write to Alternate status register) must be set to 1 or 0, respectively.

6.17 Read Sector(s) (20h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Drive sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer. Table 35 defines the Read Sector command Byte sequence.

Table 35: Read sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.18 Read Sectors Ext (24h) 48bit LBA

This command reads from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the specified LBA. When this command is issued and after each sector of data (except the last one) has been read by the host, the SSD sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.
At command completion, the Command Block Registers contain the LBA of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The flawed data is pending in the sector buffer.

Table 36: Read Multiple Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	24h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	15:8	7:0							
FEATURES	nu	nu							

6.19 Read Verify Sector(s) (40h or 41h)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Drive sets BSY. When the requested sectors have been verified, the Drive clears BSY and generates an interrupt.
If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 37 defines the Read Verify Sector command Byte sequence.

Table 37: Read Verify Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h or 41h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.20 Read Verify Ext (42h) 48bit LBA

This command is identical to the Read Sector(s) Ext command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the SSD sets BSY.
When the requested sectors have been verified, the SSD clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the LBA of the last sector verified.

If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the LBA of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 38: Read Multiple Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	42h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	15:8	7:0							
FEATURES	nu	nu							

6.21 Security Disable Password (F6h)

This command requests a transfer of a single sector of data from the host. Table 39 defines the content of this sector of information. If the password selected by word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 39: Security Disable Password

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F6h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 40: Security Password Data Content

Word	Content
0	Control word Bit 0: Identifier 0=compare User password 1=compare Master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

6.22 Security Erase Prepare (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable device erasing and unlocking. This command prevents accidental erase of the SSD.

Table 41: Security Erase Prepare

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F3h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.23 Security Erase Unit (F4h)

This command requests transfer of a single sector of data from the host. Table 43 defines the content of this sector of information. If the password does not match the password previously saved by the SSD, the SSD rejects the command with command aborted. The Security Erase Prepare command shall be completed immediately prior to the Security Erase Unit command. If the SSD receives a Security Erase Unit command without an immediately prior Security Erase Prepare command, the SSD aborts the Security Erase Unit command.

Table 42: Security Erase Unit

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F4h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 43: Security Erase Password and Parameter Data Content

Word	Content
0	Control word Bit 0: Identifier 0=compare User password 1=compare Master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

*) is the Enhance Erase option is supported (ATAID Word128 Bit5 = 1)

Enhanced erase Features if supported (see separate specification document)

6.24 Security Freeze Lock (F5h)

The Security Freeze Lock command sets the SSD to Frozen mode. After command completion, any other commands that update the SSD Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security Freeze Lock is issued when the SSD is in Frozen mode, the command executes and the SSD remains in Frozen mode. After command completion, the Sector Count Register shall be set to 0.
Commands disabled by Security Freeze Lock are:

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

If security mode feature set is not supported, this command shall be handled as Wear Level command.

Table 44: Security Freeze Lock

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.25 Security Set Password (F1h)

This command requests a transfer of a single sector of data from the host. Table 46 defines the content of the sector of information. The data transferred controls the function of this command.

Table 47 defines the interaction of the identifier and security level bits.

Table 45: Security Set Password

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F1h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 46: Security Set Password Data Content

Word	Content
0	Control word Bit 0: identifier 0=set User password 1=set Master password Bit 1-7: Reserved Bit 8: Security level 0=High 1=Maximum Bits 9-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

Table 47: Identifier and Security Level Bit Interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The SSD shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The SSD shall then be unlocked by only the User password. The Master password previously set is still stored in the SSD shall not be used to unlock the SSD.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

6.26 Security Unlock (F2h)

This command requests transfer of a single sector of data from the host. Table 40 defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in the maximum security level, then the unlock command shall be rejected. If the identifier bit is set to user, then the device compares the supplied password with the stored User password. If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when Security Unlock is issued and the device is locked. Once this counter reaches zero, the Security Unlock and Security Erase Unit commands are command aborted until after a power-on reset or a hardware reset is received. Security Unlock commands issued when the device is unlocked have no effect on the unlock counter.

Table 48: Security Unlock

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F2h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.27 Set Features (EFh)

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the SSD returns command aborted.

Table 49: Set Features

Task File Register	7	6	5	4	3	2	1	0
COMMAND	EFh							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Config							
FEATURES	Feature							

Table 50: Features Supported

Feature	Operation
01h/81h	Enable/Disable 8-bit data transfers.
02h/82h	Enable/Disable write cache.
03h	Set transfer mode based on value in Sector Count register.
05h/85h	Enable/Disable advance power management.
09h/89h	Enable/Disable extended power operations.
0Ah/8Ah	Enable/Disable power level 1 commands.
55h/AAh	Disable/Enable Read Look Ahead.
66h/CCh	Disable/Enable Power On Reset (POR) established of defaults at Soft Reset.
69h	NOP Accepted for backward compatibility.
96h	NOP Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows trade-off between current drawn and read/write speed.
BBh	4 bytes of data apply on Read/Write Long commands

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers.
Features 02h and 82h allow the host to enable or disable write cache in SSD that implement write cache. When the subcommand disable write cache is issued, the SSD shall initiate the sequence to flush cache to non-volatile memory before command completion.
Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For SSDs which support DMA, one DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Table 51: Transfer Mode Values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode(1)
Reserved	00010b	N/A
Multi-Word DMA mode	00100b	Mode(1)
Ultra DMA mode	01000b	Mode(1)
Reserved	1000b	N/A

(1)Mode = transfer mode number

If a SSD supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of "00000000b", it shall set its default PIO mode. If the value is "00000001b" and the SSD supports disabling of IORDY, then the SSD shall set its default PIO mode and disable IORDY. A SSD shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.
A SSD reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported. A SSD reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.
If an Ultra DMA mode is enabled, any previously enabled Multiword DMA mode shall be disabled by the device.
If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device.
Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of Feh.

Table 52 shows these values.

Table 52: Advanced power management levels

Level	Sector Count Value
Maximum performance	Feh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

In the current version the advanced power management levels are accepted, but don't influence performance and power consumption.
Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to Feh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.
Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.
Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the SSD with extended power as they require Power Level 1 to perform their full set of functions. Power Enhanced SSDs are required to power up and execute all supported commands and protocols in Power Level 0, their default feature shall be 8Ah: Disable Power Level 1 Commands. No commands are actually excluded for such SSDs in Power Level 0 because no commands require Power Level 1. Features 55h and BBh are the default features for the SSD; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.
Feature code 9Ah enables the host to configure the SSD to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the SSD should consume. For example, if the Sector Count register were set to 6, the SSD would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the SSD responds to the host with the range of values supported by the SSD. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The SSD shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.
Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

6.28 Set max address (F9h)

The Set max address command sets the max address of the drive. It is related to the Host protected Area feature set. Table 53 defines the Set max address command Byte sequence.

Table 53: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F8h							
DRIVE/HEAD	nu	LBA	nu	D	Set max LBA (27:24)			
CYLINDER HI	Set max LBA (23:16)							
CYLINDER LOW	Set max LBA (15:8)							
SECTOR NUM	Set max LBA (7:0)							
SECTOR COUNT	nu							VV
FEATURES	Feature							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.

Prerequisites
DRDY set to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.
VV =Value volatile. If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent nonvolatile maximum address value setting over power-up or hardware reset.

The set max address can be locked/unlocked and secured by password with following features:

Table 54: Set max features

Feature register	Command
00h	Obsolete
01h	SET MAX SET PASSWORD
02h	SET MAX LOCK
03h	SET MAX UNLOCK
04h	SET MAX FREEZE LOCK
05-FFh	Reserved

Typical use of the Set max address (F9h) and Read native max address (F8h) commands would be:

On reset
BIOS receives control after a system reset;

1. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
2. BIOS issues a SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
3. BIOS reads configuration data from the highest area on the disk;
4. BIOS issues a READ NATIVE MAX ADDRESS command followed by a SET MAX ADDRESS command to reset the device to the size of the file system.

On save to disk

1. BIOS receives control prior to shut down;
2. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
3. BIOS issues a volatile SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
4. Memory is copied to the reserved area;
5. Shut down completes;
6. On power-on or hardware reset the device max address returns to the last non-volatile setting.

These commands are intended for use only by system BIOS or other low-level boot time process.
Using these commands outside BIOS controlled boot or shutdown may result in damage to file systems on the device. Devices should return command aborted if a subsequent non-volatile SET MAX ADDRESS command is received after a power-on or hardware reset.

6.29 Set max address Ext (37h) 48bit LBA

The Set Max Address Ext command sets the max address of the drive in 48bit LBA mode. It is related to the Host protected Area feature set and 48bit feature set. Table 53 defines the Set max address command Byte sequence.

Table 55: Read native max address

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	37h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	nu	nu							VV
FEATURES	nu	nu							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.

Prerequisites
DRDY set to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.
VV =Value volatile. If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent nonvolatile maximum address value setting over power-up or hardware reset.
The output is the same as for Readout Native max address Ext (see 6.15 and 6.16)).

6.30 Set Multiple Mode (C6h)

This command enables the Drive to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the Drive sets BSY and checks the Sector Count Register.
If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains '0' when the command is issued, Read and Write Multiple commands are disabled. At power on the default mode is Read and Write Multiple disabled, unless it is disabled by a Set Feature command. Table 56 defines the Set Multiple Mode command Byte sequence.

Table 56: Set Multiple Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.31 Sleep (99h or E6)

This command causes the Drive to set BSY, enter the Sleep mode (which corresponds to the ATA 'Standby' Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command.
Table 57 defines the Standby command Byte sequence.

Table 57: Sleep

Task File Register	7	6	5	4	3	2	1	0
COMMAND	99h or E6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.32 S.M.A.R.T. (B0h)

The intent of self-monitoring, analysis, and reporting technology (the SMART feature set) is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in the IDENTIFY DEVICE data (Word 82 bit 0).

Table 58: S.M.A.R.T. Features

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	XXh							
FEATURES	Feature							

Details of S.M.A.R.T. features are described in Section 7.

6.33 Standby (96h or E2)

This command causes the Drive to set BSY, enter the Sleep mode (which corresponds to the ATA 'Standby' Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command. Table 59 defines the Standby command Byte sequence.

Table 59: Standby

Task File Register	7	6	5	4	3	2	1	0
COMMAND	96h or E2h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.34 Standby Immediate (94h or E0h)

This command causes the Drive to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.
Recovery from Sleep mode is accomplished by issuing another command.
Table 60 defines the Standby Immediate Byte sequence.

Table 60: Standby Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	94h or E0h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.35 Write Buffer (E8h)

The Write Buffer command enables the host to overwrite contents of the Drive's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes. Table 61 defines the Write Buffer command Byte sequence.

Table 61: Write Buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E8h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

6.36 Write DMA (CAh)

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the Drive sets BSY, puts all or part of the sector of data in the buffer. The Drive is then permitted, although not required, to set DRQ, clear BSY. The Drive asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Drive using DMA. While DMAREQ is asserted by the Drive, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector written. If an error occurs, the write terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.
When a Write DMA command is received by the Drive and 8 bit transfer mode has been enabled by the Set Features command, the Drive shall return the Aborted error.

Table 62: Write DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	CAh							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.37 Write DMA Ext (35h) 48bit LBA

This command uses DMA mode to write from 1 to 65536 sectors as specified in the Sector Count Register. A sector count of 0 requests 65536 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the SSD sets BSY, puts all or part of the sector of data in the buffer. The SSD is then permitted, although not required, to set DRQ, clear BSY. The SSD asserts DMARQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the SSD using the DMA protocol. While DMARQ is asserted by the SSD, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.
At command completion, the Command Block Registers contain the LBA of the last sector written. If an error occurs, the write terminates at the sector where the error occurred. The Command Block Registers contain the LBA of the sector where the error occurred. The amount of data transferred is indeterminate.
When a Write DMA command is received by the SSD and 8 bit transfer mode has been enabled by the Set Features command, the SSD shall return the Aborted error.

Table 63: Write DMA Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	35h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	15:8	7:0							
FEATURES	nu	nu							

6.38 Write DMA FUA Ext (3Dh) 48bit LBA

The WRITE DMA FUA EXT command provides the same function as the WRITE DMA EXT command except that regardless of whether write caching in the device is enabled or not, the user data shall be written to the media before ending status for the command is reported.

6.39 Write FPDMA Queued (61h) (if NCQ feature set supported)

This command is mandatory for devices implementing the NCQ feature set (see feature set reference).
This command causes data to be transferred from the host to the device.
When the Forced Unit Access (FUA) bit is set to one regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported. When the FUA bit is cleared to zero the device may return command completion before the data is written to the media.

Table 64: Write FPDMA queued

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	61h							
DRIVE/HEAD	-	FUA	1	nu	0	nu			
CYLINDER HI	LBA (47:40)	LBA23:16							
CYLINDER LOW	LBA (39:32)	LBA15:8							
SECTOR NUM	LBA (31:24)	LBA7:0							
SECTOR COUNT	nu	NCQ Tag					nu		
FEATURES	The number of logical sectors to be transferred. A value of 0000h indicates that 65,536 logical sectors are to be transferred.								

For further details see the ATA8 specification.

6.40 Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The Drive sets BSY within 400ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.
When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.
Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command. For example, each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.
Note: The current revision of the Drive only supports a block count of 1 as indicated in the Identify Drive Command information. The Write Multiple command is provided for compatibility with future products which may support a larger block count.
Table 65 defines the Write Multiple command Byte sequence.

Table 65: Write Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C5h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.41 Write Multiple Ext (39h) 48bit LBA

The Write Multiple Ext command is similar to the Write Multiple command, except that LBA addressing is mandatory, the LBA associated with this command is a 48 bit address, and the sector count field is a 16 bit field. The second (lower in the table) part of each 16 bit field can be written to or read from by setting the HOB bit of the Device Control Register to 1 before reading or writing the field. Reading or writing the task file shall reset the HOA bit to 0.
Error handling is similar to the Write Multiple command, except that the error sector address is always returned as a 48 bit address, and the sector count is a 16 bit number.

Table 66: Write Multiple Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	39h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	15:8	7:0							
FEATURES	nu	nu							

6.42 Write Multiple FUA Ext (CEh) 48bit LBA

The WRITE MULTIPLE FUA EXT command provides the same function as the WRITE MULTIPLE EXT command except that regardless of whether write caching in the device is enabled or not, the user data shall be written to the media before ending status for the command is reported.

6.43 Write Sector(s) (30h)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Drive sets BSY, sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.
For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector. Table 67 defines the Write Sector(s) command Byte sequence.

Table 67: Write Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	30h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

6.44 Write Sector(s) Ext (34h) 48bit LBA

This is the 48-bit address version of the Write Sector(s) command.
This command writes from 1 to 65,536 sectors as specified in the Sector Count Register. A sector count value of 0000h requests 65,536 sectors. The device shall interrupt for each DRQ block transferred.
If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the 48-bit LBA of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

Table 68: Write Sector(s) Ext

register write	previous	current							
Task File Register	15:8	7	6	5	4	3	2	1	0
COMMAND	-	34h							
DRIVE/HEAD	-	1	1	1	Drive	Reserved			
LBA High	LBA (47:40)	LBA (23:16)							
LBA Mid	LBA (39:32)	LBA (15:8)							
LBA Low	LBA (31:24)	LBA (7:0)							
SECTOR COUNT	15:8	7:0							
FEATURES	nu	nu							

7 S.M.A.R.T. Functionality

The SSD supports the following SMART commands, determined by the Feature Register value.

Table 69: S.M.A.R.T. Features Supported

Feature	Operation
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds (obsolete)
D2h	SMART Enable/Disable Autosave
D3h	SMART Save Attribute Values (obsolete)
D4h	SMART Execute OFF-LINE Immediate
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status

SMART commands with Feature Register values not mentioned in the above table are not supported, and will be aborted.

7.1 S.M.A.R.T. Enable / Disable operations

This command enables / disables access to the SMART capabilities of the SSD.
The state of SMART (enabled or disabled) is preserved across power cycles.

Table 70: S.M.A.R.T. Enable / Disable operations (Feature D8h / D9h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D8h / D9h							

7.2 S.M.A.R.T. Return Status

This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count attribute (typical 25% of original spare blocks) or the Erase Count attribute (typical 1%), the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

Table 71: S.M.A.R.T. return status (Feature DAh)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	DAh							

7.3 S.M.A.R.T. Enable / Disable Attribute Autosave

This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the SSD.

Table 72: S.M.A.R.T. Enable / Disable Attribute Autosave (Feature D2h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	F1h or 00h (enable or disable)							
FEATURES	D2h							

7.4 S.M.A.R.T. Save Attribute Values

This command causes the device to immediately save any updated attribute values to the device's non-volatile memory regardless of the state of the attribute autosave timer. Upon receipt of this command from the host, the device sets BSY, writes any updated attribute values to non-volatile memory, clears BSY, and asserts INTRQ. This command is effectively a no-operation command.

Table 73: S.M.A.R.T. Save Attribute Values (Feature D3h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	Nu							
SECTOR COUNT	nu							
FEATURES	D3h							

7.5 S.M.A.R.T. Execute OFF-LINE Immediate

This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the SSD.

Table 74: S.M.A.R.T. Execute OFF-LINE Immediate (Feature D4h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu (Subcommand specific)							
SECTOR COUNT	nu							
FEATURES	D4h							

7.6 S.M.A.R.T. Read data

This command returns one sector of SMART data.

Table 75: S.M.A.R.T. read data (Feature D0h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D0h							

The data structure returned is:

Table 76: S.M.A.R.T. Data Structure

Offset	Typ. Value	Description
0..1	0100h	SMART structure version
2..361	**30x12Bytes***	**Attribute entries 1 to 30 (12 bytes each, little endian, see below)**
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364..365	0000h	Total time in seconds to complete off-line data collection
366	00h	Vendor specific
367	00h	Off-line data collection capability (no off-line data collection)
368..369	0200h	SMART capabilities
370	00h	Error logging capability (no error logging)
371	00h	Vendor specific
372	01h	Short self-test routine recommended polling time
373	01h	Extended self-test routine recommended polling time
374	00h	Conveyance self-test routine recommended polling time
375..385	00h	Reserved
386..395	XX	Firmware Version/Date code (e.g. "20130517")
396...397	0000h	reserved
398..399	0000h	reserved
400...406	"SMI2250"	Controller
407...415	00h	vendor specific
416	00h	reserved
417		reserved
418...419	**XXXXh***	**Number of spare blocks (little endian)**
420...423	**XXXXXXXXh***	**Average Erase Count (little endian)**
424...510	00h	Vendor specific
511	**XXh***	**Data structure checksum**

* These fields changes during operation and give life time information.

There are 23 attributes that are defined in the SSD. These return their data in the attribute section of the SMART data, using a 12 byte data field. The Threshold values can be read out with the separate command (see Table 79).

Table 77: S.M.A.R.T. Attributes

ID	Description	Type	Value	Worst	Thresh	Raw Value
0x01 1	Raw_Read_Error_Rate	advisory	100	100	0	4bytes
0x05 5	Reallocated_Sector_Count	advisory	100	100	0	2bytes
0x09 9	Power-On Hours	advisory	100	100	0	4bytes
0x0C 12	Power_Cycle_Count	advisory	100	100	0	2bytes
0xA0 160	Uncorrectable Sector Count when read/write	advisory	100	100	0	4bytes
0xA1 161	Spare Block	pre-fail	100*)	100*)	25	4bytes
0xA3 163	Number of Initial Invalid Block	advisory	100	100	0	2bytes
0xA4 164	Total Erase Count	advisory	100	100	0	7bytes
0xA5 165	Maximum Erase Count	advisory	100	100	50	4bytes
0xA6 166	Minimum Erase Count	advisory	100	100	50	4bytes
0xA7 167	Average Erase Count	pre-fail	100*)	100*)	1	4bytes
0xA9 169	Power on UECC Count	advisory	100	100	0	6bytes
0xC0 192	Power-off Retract Count	advisory	100	100	0	2bytes
0xC2 194	Temperature (current, min, max)	advisory	100	100	0	2bytes
0xC3 195	Flash ECC Recovered	advisory	100	100	0	7bytes
0xC4 196	Reallocation Event Count (currently not implemented)	advisory	100	100	16	N/A
0xC6 198	Uncorrectable Sector Count Offline	advisory	100	100	50	4bytes
0xC7 199	UltraDMA CRC Error Count	advisory	100	100	50	2bytes
0xD7 215	TRIM Count	advisory	100	100	0	2bytes
0xF1 241	Total LBAs Written (lower 7 bytes)	advisory	100	100	0	7bytes
0xF2 242	Total LBAs Read (lower 7 bytes)	advisory	100	100	0	7bytes
0xF3 243	Total LBAs Written (upper 5 bytes)	advisory	100	100	0	5bytes
0xF4 244	Total LBAs Read (upper 5 bytes)	advisory	100	100	0	5bytes

*) Value and worst change in operation

7.6.1 Attribute Entries

This table shows the structure of the S.M.A.R.T. attribute entries in the S.M.A.R.T. data structure.

Table 78: Attribute Entry

Offset	Value	Description
0	xxh	Attribute ID – (see **Table 77**)
1..2	000Xh	Flags: X=0 advisory, X=1 Old age
3	64h	Attribute value. The value returned here is the minimum percentage of remaining value
4	64h	Worst value. The value returned here is the minimum percentage of remaining value
5..8	xxxxxxxxh	Raw value (little endian) vendor (detailed values dependent on the attribute)
9..11		reserved

7.6.2 S.M.A.R.T. Read Attribute Thresholds

This command returns one sector of SMART attribute thresholds.

Table 79: S.M.A.R.T. read data thresholds (Feature D1h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D1h							

The data structure returned is:

Table 80: S.M.A.R.T. Data Threshold Structure

Offset	Value	Description
0..1	0100h	SMART structure version
2..361		Attribute threshold entries 1 to 30 (12 bytes each)
362..379	00h	Reserved
380..510	00h	–
511	xxh	Data structure checksum

This table shows the structure of the S.M.A.R.T. attribute entries in the S.M.A.R.T. data structure.

Table 81: Attribute Threshold Entry

Offset	Value	Description
0	xxh	Attribute ID – (see **Table 77**)
1	xxh	Attribute Threshold (see **Table 77**)
2..11		reserved

8 Package mechanical

The SSD has 4 screw holes at the side and 4 at the bottom side.

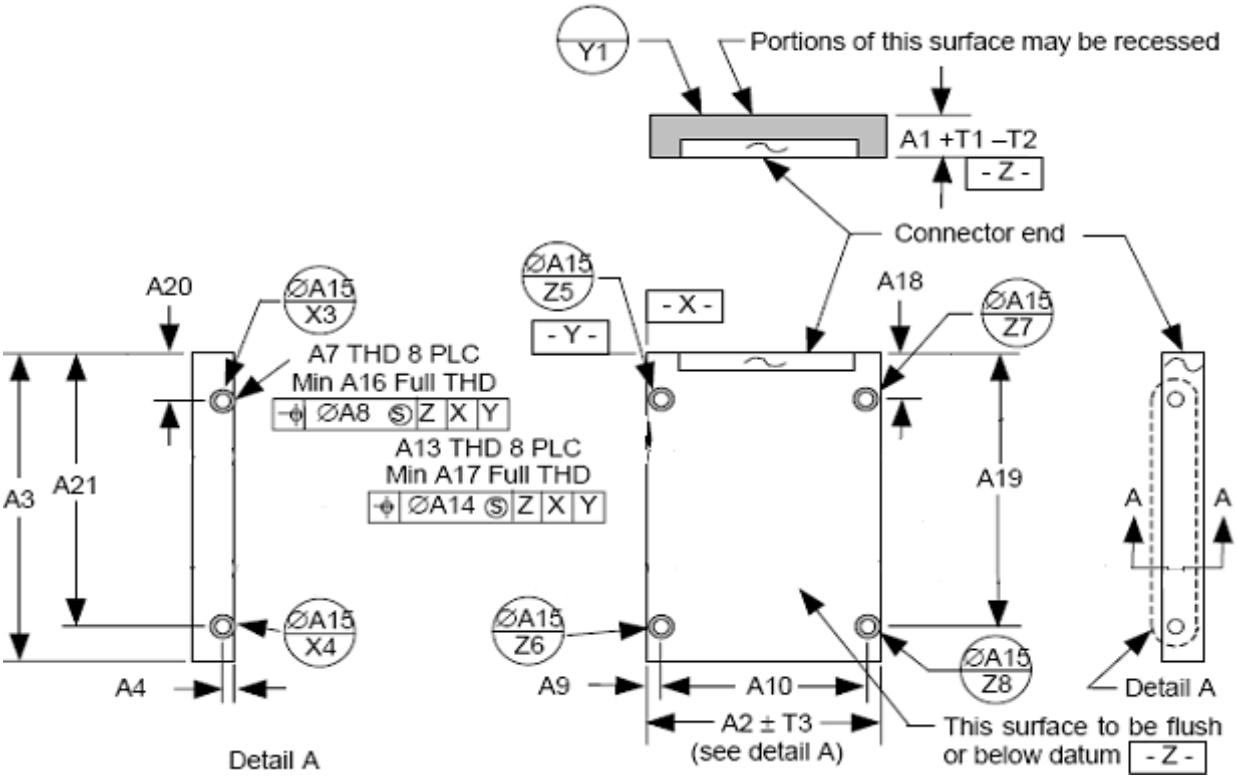


Figure 5: Housing dimensions

Dimension		mm	inches
Height	A1	9.2	0.362
Width	A2	69.85	2.752
Length	A3	100.10	3.94
Hole height	A4	3.0	0.118
	A7	n/a	n/a
	A8	0.5	0.02
Hole position	A9	4.1	0.16
Hole distance	A10	61.7	2.43
	A14	0.05	0.02
Screw head diameter	A15	6.0	0.315
Hole depth bottom	A16 min	5.0	0.2
Hole depth side	A17 min	5.0	0.2
1. hole	A18	14.0	0.551
4. hole	A19	90.6	3.567
1. hole	A20	14.0	0.551
4. hole	A21	90.6	3.567
+Height tolerance	T1	0.2	0.005
-Height tolerance	T2	0.2	0.01
Width tolerance	T3	0.2	0.01

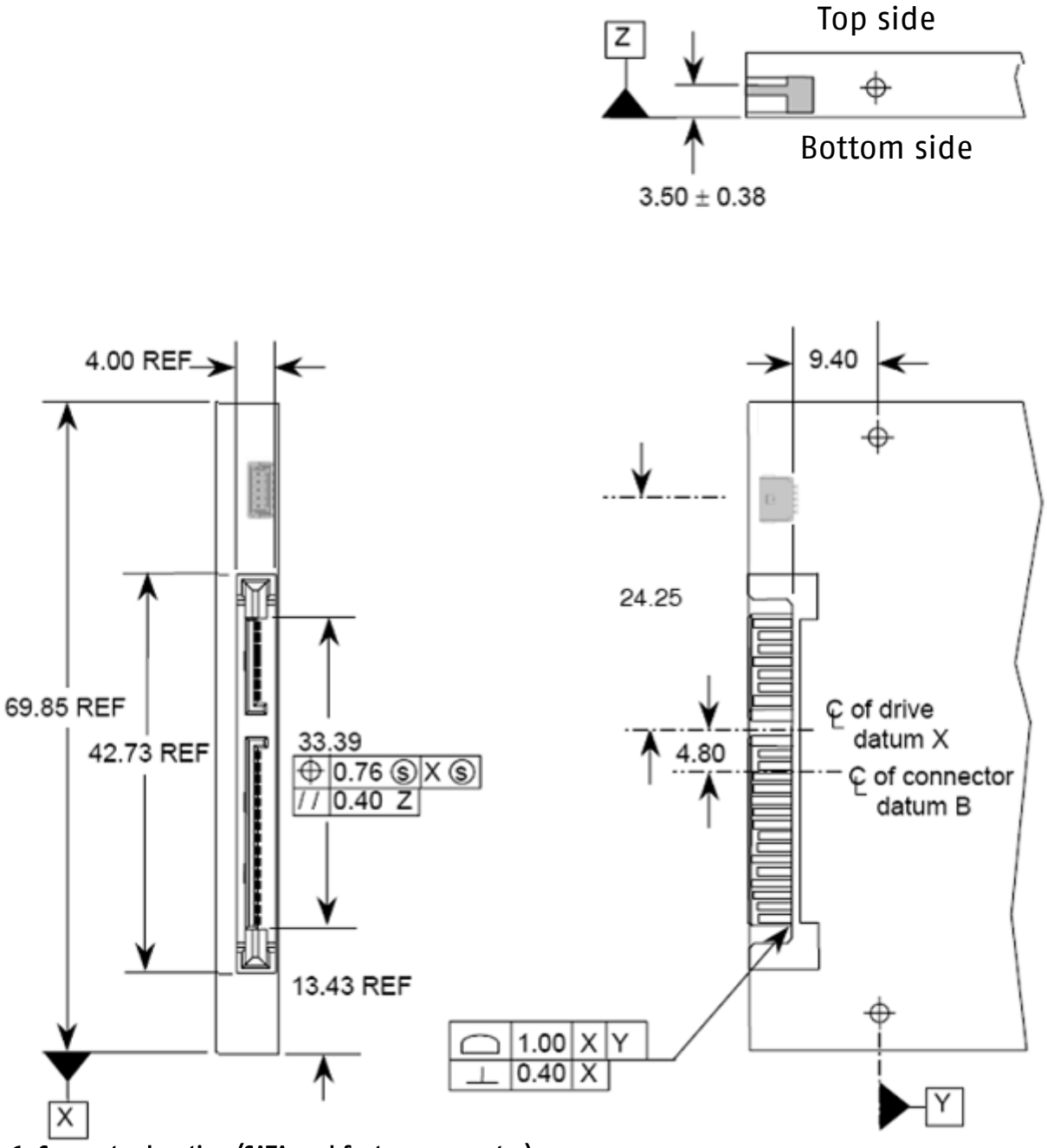


Figure 6: Connector location (SATA and feature connector)

9 CE Declaration of Conformity

We

Manufacturer: **Swissbit AG**
Industriestrasse 4
CH-9552 Bronschhofen
Switzerland

declare under our sole responsibility that the product

Product Type: **Solid State Drive (SSD)**
Brand Name: **SWISSMEMORY™**
Product Series: **X-55**
Part Number: **SFSAxxxxQxBJxxx-x-xx-xxx-xxx**

to which this declaration relates is in conformity with the following directives:

EN55022:2010
EN55024:2010
FCC47 Part 15:2009 Subpart B §15.111
CISPR 22 Ed6.0 2997-09 class B 30MHz-6GHz
EN 61000-4-2:2008
EN 61000-4-3:2010
EN 61000-6-2:2005
2002/96/EC Category 3 (WEEE)

following the provisions of Directive

Electromagnetic compatibility 2004/108/EC
Restriction of the use of certain hazardous substances 2011/65/EU

Swissbit AG, October 2013

Manuela Kögel
Head of Quality Management

10 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that Solid State Drives must comply with both Directives in order for them to be sold on the European market:

- RoHS – Restriction of Hazardous Substances
- WEEE – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2002/96/EC)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space.
«In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty»
(WEEE Directive 2002/96/EC)

When does the WEEE Directive take effect?

The Directive came into effect internationally on 13 August, 2005.

What is RoHS (2002/95/EC)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**
- **Checking the components and raw materials:**
  - Replacing non-RoHS-compliant components and raw materials in the supply chain
  - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit
- **Modifying the manufacturing processes and procedures**
  - Successfully adapting and optimizing the new management-free integration process in the supply chain
  - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials
- **Carrying out the quality process**
  - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of 1 July, 2006, only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

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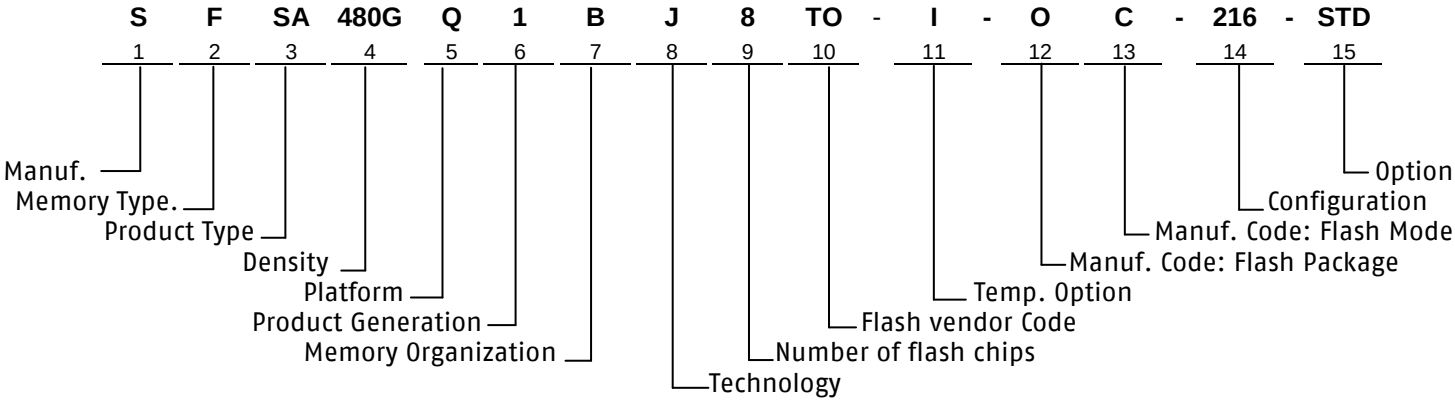
E-mail: industrial@swissbit.com – Website: www.swissbit.com

11 Part Number Decoder



11.1 Manufacturer

Swissbit code	S

11.2 Memory Type

Flash	F

11.3 Product Type

SATA-Interface	SA

11.4 Density

30 GByte	030G
60 GByte	060G
120 GByte	120G
240 GByte	240G
480 GByte	480G

11.5 Platform

SSD 2.5''	Q

11.6 Product Generation

11.7 Memory Organization

x8	B

11.8 Technology

X-5 Platform	J

11.9 Number of Flash Chip

4 Flash	4
8 Flash	8
16 Flash	A

11.10 Flash Code

Toshiba	T0

11.11 Temp. Option

Industrial Temp. Range -40°C – 85°C	I
Standard Temp. Range 0°C – 70°C	C

11.12 DIE Classification

	X-500 SLC	X-55 EM-MLC
MONO (single die package)	M	G
DDP (dual die package)	D	L
QDP (quad die package)	Q	H
ODP (octal die package)	N	O

11.13 PIN Mode

	TSOP	BGA
Single nCE & R/nB	S	A
Dual nCE & Dual R/nB	T	B
Quad nCE & Quad R/nB	U	C

11.14 Drive configuration XYZ

X→ Type

Drive Mode	PIO	DMA support	X
Fix	yes	yes	2

Y → Firmware Revision

FW Revision	Y
First	1
Second	2

Z → max. transfer mode

Max PIO Mode	Z
UDMA6 (MDMA2, PIO4)	6

11.15 Option

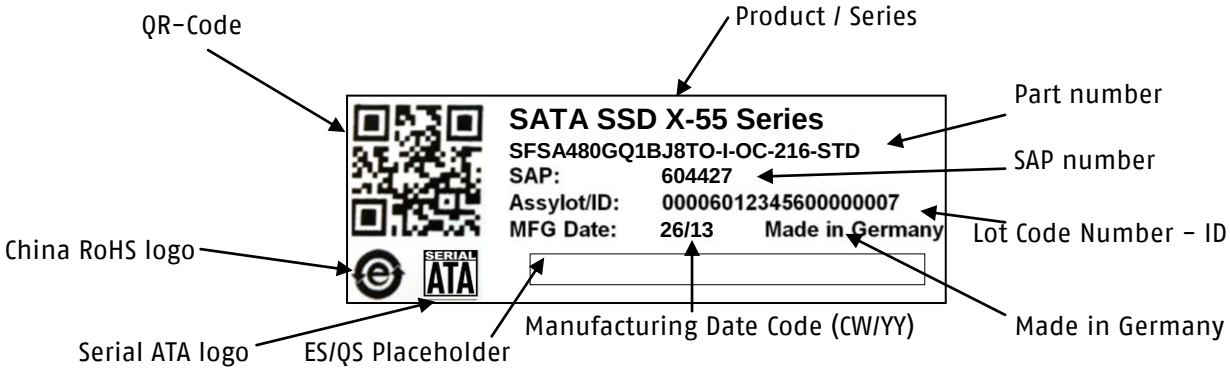
Swissbit / Standard	STD
Standard with conformal coating	STC
customer specific	xxx

12 Swissbit X-55 SSD Marking specification

12.1 Top view

connector side

12.1.1 Label content



Defined in the QR-Code:
SAP 6 digit-Assylot/ID 20 digit-MFG Date 4-digit
Example: 604427-00006012345600000007-2613

13 Revision History

Table 82: Document Revision History

Date	Revision	Revision Details
10-October-2013	1.00	First release
14-October-2013	1.01	TBW values updated and corrected (Table 11)

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