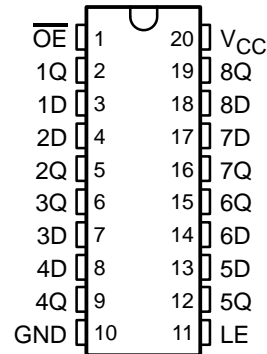


# CD54HC373, CD74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS452A – FEBRUARY 2001 – REVISED APRIL 2003

- 2-V to 6-V  $V_{CC}$  Operation
- Wide Operating Temperature Range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced Propagation Delays and Transition Times
- Standard Outputs Drive up to 15 LS-TTL Loads
- Significant Power Reduction Compared to LS-TTL Logic ICs

CD54HC373 . . . F PACKAGE  
CD74HC373 . . . E OR M PACKAGE  
(TOP VIEW)



## description/ordering information

The 'HC373 devices are octal transparent D-type latches designed for 2-V to 6-V  $V_{CC}$  operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	PDIP – E	Tube	CD74HC373E	CD74HC373E
	SOIC – M	Tube	CD74HC373M	HC373M
		Tape and reel	CD74HC373M96	
	CDIP – F	Tube	CD54HC373F3A	CD54HC373F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

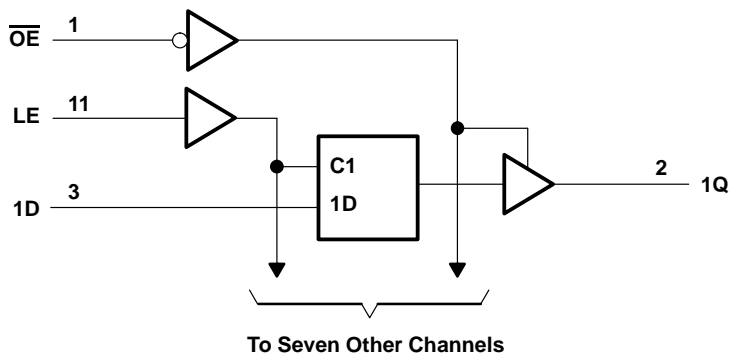
# CD54HC373, CD74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS452A – FEBRUARY 2001 – REVISED APRIL 2003

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output drain current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 35$ mA
Continuous output source or sink current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package	69°C/W
M package	58°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**CD54HC373, CD74HC373**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 4.5 V	3.15	
		V <sub>CC</sub> = 6 V	4.2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 4.5 V	1.35	
		V <sub>CC</sub> = 6 V	1.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
t <sub>t</sub>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	1000	ns
		V <sub>CC</sub> = 4.5 V	500	
		V <sub>CC</sub> = 6 V	400	
T <sub>A</sub>	Operating free-air temperature	-55	125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.9	1.9	V		
			4.5 V	4.4	4.4	4.4			
			6 V	5.9	5.9	5.9			
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	3.7	3.84			
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.2	5.34			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.1	0.1	0.1	V		
			4.5 V	0.1	0.1	0.1			
			6 V	0.1	0.1	0.1			
		I <sub>OL</sub> = 6 mA	4.5 V	0.26	0.4	0.33			
		I <sub>OL</sub> = 7.8 mA	6 V	0.26	0.4	0.33			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1	±1	±1	μA			
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0	6 V	±0.5	±10	±5	μA			
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V	8	160	80	μA			
C <sub>i</sub>			10	10	10	pF			
C <sub>o</sub>			20	20	20	pF			



**CD54HC373, CD74HC373**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$ Pulse duration, LE high	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
$t_{su}$ Setup time, data before LE↓	2 V	50		75		65		ns
	4.5 V	10		15		13		
	6 V	9		13		11		
$t_h$ Hold time, data after LE↓	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

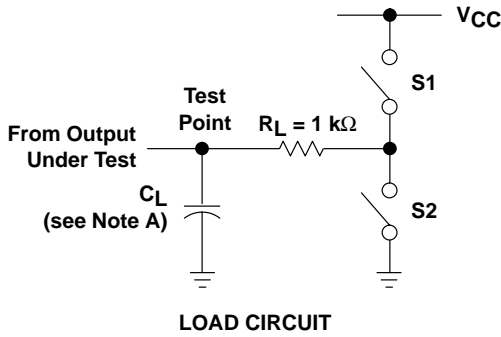
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
	LE	Q	$C_L = 50\text{ pF}$	2 V	175		265		220		
				4.5 V	35		53		44		
				6 V	30		45		37		
$t_{en}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
$t_{dis}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
$t_t$		Q	$C_L = 50\text{ pF}$	2 V	60		90		75	ns	
				4.5 V	12		18		15		
				6 V	10		15		13		

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

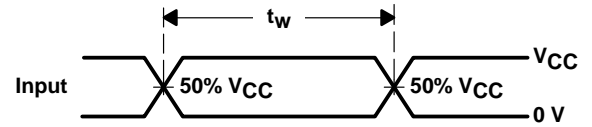
PARAMETER	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	51	pF



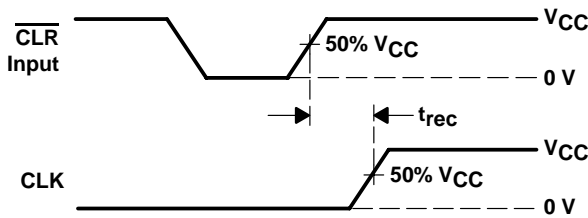
PARAMETER MEASUREMENT INFORMATION



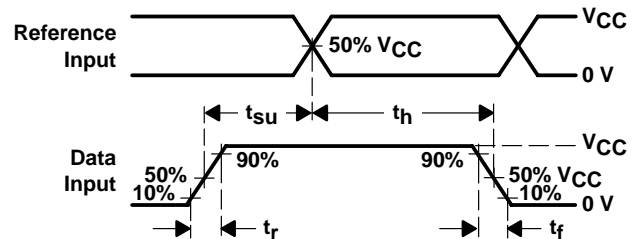
PARAMETER	S1	S2
$t_{en}$	tpZH	Open
	tpZL	Closed
$t_{dis}$	tpHZ	Open
	tpLZ	Closed
$t_{pd}$ or $t_t$	Open	Open



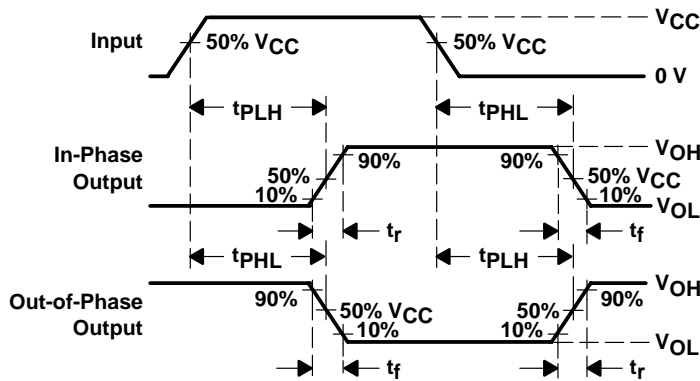
VOLTAGE WAVEFORMS  
 PULSE DURATION



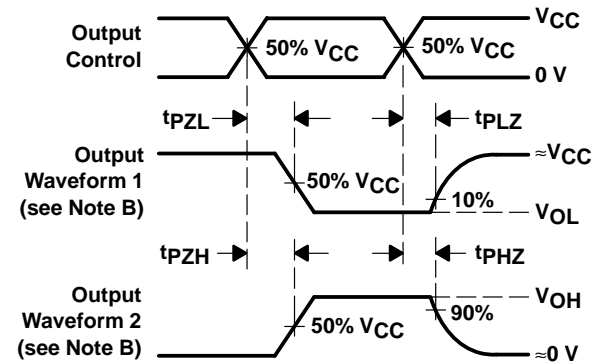
VOLTAGE WAVEFORMS  
 RECOVERY TIME



VOLTAGE WAVEFORMS  
 SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
 OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 6\text{ ns}$ ,  $t_f = 6\text{ ns}$ .  
 D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.  
 E. The outputs are measured one at a time with one input transition per measurement.  
 F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD54HC373F	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
CD54HC373F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
CD74HC373E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC373EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC373M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC373M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC373M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC373M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC373ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC373MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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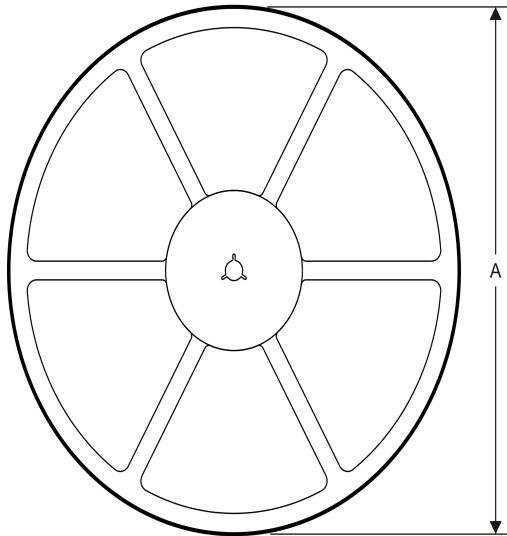
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**OTHER QUALIFIED VERSIONS OF CD54HC373, CD74HC373 :**

- Catalog: [CD74HC373](#)
- Military: [CD54HC373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC373M96	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

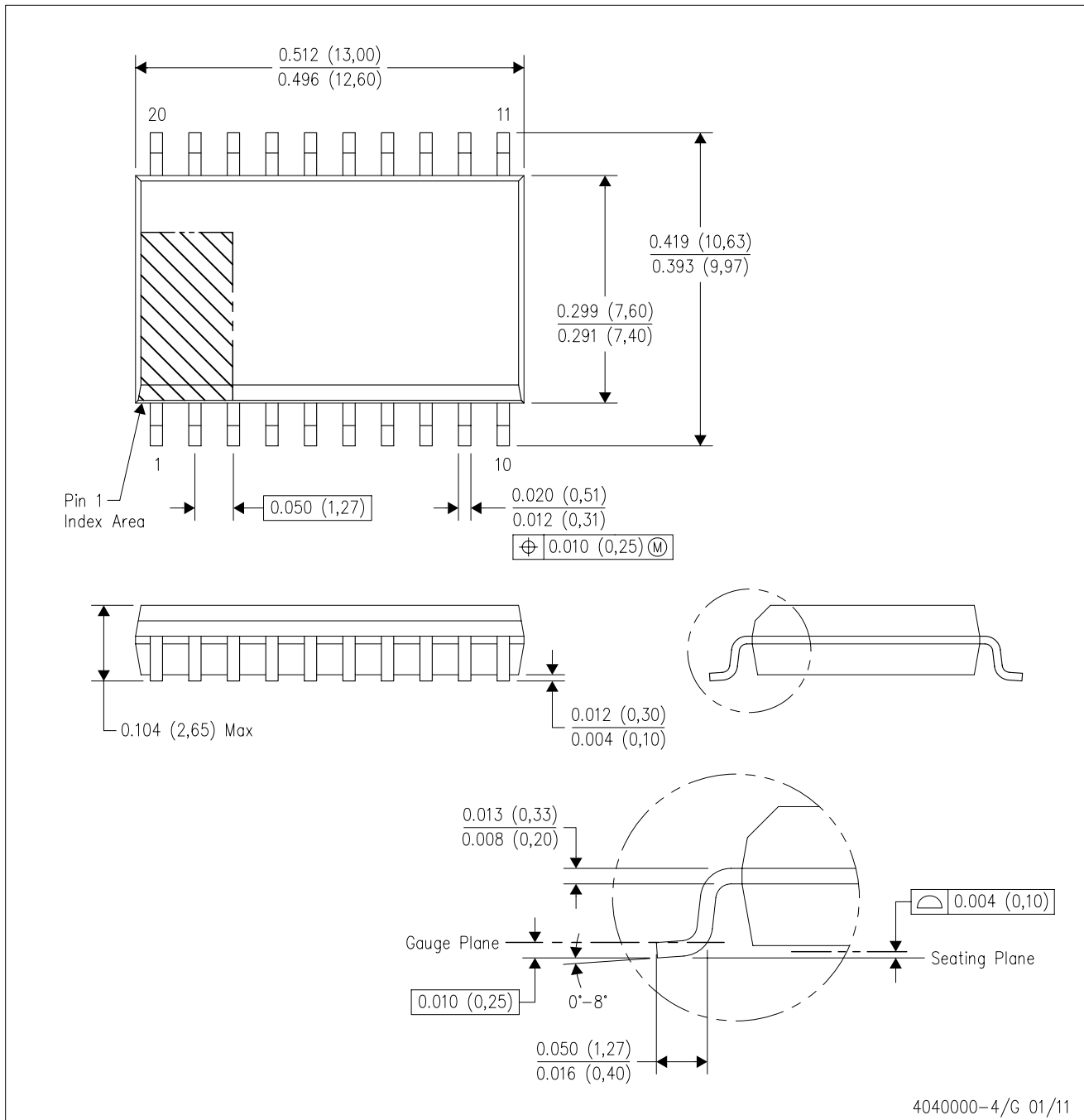
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

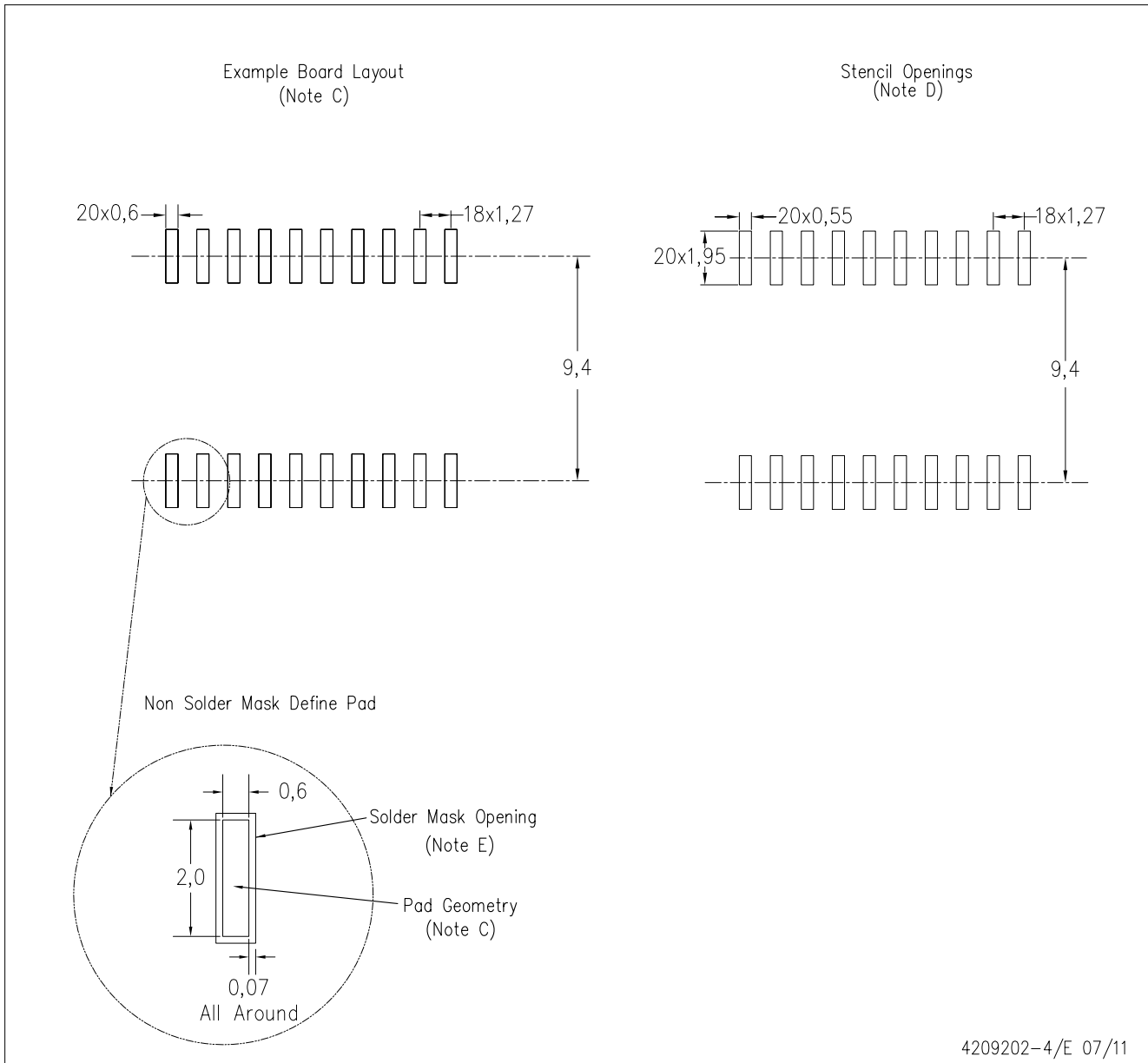
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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