TDA18219HN

Silicon Tuner for terrestrial and cable digital TV reception

Rev. 01 — 3 February 2010 Objective data sheet

1. General description

The TDA18219HN complies with most digital TV standards and delivers a LOW IF signal to a channel demodulator for digital TV. Standards that are covered include DVB-T, ISDB-T, DTMB and DVB-C.

The TDA18219HN facilitates design-ins as:

- Allowing easy on-board integration
- Drastically reducing the size of the tuner function
- Providing flexibility in system solution development

2. Features

- Fully integrated IF selectivity; eliminating the need for external SAW filters
- Fully integrated oscillators
- Alignment free
- Single 3.3 V supply voltage
- Low power consumption
- Integrated wideband gain control
- Crystal oscillator output buffer (16 MHz) for single crystal applications
- I^2C-bus interface compatible with 3.3 V microcontrollers
- Easy programming
- 5 ms tuning time
- LOW IF channel center frequency output ranging from 3 MHz to 5 MHz
- 1.7 MHz, 6 MHz, 7 MHz and 8 MHz channel bandwidths
- Loop-Through (LT)
- RoHS compliant

3. Applications

- Digital TV for STB, PCTV, DVD-R and TV applications
- Digital (DVB-T/C/H, DTMB, ISDB-T) worldwide standards supported
- Targeted specification (based on channel decoder or demodulator capabilities):
  - NorDig cable (EU)
  - C-BOOK conformance (Cable, EU)
  - NorDig 2.0 compliance (EU TV)
  - E-BOOK and D-BOOK compliances
  - ARIB STD-B21 for ISDB-T

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	full range of RF input	42	-	870	MHz
		center of channel	45	-	866	MHz
NF_{tun}	tuner noise figure	75 Ω source; maximum gain	-	5.0	5.9	dB
φ_{jit}	phase jitter	UHF; integrated from 1 kHz to 4 MHz	-	0.5	0.7	degree
α_{image}	image rejection	worst case for image rejection and 4 MHz IF frequency for levels above –50 dBm	57.5	63	-	dB
ICP_{1dB}	1 dB input compression point	at tuner input and minimum gain	124	-	-	dBμV

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA18219HN/C1	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

6. Marking

Table 3. Marking codes

Type number	Marking code
TDA18219HN/C1	18219HN

7. Block diagram

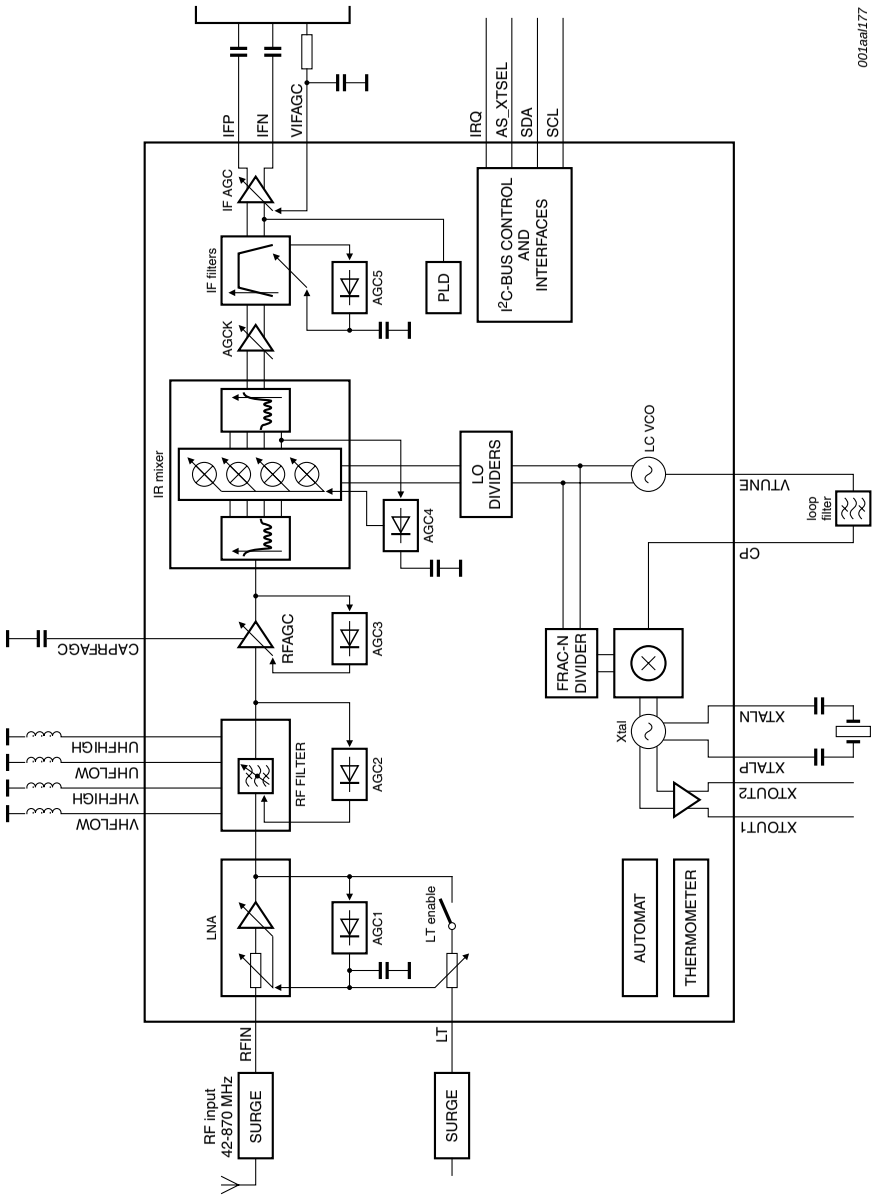


Fig 1. Block diagram

8. Pinning information

8.1 Pinning

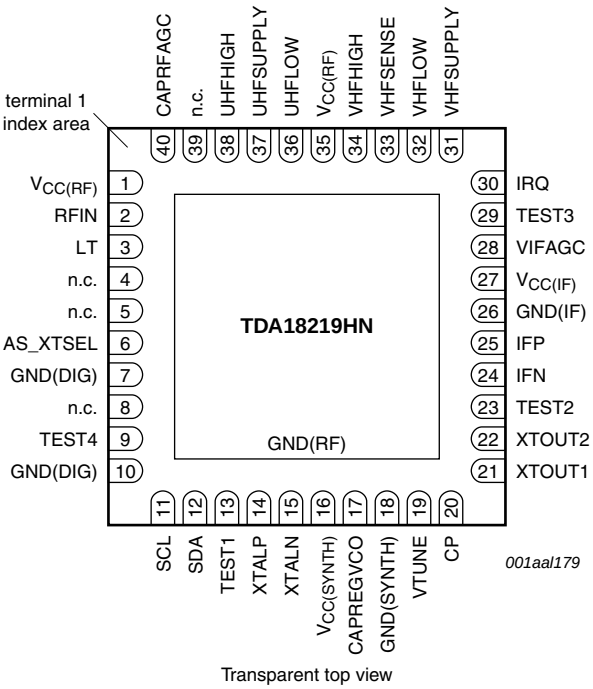


Fig 2. Pin configuration

8.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
$V_{CC(RF)}$	1	RF supply voltage
RFIN	2	unbalanced RF input
LT	3	loop-through output
n.c.	4	not connected
n.c.	5	not connected
AS_XTSEL	6	I^2C-bus address and XTOUT level selection input
GND(DIG)	7	digital ground supply voltage
n.c.	8	not connected
TEST4	9	test input 4, must be connected to ground
GND(DIG)	10	digital ground supply voltage
SCL	11	I^2C-bus clock input
SDA	12	I^2C-bus data input/output
TEST1	13	test input 1, must be connected to ground
XTALP	14	crystal oscillator positive input
XTALN	15	crystal oscillator negative input

Table 4. Pin description *...continued*

Symbol	Pin	Description
$V_{CC(SYNTH)}$	16	synthesizer supply voltage
CAPREGVCO	17	VCO regulator filtering input
GND(SYNTH)	18	synthesizer ground
VTUNE	19	VCO tuning voltage input
CP	20	charge pump output
XTOUT1	21	crystal oscillator buffer output 1
XTOUT2	22	crystal oscillator buffer output 2
TEST2	23	test input 2, must be connected to ground
IFN	24	IF negative output
IFP	25	IF positive output
GND(IF)	26	IF ground
$V_{CC(IF)}$	27	IF supply voltage
VIFAGC	28	IF gain control input
TEST3	29	test input 3, must be connected to ground
IRQ	30	interrupt request output
VHFSUPPLY	31	RF filter VHF supply input
VHFLOW	32	RF filter VHF LOW input
VHFSENSE	33	RF filter VHF sense
VHFHIGH	34	RF filter VHF HIGH input
$V_{CC(RF)}$	35	RF filter supply voltage
UHFLOW	36	RF filter UHF LOW input
UHFSUPPLY	37	RF filter UHF supply input
UHFHIGH	38	RF filter UHF HIGH input
n.c.	39	not connected
CAPRFAGC	40	RF AGC filtering
GND(RF)	die pad	RF ground

9. Functional description

The Silicon Tuner is based on single down-conversion and LOW IF architecture (LIF) that allows full integration of selectivity and eliminates the need for external SAW filters.

The RF input signal is fed to the input splitter, built-out of a Low Noise Amplifier (LNA). It is followed by an alignment free RF tuned filter to protect the rest of the tuner function against strong unwanted signals.

The LOW IF concept needs complex signals that highly suppress the N + 1 image channel thanks to image rejection calibration. The IF selectivity is performed by a complex filter and a IF filter which depends on IF frequency choice and channel bandwidth. The IF filter is built with a IF Low-Pass Filter (LPF), an IF notch filter which can be activated to suppress the residual adjacent N − 1 sound carrier and a programmable IF High-Pass Filter (HPF) for more flexibility on IF frequency.

Continuous gain control is performed after the RF filters and the IF selectivity. Stepped AGC is available at all stages (LNA, RF filter, mixer and IF LPF) in order to optimize the tuner signal-to-noise ratio. Gain settings of all stepped AGC and the RF AGC amplifier are controlled by internal broadband level detectors. The steps in the different stages are automatically compensated in IF with AGCK to keep a constant IF output level. The gain of the IF AGC amplifier is controlled by the demodulator to take advantage of the full ADC dynamic range.

A single LC-VCO operating at 7 GHz is used within a fractional-N phase lock-loop to generate the LO frequency.The clock reference signal is provided by a crystal oscillator and can be provided to a demodulator through the crystal output buffer.

All the programming is done via I^2C-bus transceiver. An embedded test tone generator is used for automatic calibration at power-on-reset.

The power level indicator can be used to indicate the RF input signal strengths of the received channel.

9.1 RF filter

The RF filter block is an alignment free tunable band-pass filter. After self calibration at power-on to compensate for external and internal components spread, the center frequency is automatically tuned to the desired frequency set via I^2C-bus to suppress the undesired interferers available on the broadband spectrum.

9.2 Crystal output mode

Pins XTOUT1 and XTOUT2 deliver a symmetrical sine waveform to drive the channel demodulator. The load on these outputs should be made identical to ensure optimum performance matching. Hence, if only one crystal output is used, the unused output must be loaded by the same capacitance. The XTOUT output level can be set to either 400 mV (p-p) or 800 mV (p-p) single ended.

9.3 AGC description

The tuner gain is composed of different variable gain stages spread according to block diagram. Using the different detectors at different stages, the gain is distributed to offer best linearity/noise compromise. The gain steps are 3 dB steps and in order to ensure gain continuity a specific stage called AGCK aims at compensating these internal steps to a minimum value. At the tuner output the gain variations appear to be continuous.

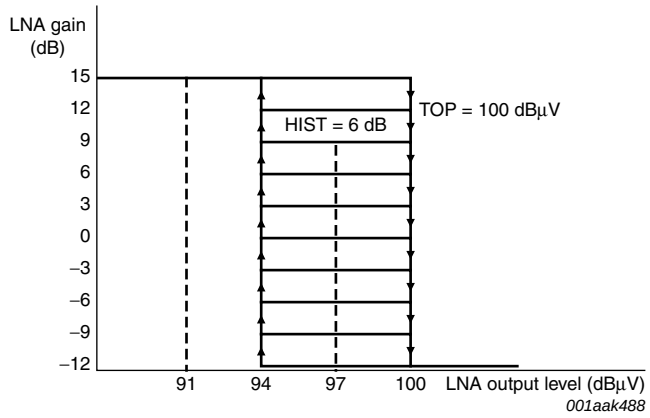
The tuner gain is externally controlled via IF AGC command (VIFAGC pin) provided to the tuner to make sure the following ADC are used full scale. The RF gain is set automatically, in accordance with the AGC TOP values.

The different stages gain values are then a combination of the following input parameters:

- Input signal
- TOP values set via I^2C-bus
- IFAGC command

In the circuit, the Take Over Point (TOP) are programmable to offer the optimal noise/linearity compromise during reception. The TOP are carefully selected not to overload following stages nor to have too weak signal to noise ratio. They correspond to decision points where the gain distribution changes inside the tuner.

In order to avoid instability of gain chain while working around level decision point a hysteresis has been implemented to avoid gain toggling. This is the reason why there are different values for TOP-up / TOP-down. Its main purpose is to make sure gain switch occurs to prevent signal distortion along the gain chain.



Remark: to get a 0 dB gain on the loop-through, then only steps from 6 dB to 15 dB are available.

Fig 3. AGC1 TOP description example

The TOP values are considered as tuner settings and could cause performances degradations if wrongly set.

Table 5. AGC number / block correspondence

AGC number	corresponding AGC block	comment
AGC1	LNA AGC	
AGC2	RF Filter AGC	Not described, handled internally by tuner
AGC3	RF AGC	
AGC4	Mixer AGC	
AGC5	LPF AGC	

9.4 Low-pass filter (LPF)

The programmable LPF avoids aliasing of demodulators Analog-to-Digital converters. In addition, it suppresses the remaining signals. The programming allows to receive signal bandwidth of 1.7 MHz, 6 MHz, 7 MHz and 8 MHz.

9.5 High-pass filter (HPF)

The HPF helps removing residual adjacent (N + 1) channel power after image rejection has been performed.

9.6 Notch filter

This block has been implemented in the IF filter to optionally provide additional robustness against adjacent analog channels. It reduces the adjacent channel sound carrier level to prevent overloading of IF output stage. The notch frequency is tracked with LPF settings.

9.7 IR mixer

The LOW IF concept needs complex signals that highly suppress the N + 1 image channel thanks to image rejection calibration.

9.8 LO generation

A single LC-VCO operating at 7 GHz is used within a fractional-N phase lock-loop to generate the LO frequency. The clock reference signal is provided by a crystal oscillator and can be provided to a demodulator through the crystal output buffer.

9.9 Thermometer

The thermometer can be used to indicate the junction temperature of the IC via I^2C-bus for soldering check. Refer to Section 10.1.2 for detailed description and operation.

9.10 Power Level Detector (PLD)

The power level indicator can be used to indicate the RF input signal strengths of the received channel via I^2C-bus. Refer to Section 10.1.4 for detailed description and operation.

9.11 I^2C-bus transceiver

The TDA18219HN is controlled via the two-wire I^2C-bus. For programming, there is one device address (7-bit) and the R/W bit for selecting read or write mode. To be able to have flexibility in the addresses within the I^2C-bus system, one of two possible addresses is selected depending on the voltage applied to address selection pin AS_XTSEL (pin 6) see Table 28 “Pin AS_XTSEL decoding”.

10. Control interface

10.1 Register table description

Table 6. Register table description

SubAdd	Name[1]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h	ID_byte_1	1	ident[14:8]						
01h	ID_byte_2	ident[7:0]							
02h	ID_byte_3	Major_rev[3:0]				Minor_rev[3:0]			
03h	Thermo_byte_1	-	TM_D[6:0]						
04h	Thermo_byte_2	-	-	-	-	-	-	-	TM_ON
05h	Power_state_byte_1	-	-	-	-	-	-	POR	LO_Lock
06h	Power_state_byte_2	-	-	-	-	SM	0	SM_LNA	SM_XT
07h	Input_Power_Level_byte	-	Power_Level[6:0]						
08h	IRQ_status	IRQ_status	-	-	-	-	-	-	-
09h	IRQ_enable	1	-	0	0	0	0	0	0
0Ah	IRQ_clear	IRQ_clear	-	0	0	0	0	0	0
0Bh	IRQ_set	0	-	0	0	0	0	0	0
0Ch	AGC1_byte_1	LT_Enable	AGC1_6_15dB	-	-	AGC1_TOP[3:0]			
0Dh	AGC2_byte_1	-	-	-	0	1	1	1	1
0Eh	AGCK_byte_1	0	0	1	1	0	0	1	0
0Fh	RF_AGC_byte_1	PD_RFAGC_Adapt	RFAGC_Adapt_TOP[1:0]		1	RF_Atten_3dB	AGC3_Top[2:0]		
10h	IR_MIXER_byte_1	-	-	-	-	AGC4_Top[3:0]			
11h	AGC5_byte_1	-	0	0	0	AGC5_Top[3:0]			
12h	IF_AGC_byte	-	-	-	-	-	IF_Level[2:0]		
13h	IF_byte_1	IF_HP_Fc[1:0]		IF_Notch	LP_FC_Offset[1:0]		LP_Fc[2:0]		
14h	Reference_byte	0	Digital_Clock	-	0	-	-	XTout[1:0]	
15h	IF_Frequency_byte	IF_Freq[7:0]							
16h	RF_Frequency_byte_1	-	-	-	-	RF_Freq[19:16]			
17h	RF_Frequency_byte_2	RF_Freq[15:8]							
18h	RF_Frequency_byte_3	RF_Freq[7:0]							

Table 6. Register table description *…continued*

SubAdd	Name[1]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
19h	MSM_byte_1	POWER_ Meas	RF_CAL_AV	RF_CAL	IR_CAL[1:0]		0	RC_CAL	Calc_PLL
1Ah	MSM_byte_2	-	-	-	-	-	-	0	MSM_Launch
1Bh	PSM_byte_1	1	1	VHFIII	1	1	1	1	1
1Ch	DCC_byte_1	0	0	0	0	-	-	-	-
1Dh	FLO_Max_byte	-	-	0	0	0	0	0	0
1Eh	IR_Cal_byte_1	0	0	0	0	0	0	0	0
1Fh	IR_Cal_byte_2	1	0	0	0	0	0	0	0
20h	IR_Cal_byte_3	-	-	-	0	0	0	0	0
21h	IR_Cal_byte_4	-	-	-	0	0	0	0	0
22h	Vsync_Mgt_byte	0	0	0	0	0	0	0	1
23h	IR_MIXER_byte_2	0	0	0	-	-	-	HI_Pass	DC_NOTCH
24h	AGC1_byte_2	0	0	0	0	1	0	0	1
25h	AGC5_byte_2	0	0	0	-	0	-	0	1
26h	RF_Cal_byte_1	0	0	0	0	0	0	0	0
27h	RF_Cal_byte_2	0	0	0	0	0	0	0	0
28h	RF_Cal_byte_3	0	0	0	0	0	0	0	0
29h	RF_Cal_byte_4	0	0	0	0	0	0	0	0
2Ah	RF_Cal_byte_5	0	0	0	0	0	0	0	0
2Bh	RF_Cal_byte_6	0	0	0	0	0	0	0	0
2Ch	RF_Filter_byte_1	0	0	0	0	1	0	1	1
2Dh	RF_Filter_byte_2	0	0	0	0	0	0	0	0
2Eh	RF_Filter_byte_3	0	0	0	0	0	0	0	0
2Fh	RF_Band_Pass_Filter_byte	0	-	-	-	-	1	1	0
30h	CP_Current_byte	-	1	0	0	0	1	1	1
31h	AGC_Det_Out_byte	X	X	X	X	X	X	X	X
32h	RF_AGC_Gain_byte_1	-	-	RF_FILTER_GAIN[1:0]		LNA_GAIN[3:0]			
33h	RF_AGC_Gain_byte_2	-	-	-	-	-	TOP_Agc3_read[2:0]		
34h	IF_AGC_Gain_byte	-	-	-	LPF_GAIN[1:0]		IR_MIXER[2:0]		
35h	Power_byte_1	X	X	X	X	X	X	X	X
36h	Power_byte_2	-	-	0	X	1	1	1	0

Table 6. Register table description *…continued*

SubAdd	Name[1]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
37h	Misc_byte_1	1	1	0	0	1	0	0	IRQ_Polarity
38h	rfcal_log_1	X	X	X	X	X	X	X	X
39h	rfcal_log_2	X	X	X	X	X	X	X	X
3Ah	rfcal_log_3	X	X	X	X	X	X	X	X
3Bh	rfcal_log_4	X	X	X	X	X	X	X	X
3Ch	rfcal_log_5	X	X	X	X	X	X	X	X
3Dh	rfcal_log_6	X	X	X	X	X	X	X	X
3Eh	rfcal_log_6	X	X	X	X	X	X	X	X
3Fh	rfcal_log_7	X	X	X	X	X	X	X	X
40h	rfcal_log_8	X	X	X	X	X	X	X	X
41h	rfcal_log_9	X	X	X	X	X	X	X	X
42h	rfcal_log_10	X	X	X	X	X	X	X	X
43h	rfcal_log_11	X	X	X	X	X	X	X	X
50h	FORBIDDEN ACCESS								
67h									
FEh	FORBIDDEN ACCESS								
FFh									

[1] The settings optimization is bound to channel decoder or demodulator choice and has a high impact on the tuner performances within system environment. Refer to Application Note *AN1002* for optimal settings.

Remark:

- The values in Table 6 must be written as described for normal operation of the tuner
- X means the value is provided by tuner and can be 0 or 1. Do not overwrite
- - means the value is undefined. No internal bit corresponds to this address.

10.1.1 Device type address ID

Table 7. ID byte bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
00h	ID_byte_1	6 to 0	Ident[14:8]	R	4724h	type number information
01h	ID_byte_2	7 to 0	Ident[7:0]			
02h	ID_byte_3	7 to 4	Major_rev[3:0]	R		major releases; current = 1
		3 to 0	Minor_rev[3:0]	R		minor releases; current = 1

10.1.2 Temperature sensor

Table 8. Temperature sensor bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
03h	Thermo_byte_1	6 to 0	TM_D[6:0]	R	-	a junction temperature measurement ranging from 22 °C to 127 °C is indicated through these bits
04h	Thermo_byte_2	0	TM_ON	W		temperature sensor ON or OFF
					0	temperature sensor switched off
					1	temperature sensor switched on

Remark: The thermometer value is updated each time a read is performed on the byte Thermo_byte_1, if TM_ON is set to 1. Otherwise, temperature value is not updated.

10.1.3 Power state

Table 9. Power state bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
05h	Power_state_byte_1	1	POR	R	-	detects when the tuner supply voltage went below POR threshold voltage. The tuner is then reset to its original settings (tuner not initialized).
					0	once it has been read
					1	the POR occurred on the tuner
		0	LO_Lock	R		LO lock flag
					0	PLL unlocked
					1	PLL locked
06h	Power_state_byte_2	0	SM_XT	R/W	see Table 10	
		1	SM_LNA	R/W	see Table 10	
		3	SM	R/W	see Table 10	

Table 10. Mode selection

SM[1]	SM_LNA[1]	SM_XT[1]	Mode
0	0	0	Normal mode = ON
1	0	0	Standby mode with LT ON and XTOUT ON

Table 10. Mode selection *...continued*

SM[1]	SM_LNA[1]	SM_XT[1]	Mode
1	0	1	Standby mode with LT ON and XTOUT OFF
1	1	0	Standby mode with LT OFF and XTOUT ON
1	1	1	Standby mode with LT OFF and XTOUT OFF

[1] All others values are forbidden.

10.1.4 Power level detector

Table 11. Power level detector bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
07h	Input_Power_Level_byte	6 to 0	Power_Level[6:0]	R	-	The power value is in the range from 40 dBμV (RMS) to 110 dBμV (RMS). Outside this range, Power_Level value[1] is computed as follows: • power < 40 dBμV (RMS): Power_Level = 0 • power > 110 dBμV (RMS): Power_Level = 127

[1] Power_Level value is updated only if requested via triggering of MSM_byte_1 and MSM_byte_2.

Remark: The power level measurement is not done continuously but only on request performed by using bytes MSM_byte_1 (19h) and MSM_byte_2 (1Ah):

- Set MSM_byte_1 to 80h to indicate a power measurement is required
- Trigger the measurement by writing 01h in MSM_byte_2
- Then read byte Input_Power_Level_byte (07h) for result

Remark: This feature purpose is to ease antenna pointing when no picture is displayed on screen only. In case a power level detection is required while displaying a picture, refer to software procedure described in application note.

10.1.5 IRQ

Table 12. IRQ bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
08h	IRQ_status	7	IRQ_status	R/W		
					0	IRQ_clear is set to 1
					1	all calibration sequences selected by MSM_byte_1 and launched by MSM_byte_2 are completed
0Ah	IRQ_clear	7	IRQ_clear	R/W		
					0	
					1	drops the bit IRQ_status

Remark: An IRQ information is generated on IRQ pin (30) that reflects the IRQ_status bit. The polarity of the pin can be selected with IRQ_Polarity bit at address 0x37h. In Normal mode of operation, the IRQ status is then raised at the end of the calibration sequence selected via MSM_byte_1 and MSM_byte_2 and at each new channel.

10.1.6 AGC and Take Over Points (TOP)

Table 13. AGC and Take Over Points bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	AGC1_byte_1	7	LT_Enable	R/W		LT output
					0	disable
					1	enable
		6	AGC1_6_15dB	R/W		limits AGC1 gain range from +6 dB to +15 dB
					0	range is from –12 dB to +15 dB
					1	range is from +6 dB to +15 dB
		3 to 0	AGC1_TOP[3:0]	R/W	see Table 14	set the TOP of the LNA detection loop (AGC1) in accordance with the reception standard or the system settings.
0Fh	RF_AGC_byte_1	7	PD_RFAGC_Adapt	R/W		RF AGC adapts algorithm power-down
					0	ON
					1	OFF
		6 to 5	RFAGC_Adapt_TOP[1:0]	R/W	-	“AGC3 Adapt” algorithm decreases the AGC3 TOP for low LPF gains. LPF gain is put to low value by AGC5 detector loop in the ACI (N) and (N – 1) reception cases. Decreasing the AGC3 TOP then limits signal C / N (Carrier / Noise) degradation caused by distortion in the RF stages. At opposite, LPF gain is put to high value by AGC5 detector loop in the ACI (N – X) and (N + X) reception cases. Increasing the AGC3 TOP then limits signal C / N degradation caused by noise from RF AGC stage. PD_RFAGC_Adapt allows disabling this algorithm. RFAGC_Adapt_TOP allows choosing the low AGC3 TOP value, the high one being chosen via the AGC3 TOP field.
		3	RF_Atten_3dB	R/W		Adds 3 dB attenuation out of RF AGC
					0	OFF
					1	ON
		2 to 0	AGC3_TOP[2:0]	R/W	see Table 15	sets the RF AGC, MIXER and LPF blocks TOP. These bits must be set according to the desired reception standard and required desired performances
10h	IR_MIXER_byte_1	3 to 0	AGC4_TOP[3:0]	R/W	see Table 16	
11h	AGC5_byte_1	3 to 0	AGC5_TOP[3:0]	R/W	see Table 17	
12h	IF_AGC_byte	2 to 0	IF_Level[2:0]	R/W	see Table 18	sets the tuner desired maximum output level. This will enable internal computation of the best linearity/noise compromise based on desired output level

Table 14. AGC1 TOP values

AGC1_TOP[3:0] (dec)[1]	AGC1 TOP Down (dBμV)	AGC1 TOP Up (dBμV)
0	95	89
5	99	93
10	100	94
15	101	95

[1] All others values are forbidden.

Table 15. AGC3 TOP values

AGC3_TOP[2:0] (dec)	AGC3 TOP (dBμV)
0	94
1	96
2	98
3	100
4	102
5	104
6	106
7	107

Table 16. AGC4 TOP values

AGC4_TOP[3:0] (dec)[1]	AGC4 TOP Down (dBμV)	AGC4 TOP Up (dBμV)
1	105	100
4	107	102
6	108	103
8	109	104
11	110	105
14	112	107

[1] All others values are forbidden.

Table 17. AGC5 TOP values

AGC5_TOP[3:0] (dec)[1]	AGC5 TOP Down (dBμV)	AGC5 TOP Up (dBμV)
1	105	100
4	107	102
6	108	103
8	109	104
11	110	105
14	112	107

[1] All others values are forbidden.

Table 18. Tuner output level

IF_Level[2:0] (hex)	Output level (V (p-p) differential)[1])	Minimum gain (dB)	Maximum gain (dB)
111	0.5	−12	18
110	0.6	−10.3	19.7
101	0.7	−9	21
100	0.85	−7.5	22.5
011	0.8	−8	22
010	1	−6	24
001	1.25	−4	26
000	2	0	30

[1] Output level depends on standard and ADC headroom

10.1.7 IF Filtering

Table 19. IF Filtering bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
13h	IF_byte_1	7 to 6	IF_HP_Fc[1:0]	R/W		tunes the IF HPF cut-off frequency. The high-pass frequency must be set in accordance with the desired reception standard.
						high-pass frequency:
					00	0.4 MHz
					01	0.85 MHz
					10	1 MHz
					11	1.5 MHz
		5	IF_Notch	R/W		enables or disables a notch implemented for adjacent N − 1 sound carrier suppression. The notch frequency depends on LP_Fc.
					0	OFF
					1	ON
		4 to 3	LP_FC_Offset[1:0]	R/W		enables offset to LPF cut-off frequency providing further adjacent channel rejection
					00	0
					01	−4 %
					10	−8 %
					11	forbidden
		2 to 0	LP_Fc[2:0]	R/W		selects the IF LPF cut-off frequency. It must be set according to desired reception standard.
						LP cut-off frequency: IF notch frequency
					100	1.7 MHz -
					000	6 MHz 6.5 MHz
					001	7 MHz 7.25 MHz
					010	8 MHz 8.25 MHz
					011	forbidden forbidden
					101	forbidden forbidden
					11x	forbidden forbidden

10.1.8 XTOUT

Table 20. XTOUT bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
14h	Reference_byte	1 to 0	XTout[1:0]	R/W		provides 16 MHz reference signal on the XTOUT1, XTOUT2 pins.
						XTOUT mode:
					00	no signal
					01	forbidden
					10	forbidden
					11	16 MHz
		6	Digital_Clock	R/W		spreads digital clock power to improve tuner EMC behavior
					0	OFF
					1	ON

10.1.9 IF and RF frequency

Table 21. IF and RF frequency bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
15h	IF_Frequency_byte	7 to 0	IF_Freq[7:0]	R/W	-	sets the tuner desired IF frequency by 50 kHz steps. For example, to set the IF frequency to 4 MHz, IF_Freq value must be 4000/50 = 80.
16h	RF_Frequency_byte_1	3 to 0	RF_Freq[19:16]	R/W	-	sets the desired RF frequency expressed in kHz
17h	RF_Frequency_byte_2	7 to 0	RF_Freq[15:8]			
18h	RF_Frequency_byte_3	7 to 0	RF_Freq[7:0]			

10.1.10 Calibration controls

Table 22. Calibration control bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
19h	MSM_byte_1	7	POWER_Meas	R/W	-	these bits are used to control the calibration and calculation automats embedded in the chip and must be used according to the programming flowchart Figure 4
		6	RF_CAL_AV	R/W	-	
		5	RF_CAL	R/W	-	
		4 to 3	IR_CAL[1:0]	R/W	-	
		1	RC_CAL	R/W	-	
		0	Calc_PLL	R/W	-	
1Ah	MSM_byte_2	0	MSM_Launch	R/W	-	

10.1.11 IF filtering options

Table 23. IR Mixer bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
23h	IR_Mixer_byte_2	1	HI_Pass	R/W	-	enables the high-pass frequency filter.
		0	DC_NOTCH	R/W		controls a DC notch in the IR mixer
					0	OFF
					1	ON

10.1.12 Gain values

Table 24. AGC bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
32h	RF_AGC_Gain_byte_1	5 to 4	RF_FILTER_GAIN[1:0]	R		RF FILTER gain value
					00	−11 dB
					01	−8 dB
					10	−5 dB
					11	−2 dB
		3 to 0	LNA_GAIN[3:0]	R	[1]	LNA gain value
					0000	−12 dB
					0001	−9 dB
					0010	−6 dB
					0011	−3 dB
					0100	0 dB
					0101	3 dB
					0110	6 dB
					0111	9 dB
					1000	12 dB
					1001	15 dB
33h	RF_AGC_Gain_byte_2	2 to 0	TOP_Agc3_read[2:0]	R		gives the TOP_AGC3 value
					000	94 dBµVrms
					001	96 dBµVrms
					010	98 dBµVrms
					011	100 dBµVrms
					100	102 dBµVrms
					101	104 dBµVrms
					110	106 dBµVrms
					111	107 dBµVrms
34h	IF_AGC_Gain_byte	4 to 3	LPF_GAIN[1:0]	R		LPF gain value
					00	0 dB
					01	3 dB
					10	6 dB
					11	9 dB
		2 to 0	IR_MIXER[2:0]	R	[1]	IR MIXER gain value
					000	2 dB
					001	5 dB
					010	8 dB
					011	11 dB
					100	14 dB

[1] Other values are forbidden.

10.1.13 IRQ polarity

Table 25. IRQ polarity bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
37h	Misc_byte_1	0	IRQ_Polarity	R/W		selects the IRQ pin polarity
						IRQ pin output voltage when IRQ raised:
					0	V_{CC}
					1	0

10.1.14 rfcal_log

These bytes are providing the outcome of the RF filter calibration. It can be used as an indicator regarding RF filter robustness implementation on PCB.

Table 26. rfcal_log bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
38h	rfcal_log1	7 to 0		R	-	provides RF filter calibration results according to the following convention: • Bit [7] is set to 1 in case of calibration error • Bit [6:0] is a signed number indicating the number of switch capacitors
39h	rfcal_log2	7 to 0		R	-	
3Ah	rfcal_log3	7 to 0		R	-	
3Bh	rfcal_log4	7 to 0		R	-	
3Ch	rfcal_log5	7 to 0		R	-	
3Dh	rfcal_log6	7 to 0		R	-	
3Eh	rfcal_log7	7 to 0		R	-	
3Fh	rfcal_log8	7 to 0		R	-	
40h	rfcal_log9	7 to 0		R	-	
41h	rfcal_log10	7 to 0		R	-	
42h	rfcal_log11	7 to 0		R	-	
43h	rfcal_log12	7 to 0		R	-	

10.1.15 Forbidden

Table 27. Forbidden bit descriptions

Address	Register	Bit	Symbol	Access	Value	Description
50h to 67h	-	7 to 0	-	-	-	these bytes are forbidden and must not be written nor read Any modification of these bytes can lead to performance degradation.
FEh	-	7 to 0	-	-	-	
FFh	-	7 to 0	-	-	-	

10.2 Tuner programming sequences with fixed delays or using IRQ

10.2.1 IRQ

In the following drawing,

- Transition 0 (initialisation):
  - Power_state_byte_2: wakes the tuner up
  - MSN_byte_1 (3Bh)
  - MSN_byte_2 (01h): launches tuner calibration
  - IRQ is generated once operations are completed

  - Reference_byte (4Xh)
  - Power_byte_2 (0Eh): sets clock mode
  - Power_state_byte_2: puts the tuner in Standby mode
- Transition 1 (standard selection):
  - IF_Frequency_byte
  - IF_AGC_byte
  - IF_byte_1
  - IR_MIXER_byte_2
  - AGC1_byte_1
  - AGC2_byte_1
  - AGCK_byte_1
  - RF_AGC_byte_1
  - IR_MIXER_byte_1
  - AGC5_byte_1
  - PSM_byte_1
  - Configures the settings that depends on the chosen received TV standard (standard and demodulator dependant)
- Transition 2 (first frequency selection after standard change):
  - Power_state_byte_2: wakes the tuner up
  - Power_byte_2 (0h): sets clock mode
  - RF_Frequency_byte_1
  - RF_Frequency_byte_2
  - RF_Frequency_byte_3: sets the tuner to the wanted RF frequency
  - MSN_byte_1 (41h)
  - MSN_byte_2 (01h): RF filters tuning, PLL locking
  - Tunes the settings that depend on the RF input frequency, expressed in kHz, RF filters tuning, PLL locking
  - IRQ is generated once operations are completed
- Transition 3 (standby):
  - Power_byte_2 (0Eh): sets clock mode
  - Power_state_byte_2
  - Sets the tuner into one of the available Standby modes, keeping the digital data unchanged
- Transition 4 (frequency selection within same standard):
  - RF_Frequency_byte_1
  - RF_Frequency_byte_2
  - RF_Frequency_byte_3: sets the tuner to the desired RF frequency
  - MSN_byte_1 (41h)
  - MSN_byte_2 (01h): RF filters tuning, PLL locking

- Tunes the settings that depend on the RF input frequency, expressed in kHz, RF filters tuning, PLL locking
- IRQ is generated once operations are completed

Remark: a transition action can be launched only after having acknowledged the IRQ of the previous state if applicable and clear the IRQ_clear byte.

Remark: IRQ can be polled in I^2C-bus register table or checked on dedicated pin.

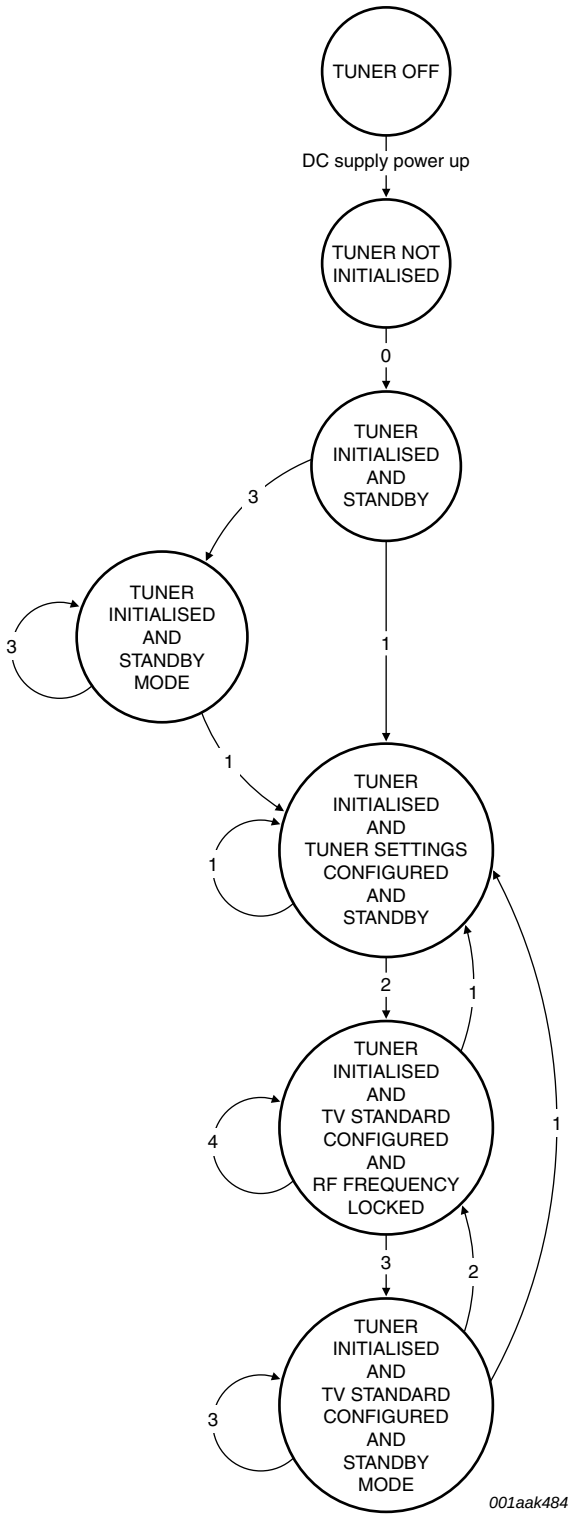


Fig 4. Tuner programming sequence with IRQ

10.3 Channel change programming required parameters

10.3.1 Same reception mode

The new channel to be programmed is within the same standard as the previous one (same channel demodulator).

To be programmed:

- RF frequency
- MSM byte

10.3.2 Different reception mode

The new channel to be programmed is from a different standard compared to the previous one (different channel demodulator).

To be programmed:

- AGC TOP
- IF Frequency
- IF output level
- IF bandwidth
- RF frequency
- MSM byte

11. Hardware settings

11.1 XTOUT output level and I²C-bus address

Table 28. Pin AS_XTSEL decoding

Pin AS_XTSEL	Tuner write address	Tuner status
0 V to 0.1 × V_{CC}	C0h	XTOUT 400 mV (p-p); single ended
0.2 × V_{CC} to 0.3 × V_{CC}	C0h	XTOUT 800 mV (p-p); single ended
0.4 × V_{CC} to 0.6 × V_{CC}	C6h	XTOUT 400 mV (p-p); single ended
0.9 × V_{CC} to V_{CC}	C6h	XTOUT 800 mV (p-p); single ended

12. Internal circuitry

Table 29. Internal circuits for each pin

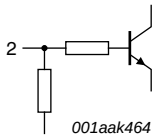
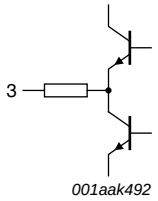
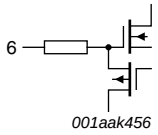
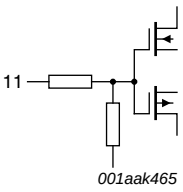
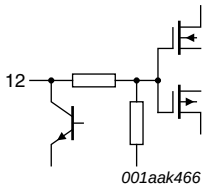
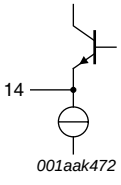
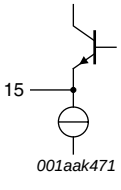
Symbol	Pin	Description[1]
RFIN	2	
LT	3	
AS_XTSEL	6	
SCL	11	
SDA	12	
XTALP	14	
XTALN	15	

Table 29. Internal circuits for each pin *...continued*

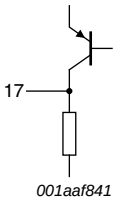
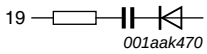
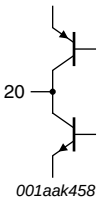
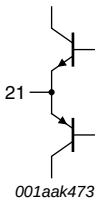
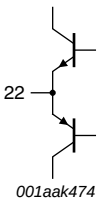
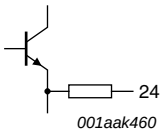
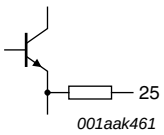
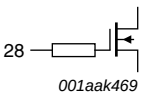
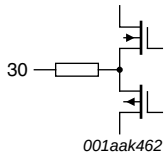
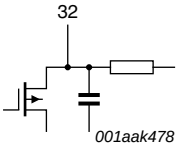
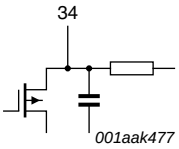
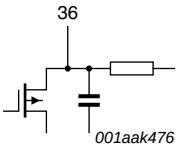
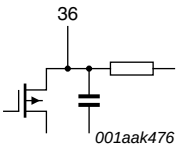
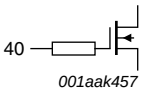
Symbol	Pin	Description[1]
CAPREGVCO	17	
VTUNE	19	
CP	20	
XTOUT1	21	
XTOUT2	22	
IFN	24	
IFP	25	
VIFAGC	28	

Table 29. Internal circuits for each pin *...continued*

Symbol	Pin	Description[1]
IRQ	30	
VHFLOW	32	
VHFHIGH	34	
UHFLOW	36	
UHFHIGH	38	
CAPRFAGC	40	

[1] ESD protection components are not shown.

13. Limiting values

Table 30. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.6	V
V_I	input voltage	V_{CC} < 3.3 V	–0.3	V_{CC} + 0.3	V
		V_{CC} > 3.3 V	–0.3	+3.6	V
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	+120	°C
V_{ESD}	electrostatic discharge voltage	EIA/JESD22-A114 (human body model)	–2	+2	kV
		EIA/JESD22-C101-C (FCDM) class III[1]	750	-	V

[1] Class III: 500 V to 1000 V.

14. Thermal characteristics

Table 31. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	according to JEDEC specification 4L board with 9 thermal vias	31.4	K/W

15. Characteristics

Table 32. General characteristics for TV reception (RF input to IF output)

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 1 V (p-p); IF output load of 1 kΩ/1 pF; AGC1 range: from –12 dB to +15 dB; AGC1 TOP: 95/89 dBμV; AGC3 TOP: 96 dBμV; AGC4 TOP: 105/100 dBμV; AGC5 TOP: 105/100 dBμV; IF LEVEL: –6/24 dB; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			3.13	3.30	3.47	V
$V_{O(p-p)(max)}$	maximum peak-to-peak output voltage	differential IF output		0.5	-	2	V
I_{CC}	supply current	Normal mode		<tbd>	240	<tbd>	mA
		Standby mode					
		crystal oscillator ON, XTOUT OFF, LT ON		<tbd>	38	<tbd>	mA
		only crystal oscillator ON		<tbd>	12	<tbd>	mA
f_{RF}	RF frequency	full range of RF input		42	-	870	MHz
		center of channel		45	-	866	MHz
f_{lo}	local oscillator frequency	for respective IF frequency		50	-	870.25	MHz
VSWR	voltage standing wave ratio	RF input; 75 Ω nominal impedance, level below 95 dBμV		-	2.6	<tbd>	-
NF_{tun}	tuner noise figure	75 Ω source; maximum gain		-	5.0	5.9	dB
		75 Ω source; 60 dBμV condition	[1]	-	-	6.6	dB
$G_{v(max)}$	maximum voltage gain	all bands		<tbd>	87	<tbd>	dB
$G_{v(min)}$	minimum voltage gain	all bands		<tbd>	–28	<tbd>	dB
ΔG_{rsd}	residual gain variation	in case of RF gain change	[2]	-	-	0.7	dB
$\Delta G_{AGC(tun)}$	tuner AGC gain range			-	115	-	dB
ICP_{1dB}	1 dB input compression point	at tuner input and minimum gain		124	-	-	dBμV
φ_n	phase noise	UHF and VHF bands					
		at 1 kHz frequency offset		-	-	–80	dBc/Hz
		at 10 kHz frequency offset		-	-	–85	dBc/Hz
		at 100 kHz frequency offset		-	-	–105	dBc/Hz
$t_{startup(tun)}$	tuner start-up time			-	400	-	ms
t_{set}	setting time	tuner channel change		-	-	5	ms
$IP3_I$	input third-order intercept point	gain corresponding to 100 dBμV	[3]	120	-	-	dBμV
$IP2_I$	input second-order intercept point	gain corresponding to 100 dBμV	[3]	160	-	-	dBμV
φ_{jit}	phase jitter	UHF; integrated from 1 kHz to 4 MHz		-	0.5	0.7	degree

Table 32. General characteristics for TV reception (RF input to IF output) *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 1 V (p-p); IF output load of 1 kΩ/1 pF; AGC1 range: from –12 dB to +15 dB; AGC1 TOP: 95/89 dBμV; AGC3 TOP: 96 dBμV; AGC4 TOP: 105/100 dBμV; AGC5 TOP: 105/100 dBμV; IF LEVEL: –6/24 dB; unless otherwise specified.

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
$f_{-3dB(hpf)}$	high-pass filter cut-off frequency	3 db cut-off frequency:							
		DC_NOTCH	IF_HP_FC	HI_Pass					
		0	XX	0		-	130	-	kHz
		1	XX	0		-	250	-	kHz
		1	00	1		-	290	-	kHz
		1	01	1		-	610	-	kHz
		1	10	1		-	720	-	kHz
		1	11	1		-	1080	-	kHz
$f_{-3dB(lpf)}$	low-pass filter cut-off frequency								
		for a 1.7 MHz channel				-	1.59	-	MHz
		for a 6 MHz channel				-	6.58	-	MHz
		for a 7 MHz channel				-	7.35	-	MHz
		for a 8 MHz channel				-	8.35	-	MHz
α_{lpf}	low-pass filter attenuation	N – 1 sound carrier			[4]	14	-	-	dB
		N – 1			[5]	23	-	-	dB
		N ± 2				60	-	-	dB
		> 18 MHz				60	-	-	dB
$f_{c(notch)}$	notch center frequency	• for 6 MHz LPF				-	6.5	-	MHz
		• for 7 MHz LPF				-	7.25	-	MHz
		• for 8 Mhz LPF				-	8.25	-	MHz
G_{tlt}	tilt gain	in band, 6 MHz, 7 MHz and 8 MHz channels				-	1	3	dB
α_{image}	image rejection	worst case for image rejection and 4 MHz IF frequency for levels above –50 dBm				57.5	63	-	dB
CSO	composite second-order distortion	worst interferer over RF frequency wrt to wanted carrier				<tbd>	<tbd>	<tbd>	dBc
CTB	composite triple beat	worst interferer over RF frequency wrt to wanted carrier				<tbd>	<tbd>	<tbd>	dBc

[1] Single wanted channel, 60 dBμV, at tuner input.

[2] If this residual step is considered as limitating for the IC performances, refer to the Application Note *AN1002* for compromise to circumvent it.

[3] Single wanted channel, 100 dBμV level, at tuner input.

[4] Wanted channel being N, rejection of the N + n channel sound carrier for analog reception.

[5] Adjacent channel power rejection.

Table 33. General characteristics for TV reception (RF input to IF output) in case of LT usage

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 1 V (p-p); IF output load of 1 kΩ/1 pF; AGC1 range: from +6 dB to +15 dB; AGC1 TOP: 95/89 dBμV; AGC3 TOP: 96 dBμV; AGC4 TOP: 105/100 dBμV; AGC5 TOP: 105/100 dBμV; IF LEVEL: −6/24 dB; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$G_{v(max)}$	maximum voltage gain	all bands		<tbd>	<tbd>	<tbd>	dB
$G_{v(min)}$	minimum voltage gain	all bands		<tbd>	<tbd>	<tbd>	dB
ΔG_{rsd}	residual gain variation	in case of RF gain change	[1]	-	-	<tbd>	dB
$\Delta G_{AGC(tun)}$	tuner AGC gain range			-	<tbd>	-	dB
ICP_{1dB}	1 dB input compression point	at tuner input and minimum gain		<tbd>	-	-	dBμV
$IP3_I$	input third-order intercept point	gain corresponding to 100 dBμV	[2]	<tbd>	-	-	dBμV
$IP2_I$	input second-order intercept point	gain corresponding to 100 dBμV	[2]	<tbd>	-	-	dBμV
CSO	composite second-order distortion	worst interferer over RF frequency wrt to wanted carrier		<tbd>	<tbd>	<tbd>	dBc
CTB	composite triple beat	worst interferer over RF frequency wrt to wanted carrier		<tbd>	<tbd>	<tbd>	dBc

[1] If this residual step is considered as limitating for the IC performances, refer to application note for compromise to circumvent it.

[2] Single wanted channel, 100 dBμV level, at tuner input.

Table 34. Loop-through characteristics

T_{amb} = 25 °C; V_{CC} = 3.3 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	full range of RF input	42	-	870	MHz
VSWR	voltage standing wave ratio	75 Ω nominal impedance	-	-	3	
NF	noise figure		-	6	-	dB
G_v	voltage gain		1	-	4	dB
CSO	composite second-order distortion	129-NTSC channels 75 dBμV input level	-	-	−57	dBc
CTB	composite triple beat	129-NTSC channels 75 dBμV input level	-	-	−57	dBc

Remark: The LT function is available whatever the AGC1 gain range, nevertheless if the level is such that AGC1 goes below +6 dB, LT output will then reproduce AGC1 gain steps from +3 dB to −12 dB if the AGC1 gain range is not limited by AGC1_6_15dB bit. (0Ch, bit 6).

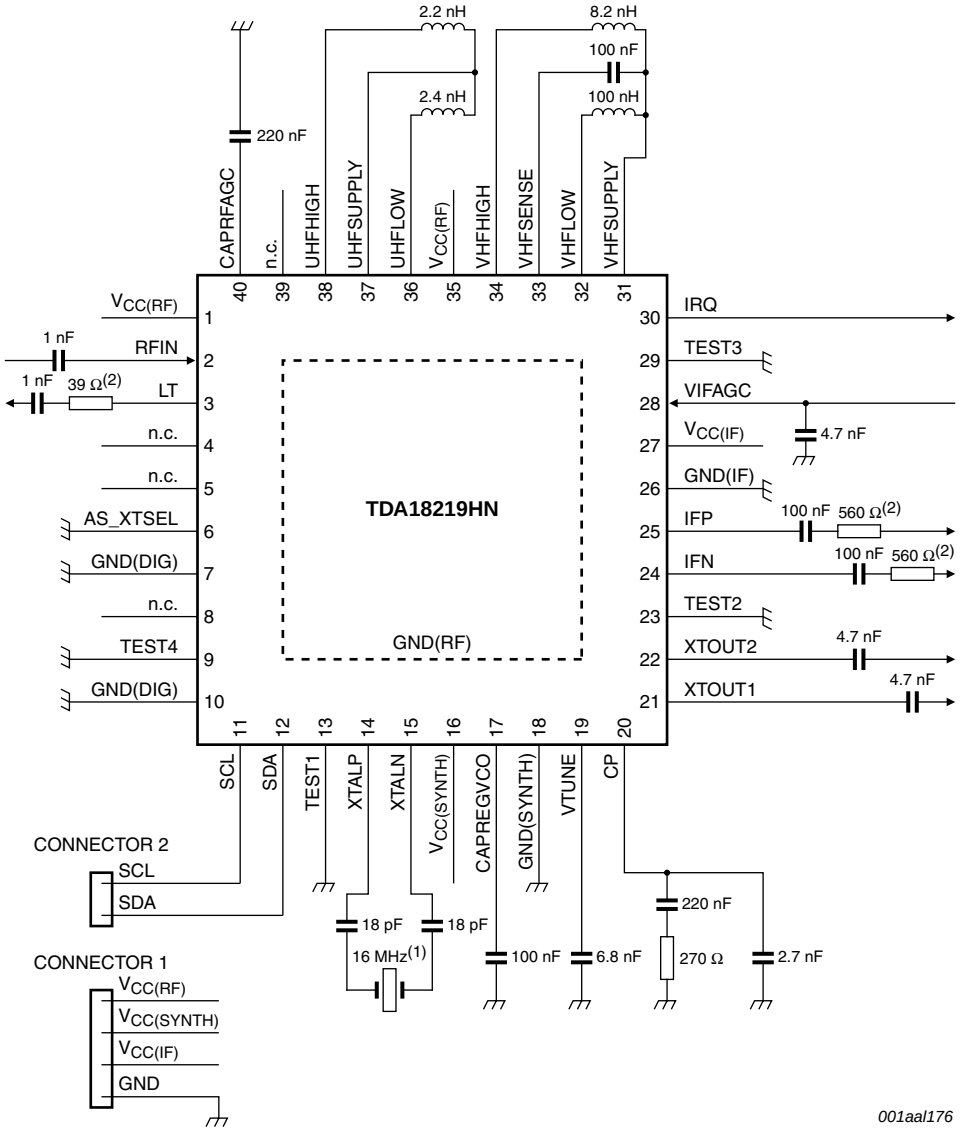
Table 35. Pins Characteristics

T_{amb} = 25 °C; V_{CC} = 3.3 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF AGC input						
V_{AGC}	AGC voltage		0	-	V_{CC}	V
dG_{AGC}/dV	rate of change of AGC gain with voltage		-	50	65	dB/V
Crystal oscillator						
f_{xtal}	crystal frequency		-	16	-	MHz
Z_i	input impedance	magnitude value	-	<tbd>	-	Ω
Crystal oscillator output buffer						
R_o	output resistance	16 MHz output frequency	-	460	-	Ω
Digital levels (I^2C-bus)[1]						
Pin SCL						
V_{IL}	LOW-level input voltage	V_{CC} related input levels	-	-	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage	V_{CC} related input levels	$0.7V_{CC}$	-	-	V
f_{SCL}	SCL clock frequency		-	-	400	kHz
Pin SDA						
V_{IL}	LOW-level input voltage	V_{CC} related input levels	-	-	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage	V_{CC} related input levels	$0.7V_{CC}$	-	-	V
V_{OL}	LOW-level output voltage	I_O = 3 mA (sink current)	-	-	0.4	V

[1] Devices that use non-standard supply voltages, which do not conform the intended I^2C-bus system levels, must relate their input levels to the supply voltage (V_{CC}) to which the pull-up resistors are connected.

These performances are measured in putting the tuner in following configuration:



Remark: Decoupling capacitors are not depicted.

(1) Quartz references are: NX5032GA and NX3225GA

(2) The series resistors connected on the pins 3, 24 and 25 are used for test purpose only; not necessary for the application.

Fig 5. Measurement schematic

Table 36. Used coils type 402

band	coil reference	component size
UHF HIGH COIL	LQW5AN2N2C10	402
UHF LOW COIL	LQP15MN2N4W02	402
VHF HIGH COIL	LQP15MN8N2B02	402
VHF LOW COIL	LQG15HNR10J02	402

Table 37. Used coils type 603

band	coil reference	component size
UHF HIGH COIL	LQW18AN2N2D00	603
UHF LOW COIL	LQP18MN2N2C02	603
VHF HIGH COIL	LQP18MN8N2C02	603
VHF LOW COIL	LQW18ANR10J00	603

Remark: All following curves represent typical results observed on samples.

15.1 IF filtering curves

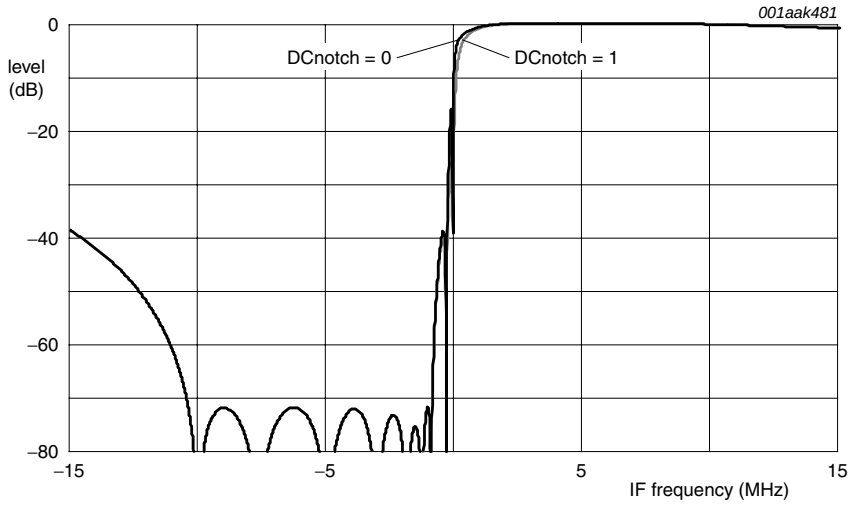


Fig 6. DC notch

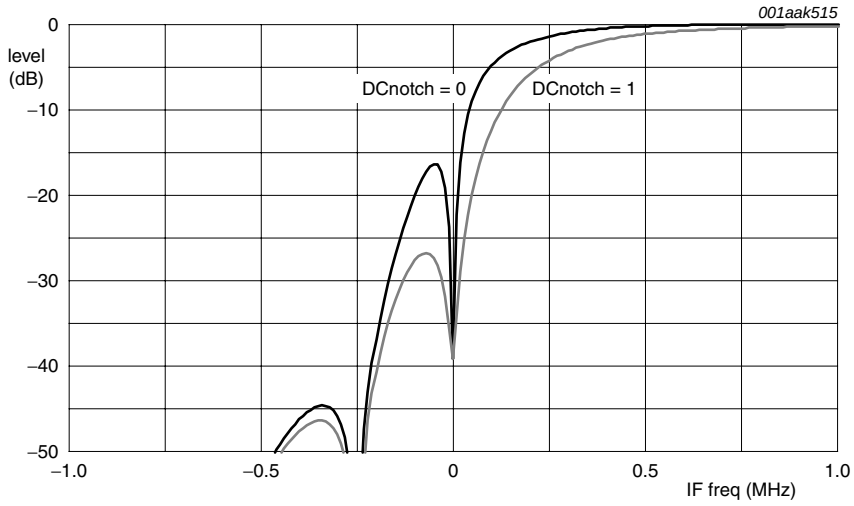
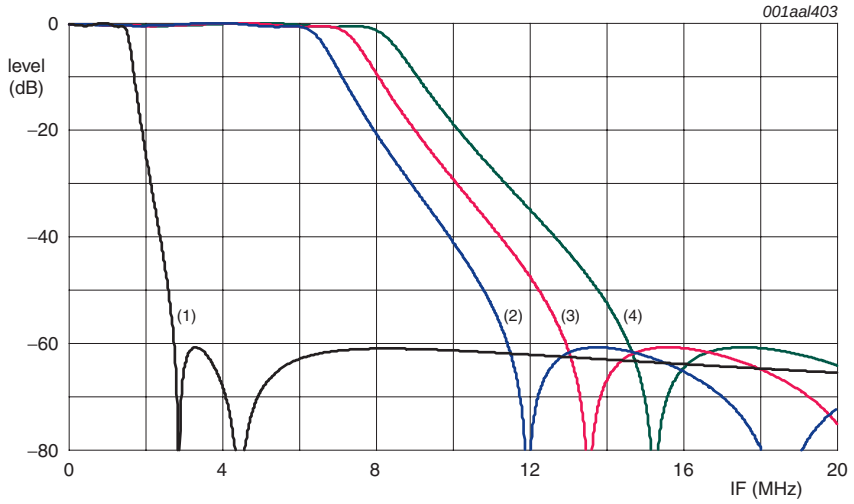


Fig 7. DC notch zoom



(1) LPF = 1.7 MHz
(2) LPF = 6 MHz
(3) LPF = 7 MHz
(4) LPF = 8 MHz

Fig 8. Low-pass filter

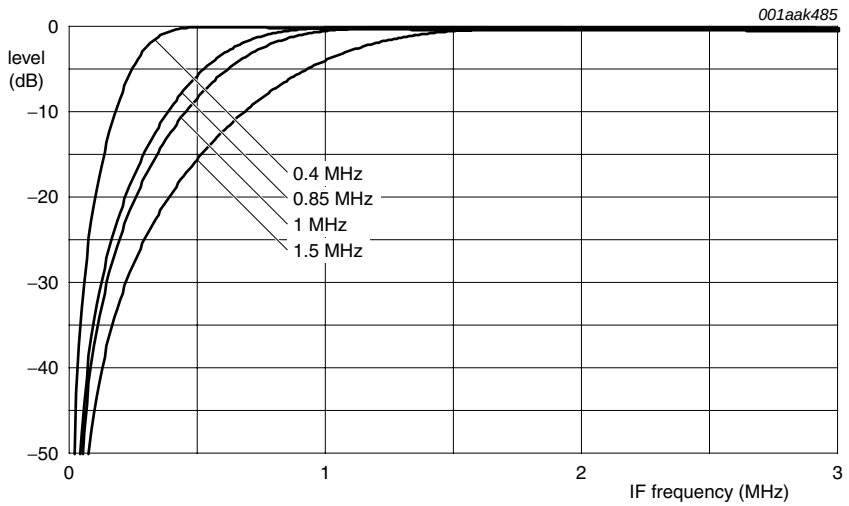


Fig 9. High-pass filter

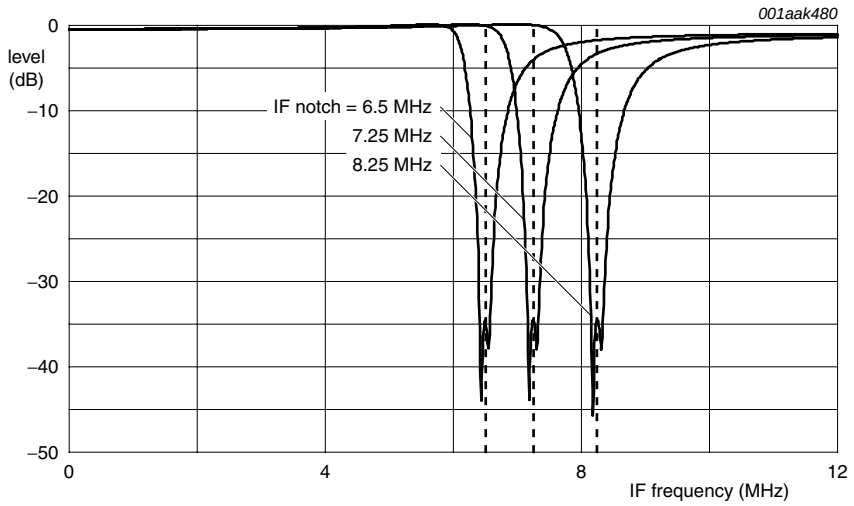
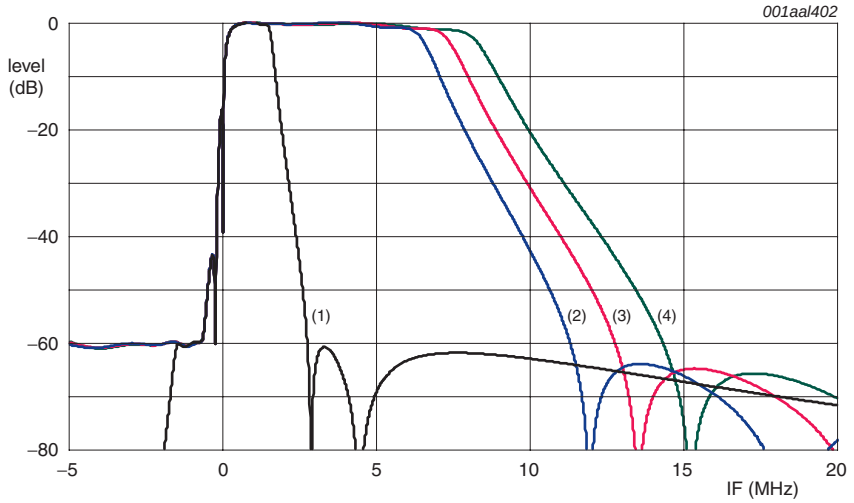
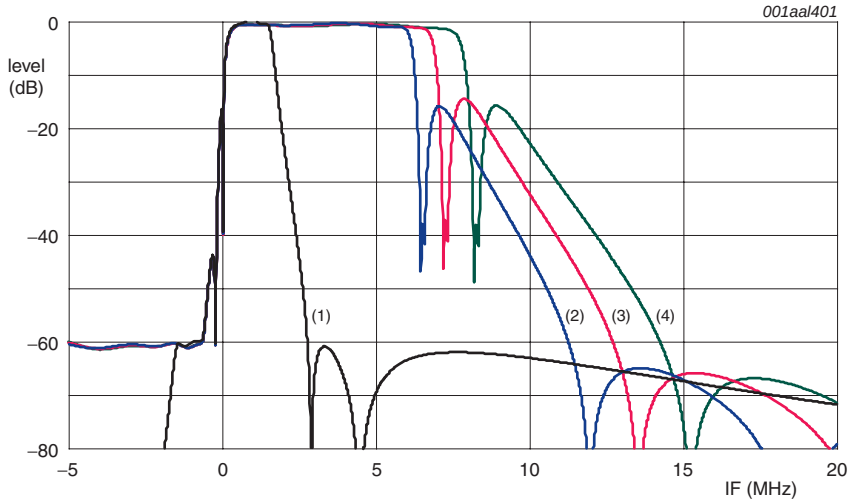


Fig 10. IF notches



(1) LPF = 1.7 MHz
(2) LPF = 6 MHz
(3) LPF = 7 MHz
(4) LPF = 8 MHz

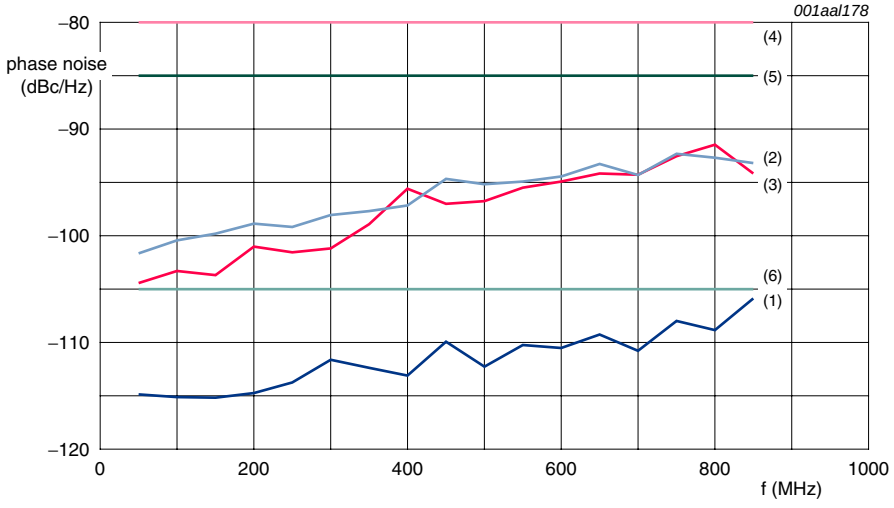
Fig 11. IF selectivity without notch



(1) LPF = 1.7 MHz
(2) LPF = 6 MHz
(3) LPF = 7 MHz
(4) LPF = 8 MHz

Fig 12. IF selectivity with notch

15.2 Phase noise curves



(1) 100 kHz
(2) 10 kHz
(3) 1 kHz
(4) Spec_1 kHz
(5) Spec_10 kHz
(6) Spec_100 kHz

Fig 13. Phase noise

15.3 IF gain versus VAGC

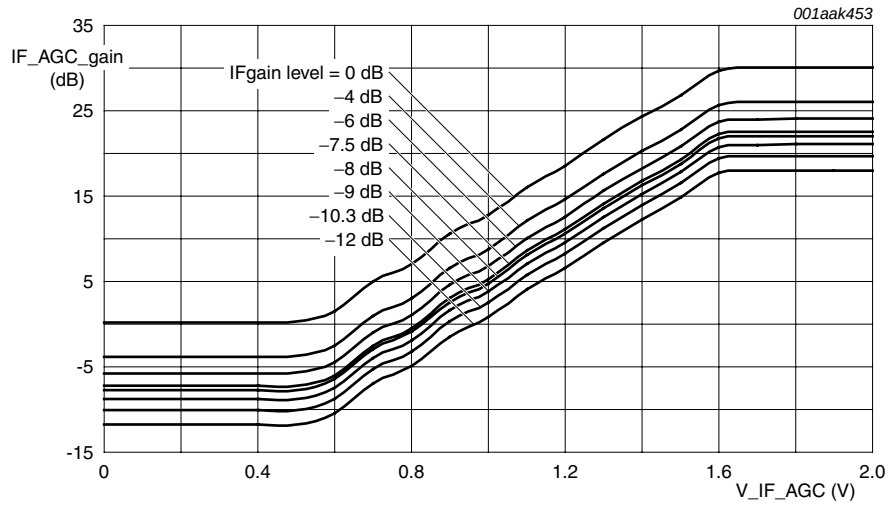


Fig 14. IF gain versus VAGC

15.4 NF curves

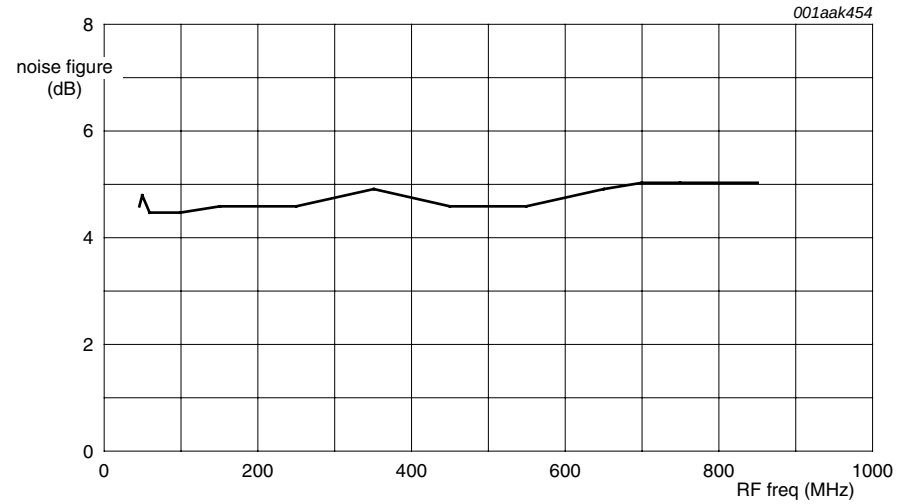


Fig 15. Noise figure

16. Application information

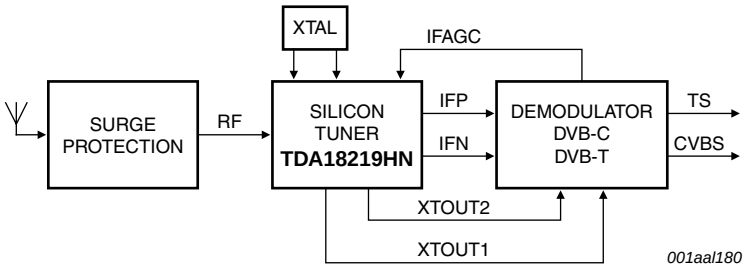
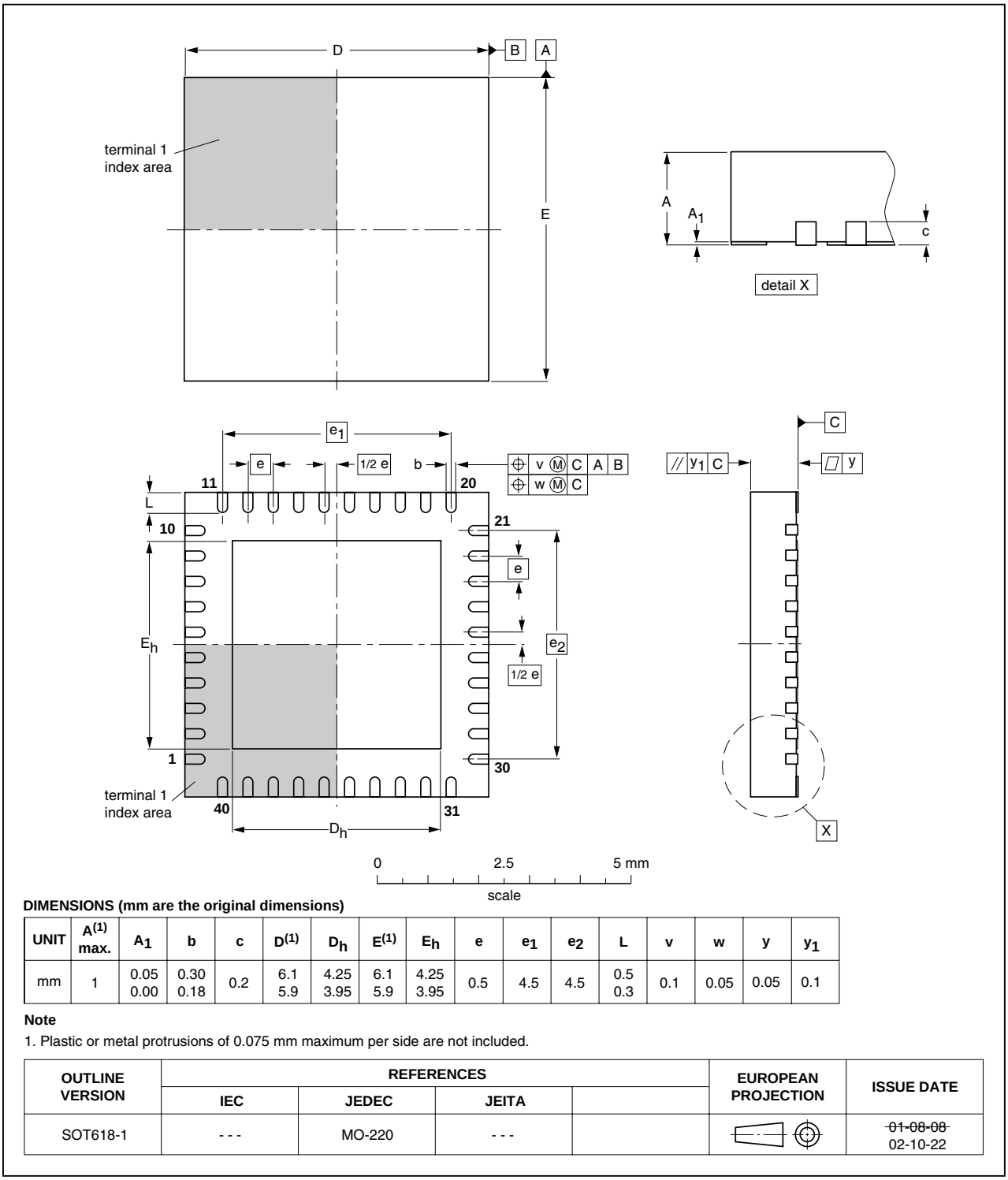


Fig 16. Tuner application diagram

17. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 17. Package outline SOT618-1 (HVQFN40)

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 38 and 39

Table 38. SnPb eutectic process (from J-STD-020C)

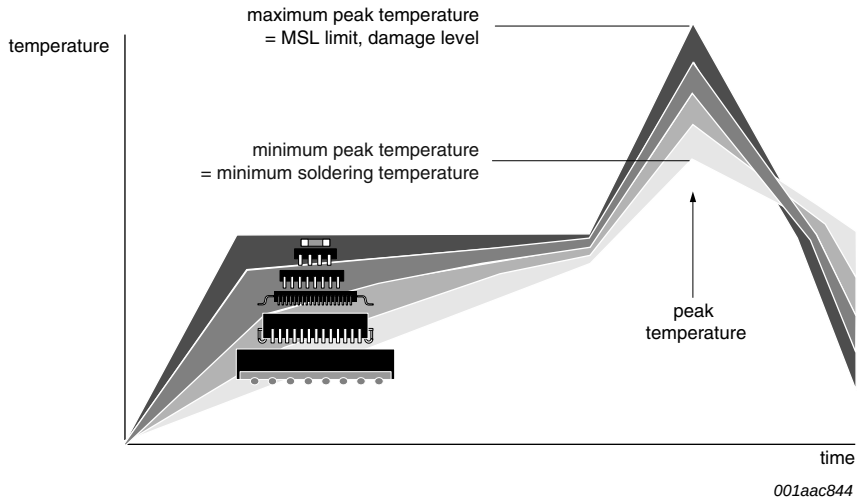
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 39. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 40. Abbreviations

Acronym	Description
ACI	Adjacent Channel Interferer
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AGCK	Automatic Gain Control step Killer
ARIB	Association of Radio Industries and Businesses
D-BOOK	Digital Terrestrial Television Requirements for Interoperability issued by the Digital Television Group in UK
DTMB	Digital Terrestrial Multimedia Broadcast
DVB	Digital Video Broadcasting
DVB-T/C/H	DVB-Terrestrial/Cable/Handheld
DVD-R	DVD-Recorder
EMC	ElectroMagnetic Compatibility
EU	European Union
FRAC-N	Fractional-N
HPF	High-Pass Filter
IF	Intermediate Frequency
IR	Image Rejection
IRQ	Interrupt ReQuest
ISDB-T	Integrated Services Digital Broadcasting - Terrestrial
LC-VCO	Inductors and Capacitors - Voltage Controlled Oscillator

Table 40. Abbreviations *...continued*

Acronym	Description
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass filter
LT	Loop-through
MSM	Main State Machine
NTSC	National Television System Committee
PCTV	Personal Computer Television
PLD	Power Level Detector
PLL	Phase-Locked Loop
POR	Power-On Reset
RC CAL	Resistors and Capacitors calibrations
RF	Radio Frequency
RoHS	Restriction of the use of certain Hazardous Substances
SAW	Surface Acoustic Wave
STB	Set Top Box
TOP	Take Over Point
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency

20. Revision history

Table 41. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA18219HN_1	20100203	Objective data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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23. Tables

24. Figures

25. Contents

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