TPD2E2U06-Q1 Automotive Dual-Channel High-Speed ESD Protection Device

1 Features

- AEC-Q101 Qualified
- IEC 61000-4-2 Level 4
  - ±25-kV (Contact Discharge)
  - ±30-kV (Air-gap Discharge)
- IO Capacitance 1.5 pF (Typ)
- DC Breakdown Voltage 6.5 V (Min)
- Ultra-Low Leakage Current 10 nA (Max)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to +125°C
- Small Easy-to-Route DBZ Package

2 Applications

- Automotive Infotainment
- Automotive Gauge Clusters

3 Description

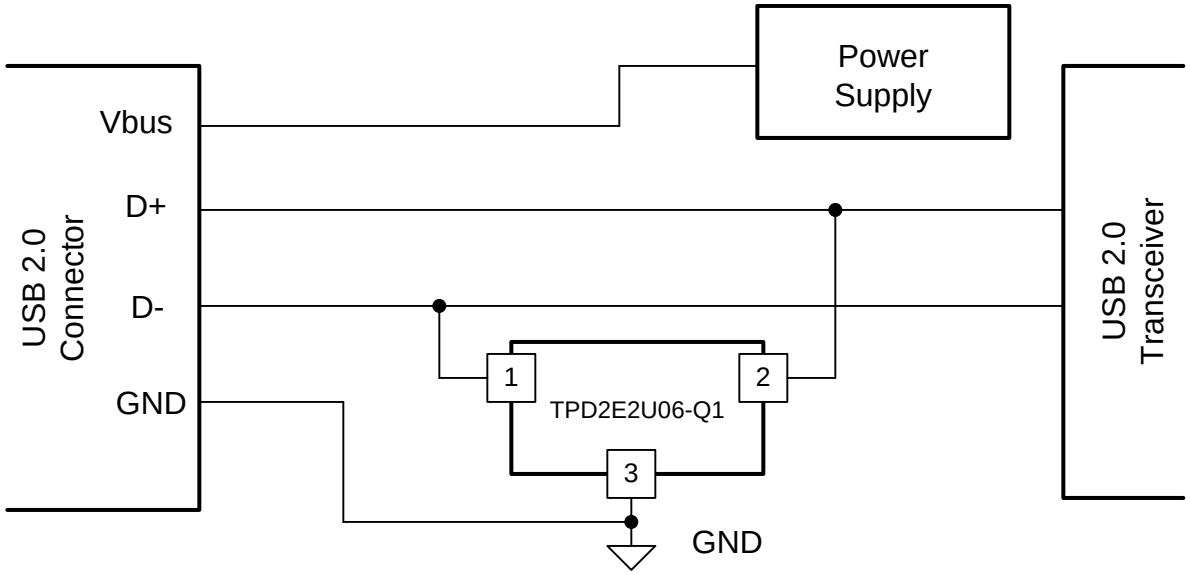
The TPD2E2U06-Q1 is a Transient Voltage Suppressor (TVS) Electrostatic Discharge (ESD) protection diode array with low capacitance. It is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The 1.5-pF line capacitance makes it ideal for protecting interfaces such as USB 2.0, LVDS, Antenna, and I^2C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2E2U06-Q1	SOT23 (3)	2.90 mm × 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision A (December 2014) to Revision B — **Page**

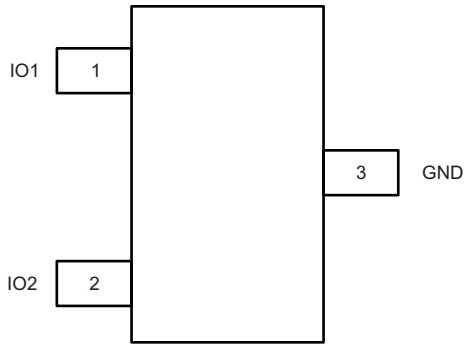
- Added temperature specification to V_{BR} TEST CONDITIONS. ... 4

Changes from Original (December 2014) to Revision A — **Page**

- Initial release of full document. ... 1

6 Pin Configuration and Functions

DBZ
2.9 mm × 1.3 mm × 0.95 mm
(1.9-mm PITCH)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IO1	1	I/O	The IO1 and IO2 pins are an ESD protected channel. Connect these pins to the data line as close to the connector as possible.
IO2	2	I/O	
GND	3	G	The GND (ground) pin is connected to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_{PP}	Peak pulse current (t_p = 8/20 µs)		5.5 (1)	A
P_{PP}	Peak pulse power (t_p = 8/20 µs)		75 (1)	W
T_J	Junction temperature	–40	125	°C
T_S	Storage temperature	–65	150	°C

(1) Measured at 25°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001, all pins (1)	±10000	V
		Charged device model (CDM), per AEC Q101-005, all pins	±1000	
		IEC 61000-4-2 Contact	±25000	V
		IEC 61000-4-2 Air Gap	±30000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input Pin Voltage	0		5.5	V
T_A	Operating Free Air Temperature	-40		125	℃

7.4 Thermal Information

THERMAL METRIC[1]		TPD2E2U06-Q1 DBZ 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	439.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	194.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	173.9	
ψ_{JT}	Junction-to-top characterization parameter	53.7	
ψ_{JB}	Junction-to-board characterization parameter	172.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, .

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 µA			5.5	V
V_{CLAMP}	IO to GND	I_{PP} = 1 A, TLP[1][2]		9.7		V
		I_{PP} = 5 A, TLP[1][2]		12.4		
	GND to IO	I_{PP} = 1 A, TLP[1][2]		1.9		
		I_{PP} = 5 A, TLP[1][2]		4		
R_{DYN}	Dynamic resistance	IO to GND[3][2]		0.6		Ω
		GND to IO[3][2]		0.4		
C_L	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V[2]		1.5	1.9	pF
C_{CROSS}	Channel-to-channel input capacitance	Pin 3 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins[2]		0.02	0.03	pF
Δ_{CL}	Variation of channel input capacitance	Pin 3 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, Pin 1 to GND – Pin 2 to GND[2]		0.03	0.1	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA[2]	6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V		1	10	nA

(1) Transmission Line Pulse with 10-ns rise time, 100-ns width.
(2) Measured at 25°C.
(3) Extraction of R_{DYN} Using least squares fit of TLP characteristics between I = 20 A and I = 30 A.

7.6 Typical Characteristics

Measured at T_A = 25°C unless otherwise specified

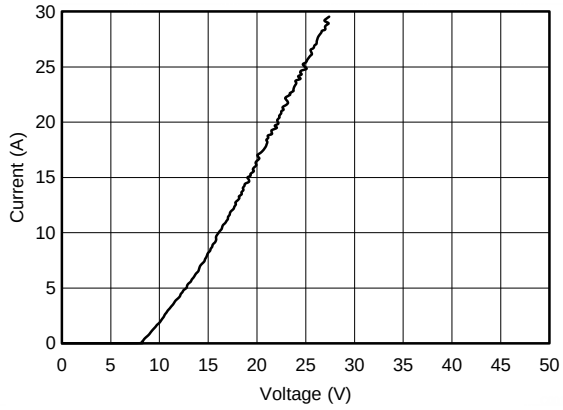


Figure 1. TLP, Data to GND

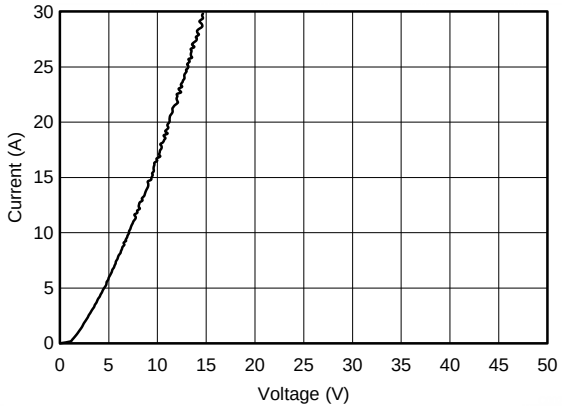


Figure 2. TLP, GND to Data

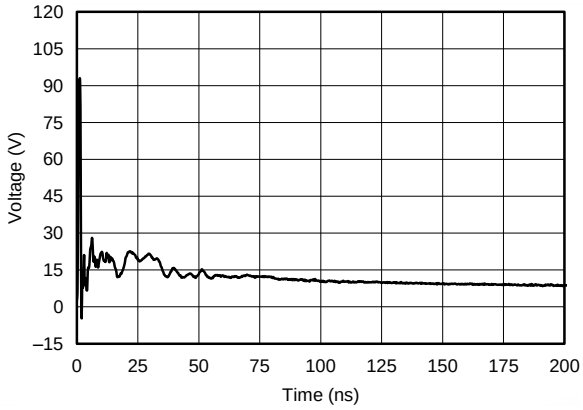


Figure 3. IEC 61000-4-2 Clamping Voltage, +8 kV Contact

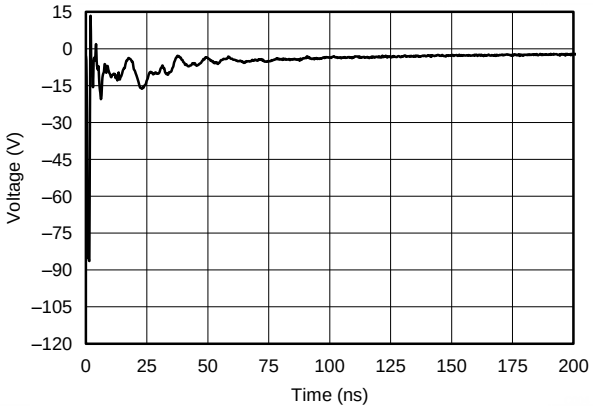


Figure 4. IEC 61000-4-2 Clamping Voltage, –8 kV Contact

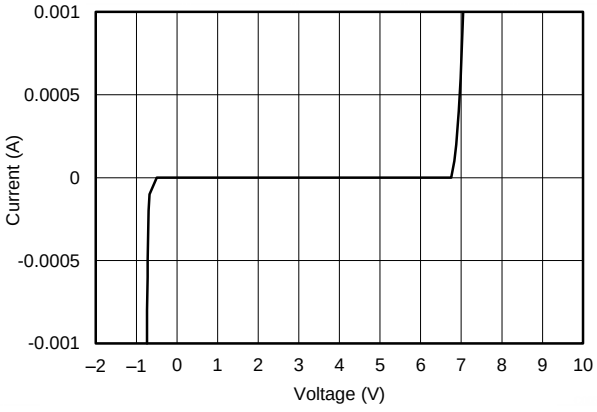


Figure 5. IV Curve, T_A = 25°C

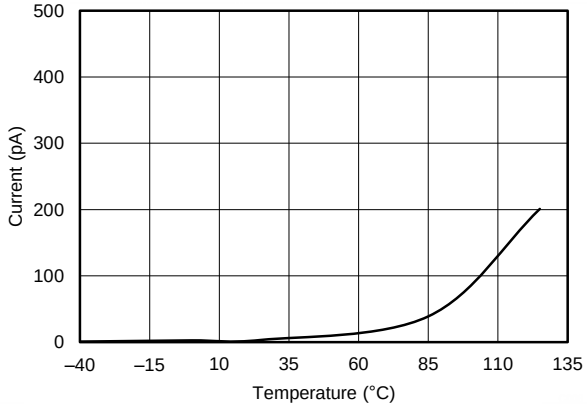


Figure 6. I_{LEAK} vs Temperature, V_{IN} = 2.5 V

Typical Characteristics (continued)

Measured at T_A = 25°C unless otherwise specified

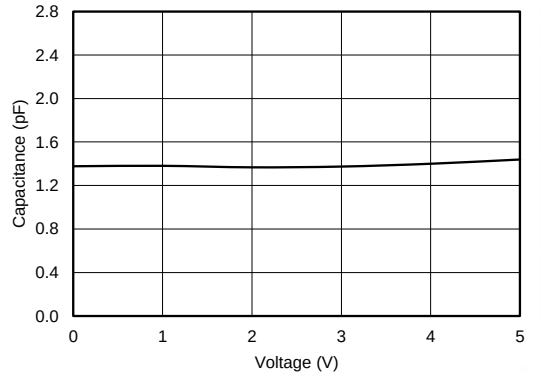


Figure 7. Capacitance Across V_{BIAS} f = 1 MHz

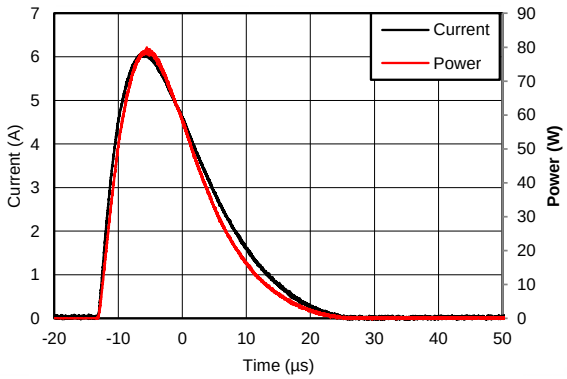


Figure 8. Surge Curve (t_p = 8/20 µs) IO TO GND

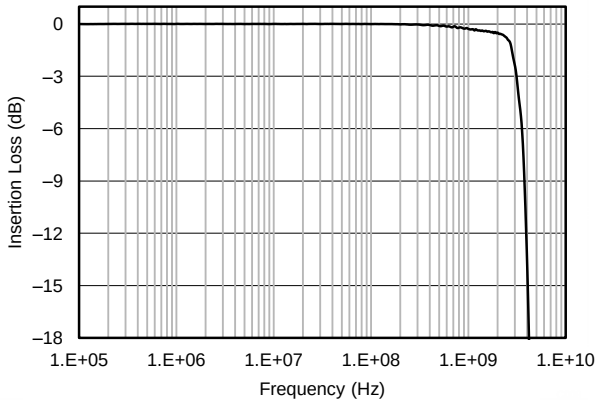


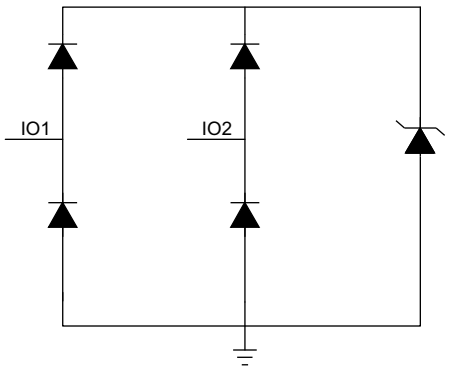
Figure 9. Insertion Loss

8 Detailed Description

8.1 Overview

The TPD2E2U06-Q1 is a TVS ESD protection diode array with low capacitance. It is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The 1.5-pF line capacitance makes it ideal for protecting interfaces such as USB 2.0, LVDS, Antenna, and I^2C.

8.2 Functional Block Diagram



8.3 Feature Description

The TPD2E2U06-Q1 is a TVS ESD protection diode array with low capacitance. It is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The 1.5-pF line capacitance makes it ideal for protecting interfaces such as USB 2.0, LVDS, Antenna, and I^2C.

8.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards. It passes HBM H3B (±8 kV) and CDM C5 (±1 kV) ESD ratings and is qualified to operate from –40°C to 125°C.

8.3.2 IEC 61000-4-2 Level 4

The I/O pins can withstand ESD events up to ±25-kV contact and ±30-kV air. An ESD/surge clamp diverts the current to ground.

8.3.3 IO Capacitance

The capacitance between each I/O pin to ground is 1.5 pF. These capacitances support data rates in excess of 1.5 Gbps.

8.3.4 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

8.3.5 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Max) with a bias of 2.5 V.

8.3.6 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.7 V (I_{PP} = 1 A).

8.3.7 Industrial Temperature Range

This device is designed to operate from –40°C to 125°C.

Feature Description (continued)

8.3.8 Small Easy-to-Route Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

8.4 Device Functional Modes

TPD2E2U06-Q1 is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±30 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD2E2U06-Q1 (usually within 10's of nano-seconds) the device reverts to passive.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TPD2E2U06-Q1 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

9.2 Typical Application

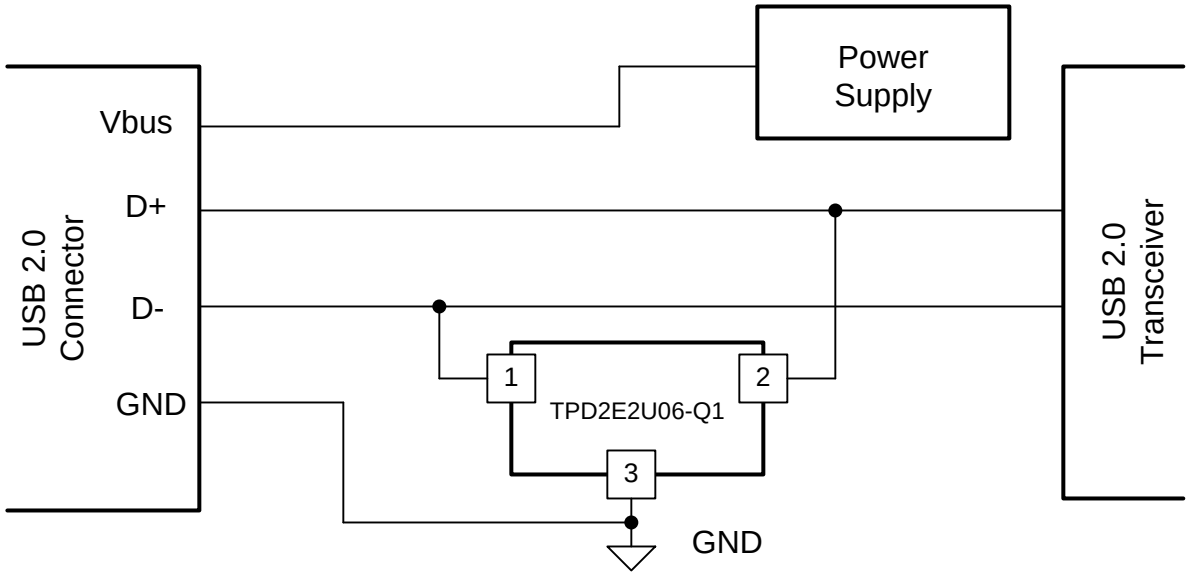


Figure 10. Typical USB Application Diagram

9.2.1 Design Requirements

For this design example, one TPD2E2U06-Q1 device will be used in a USB 2.0 application. This will provide complete port protection.

Given the USB 2.0 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on Pins 1 or 2	0 V to 3.3 V
Operating Frequency	240 MHz

9.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range of all the protected lines
- Operating frequency

9.2.2.1 Signal Range

The TPD2E2U06-Q1 has 2 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 2 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

9.2.2.2 Operating Frequency

The TPD2E2U06-Q1 has a capacitance of 1.5 pF (Typ), supporting USB 2.0 data rates.

9.2.3 Application Curves

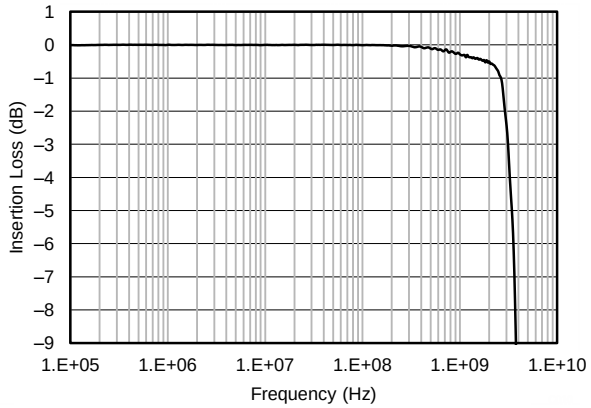


Figure 11. Insertion Loss Graph

10 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care should be taken to make sure that the maximum voltage specifications for each line are not violated.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

This application is typical of a differential data pair application, such as USB 2.0.

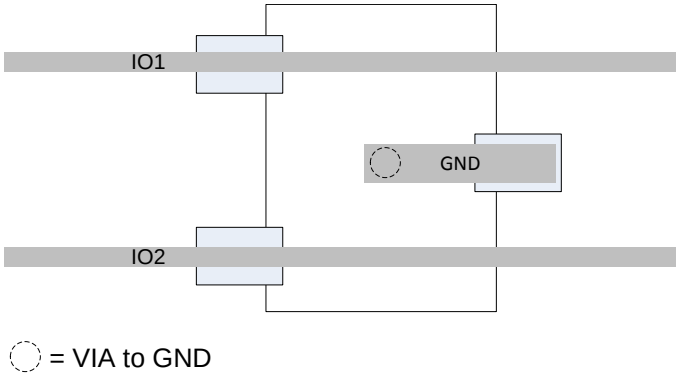


Figure 12. Routing with DBZ Package

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E2U06QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22U6Q	Samples
TPD2E2U06QDCKRQ1	PREVIEW	SC70	DCK	3	3000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD2E2U06-Q1 :

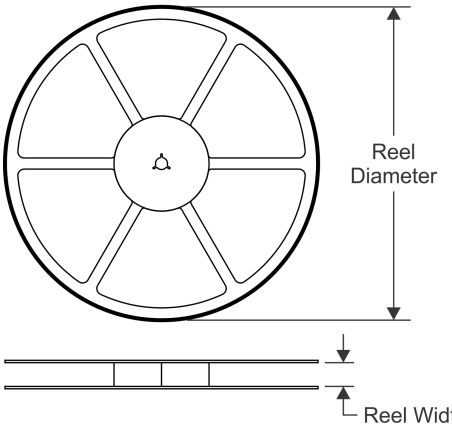
- Catalog: TPD2E2U06

NOTE: Qualified Version Definitions:

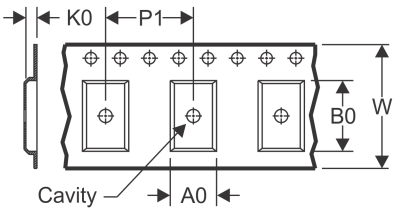
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

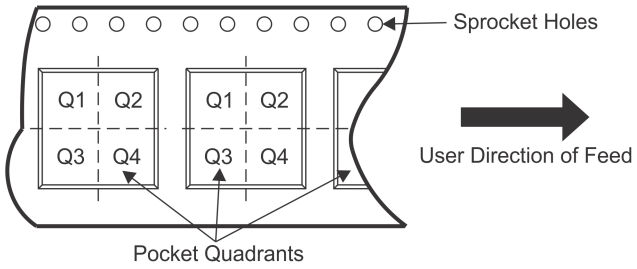


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

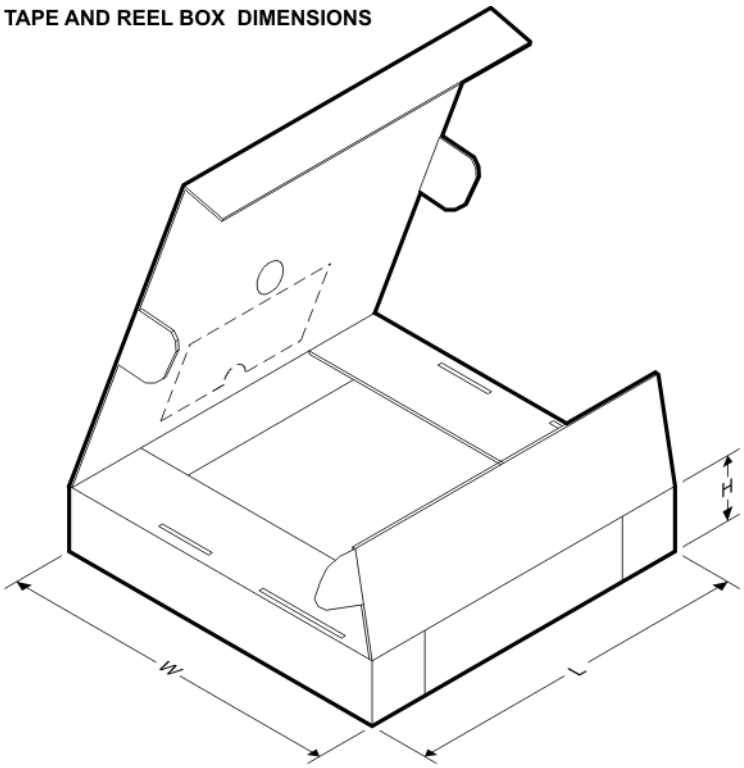
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

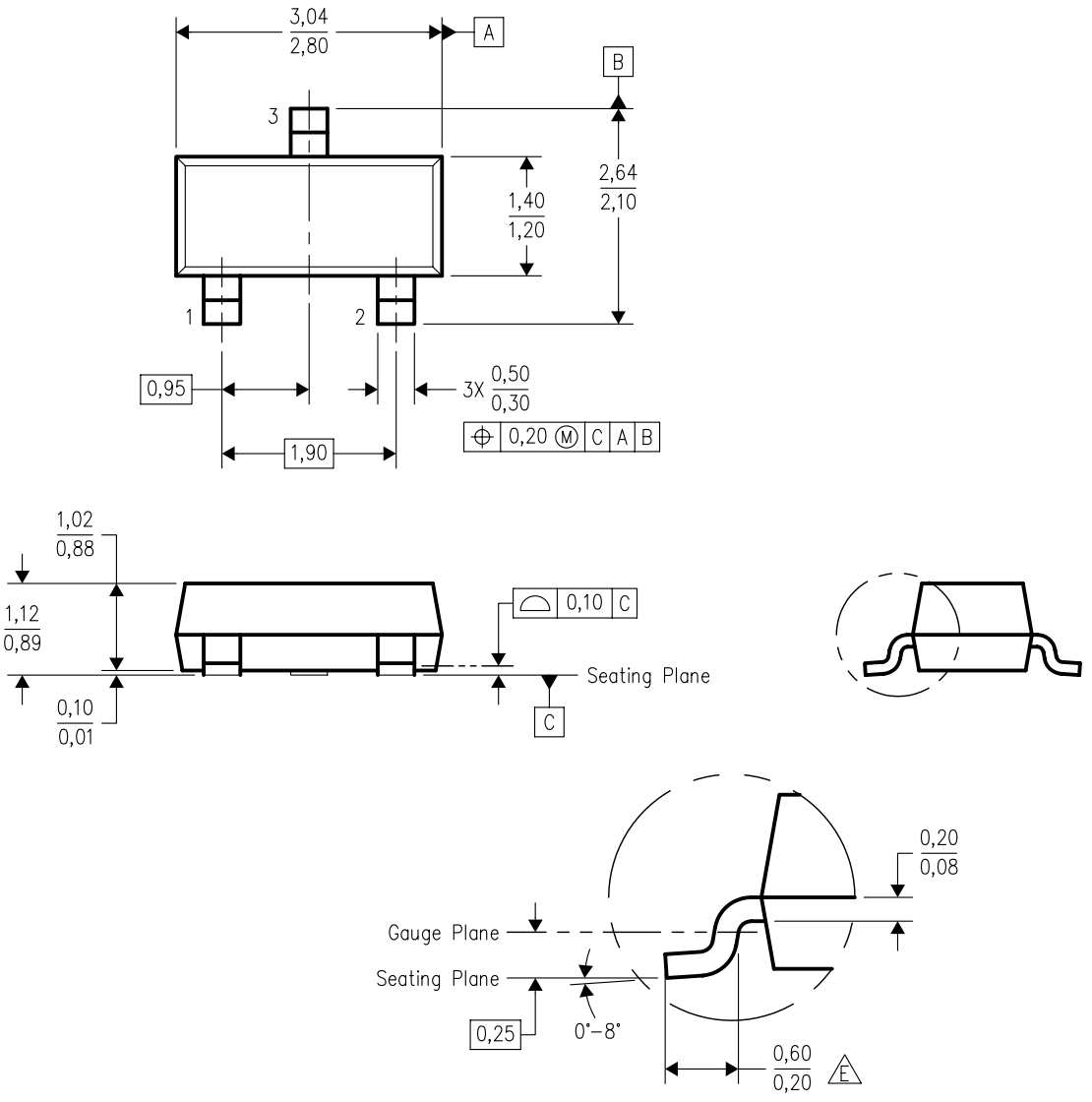
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

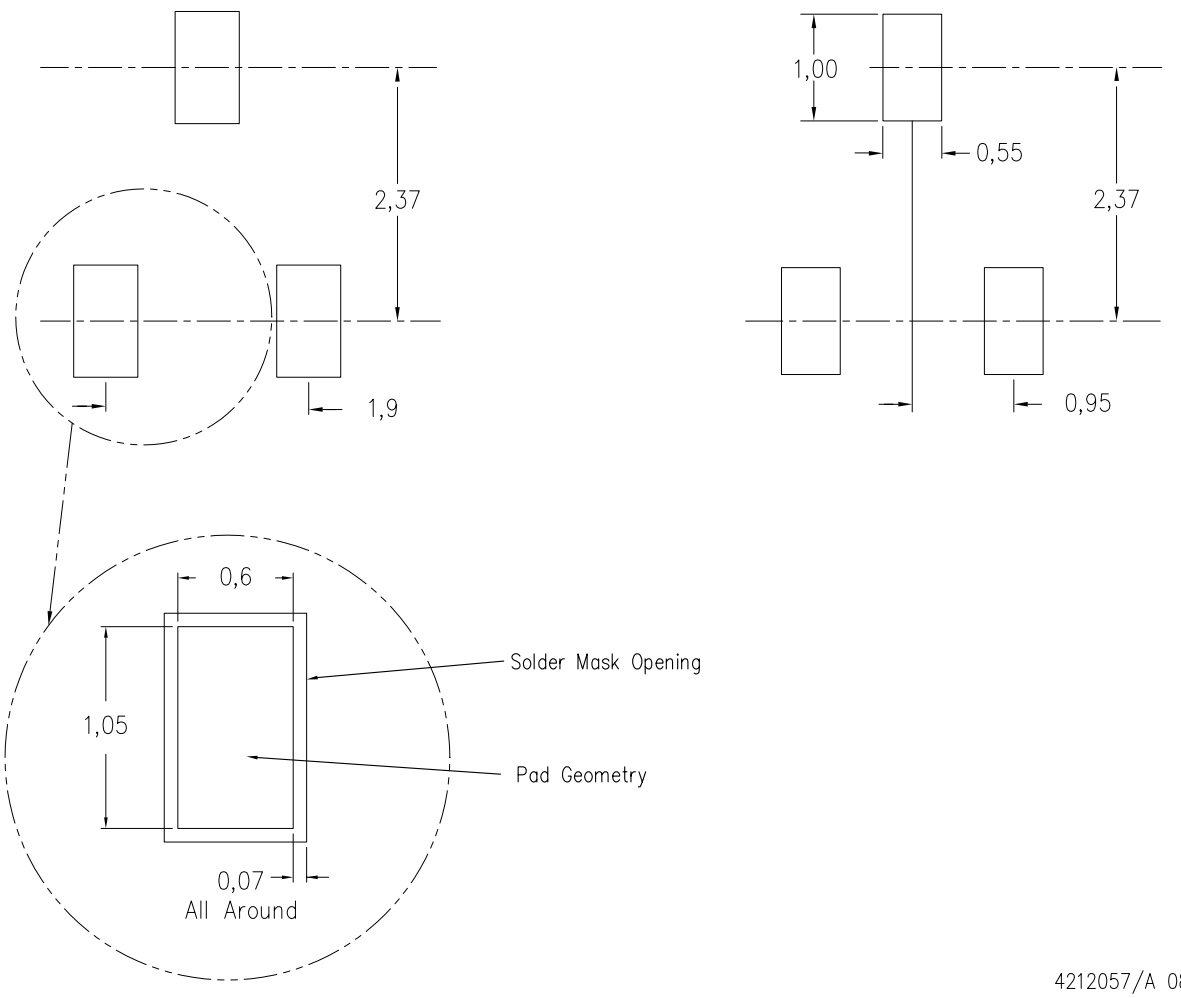
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E2U06QDBZRQ1	SOT-23	DBZ	3	3000	223.0	270.0	35.0

DBZ (R–PDSO–G3) PLASTIC SMALL–OUTLINE



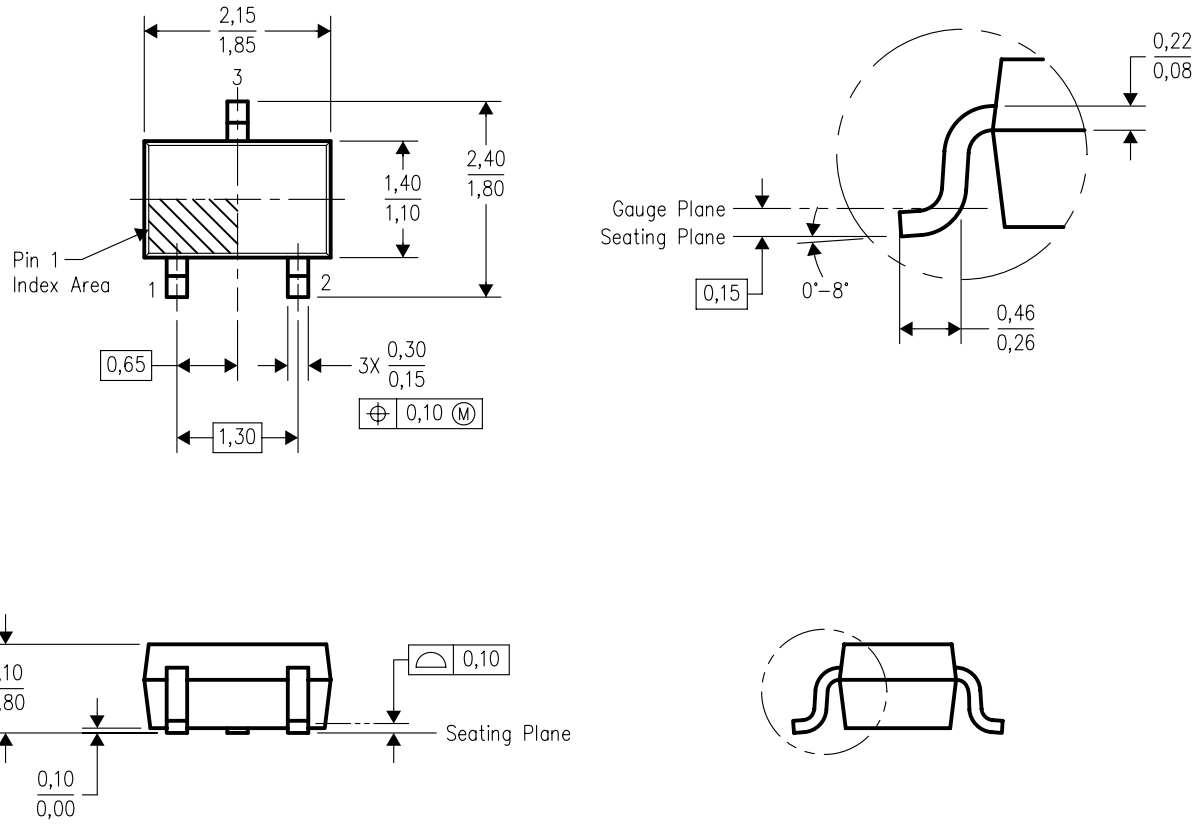
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Lead dimensions are inclusive of plating.
D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

DBZ (R–PDSO–G3) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R–PDSO–G3) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

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