关于 LSI 产品 封装的
热阻、热特性参数

目次

1. 目的

在该应用笔记中，有 ROHM 制造的 LSI 芯片的封装群的热阻和热特性参数的定义及其活用方法。

2. 标准

该应用笔记中记载的内容符合JEDEC标准（JESD 51-2A，3，5，7，9，10）。

3. 用语及其定义

3.1 TA（Ambient air temperature）
周围环境温度。

3.2 TJ（Junction temperature）
PN结的结温。

3.3 TT（The temperature at the top center of the outside surface of the component package ）
封装上表面中心温度。

3.4 θJA（Theta from Junction to Ambient）
从PN结到周围环境的热阻。从多个路径进行散热。

3.5 ΨJT（The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package）
从连接到封装上面中心的热特性参数。因为在封装上面以外也进行热传导，所以根据散热量，值会有变化。

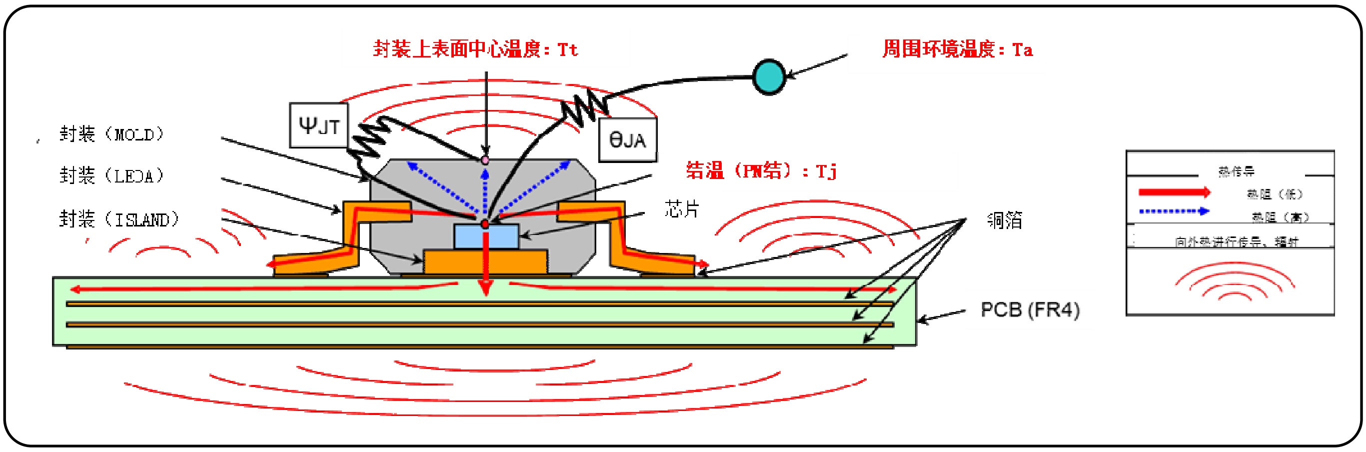


图1. 热阻θJA和热特性参数ψJT的定义（例：HTSOP-J8）

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	7	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance(NOTE 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(NOTE 3)	2s2p(NOTE 4)	
HTSOP-J8				
Junction to Ambient	θ_{JA}	206.4	45.2	°C/W
Junction to Top Characterization Parameter (NOTE 2)	Ψ_{JT}	21	13	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
1s	FR-4	114.3mm x 76.2mm x 1.57mmt

Component trace	
Copper Pattern	Thickness
Component mounting and trace fan-out region	70μm

(Note 4)Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size	Thermal via(NOTE 5)	
			Pitch	Diameter
2s2p	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Component trace		Plane		Backside trace	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Component mounting and trace fan-out region	70μm	74.2mm^2(Square)	35μm	74.2mm^2(Square)	70μm

(Note 5) This through hole via connects with the top copper pattern. The placement and dimensions obey a land pattern.

图2. Datesheet记载例（例：HTSOP-J8）

4. 测量环境（JESD51-2A）

如图3所示，在符合JESD 51-2A（Still-Air）的环境下进行热阻测量。

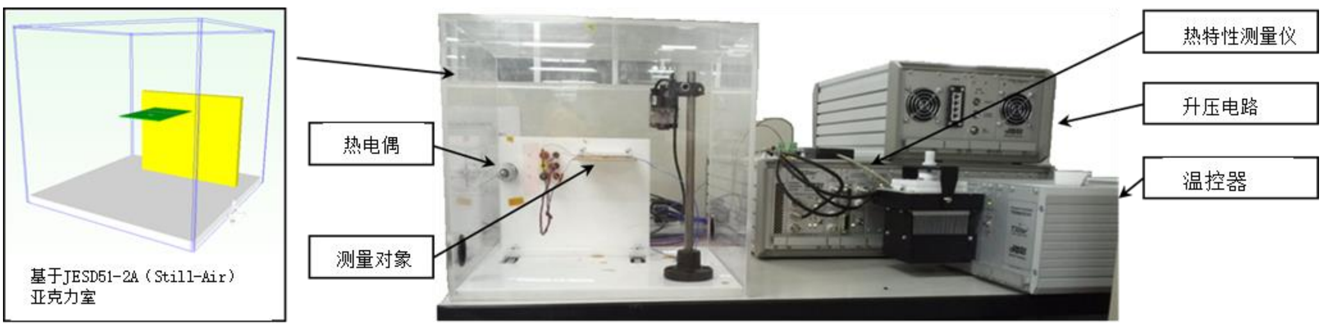


图3. 热阻测量环境

表1. 热阻测量机器

测量仪器	厂家	型号	备注
热特性测量仪	Mentor Graphics	T3Ster	-
恒温器	Mentor Graphics	T3Ster	-
K型热电偶(NOTE1)	坂口热电	K6010	Class1 / Φ0.1mm

(NOTE1)将K型热电偶固定在封装上表面中心，测量封装上表面中心温度T_T。

5. 测量用基板规格

热阻测量是在如表2、图4、图5，符合JESD51-3,5,7,9,10 标准的测量用基板上所实施的。

表2．热阻测量用基板的尺寸（PKG最长边的长度适用于PKG尺寸）

	测定基板	基板材	基板尺寸	热通孔 (NOTE1)		插件通孔 (NOTE2)
				间距	直径	直径
SMD (PKG尺寸＜27mm)	1层基板	FR4	114.3mm x 76.2mm x 1.57mmt	-	-	-
	4层基板		114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm	-
BGA, THD (PKG尺寸≦40mm)	1层基板	FR4	114.5mm x 101.5mm x 1.6mmt	-	-	Φ0.85mm
	4层基板			1.20mm	Φ0.30mm	Φ0.85mm

	基板	1层(表面)铜箔		2层、3层(内层)铜箔		4层(里面)铜箔	
		铜箔种类	铜箔厚度	铜箔种类	铜箔厚度	铜箔种类	铜箔厚度
SMD (PKG尺寸＜27mm)	1层基板	安装Land种类 +引出电极用的配线	70μm	-	-	-	-
	4层基板			74.2mm□(正方形)	35μm	74.2mm□(正方形)	70μm
BGA, THD (PKG尺寸≦40mm)	1层基板	安装Land种类 +引出电极用的配线	70μm	-	-	-	-
	4层基板			99.5mm□(正方形)	35μm	99.5mm□(正方形)	70μm

(NOTE1) 热通孔：通孔是用来连接全层的铜箔。配线要按Land种类来进行。（对应带散热板的封装）

(NOTE2) 插件通孔：THD安装用的通孔、连接到第1层的铜箔。配置和尺寸要按Land种类来进行。

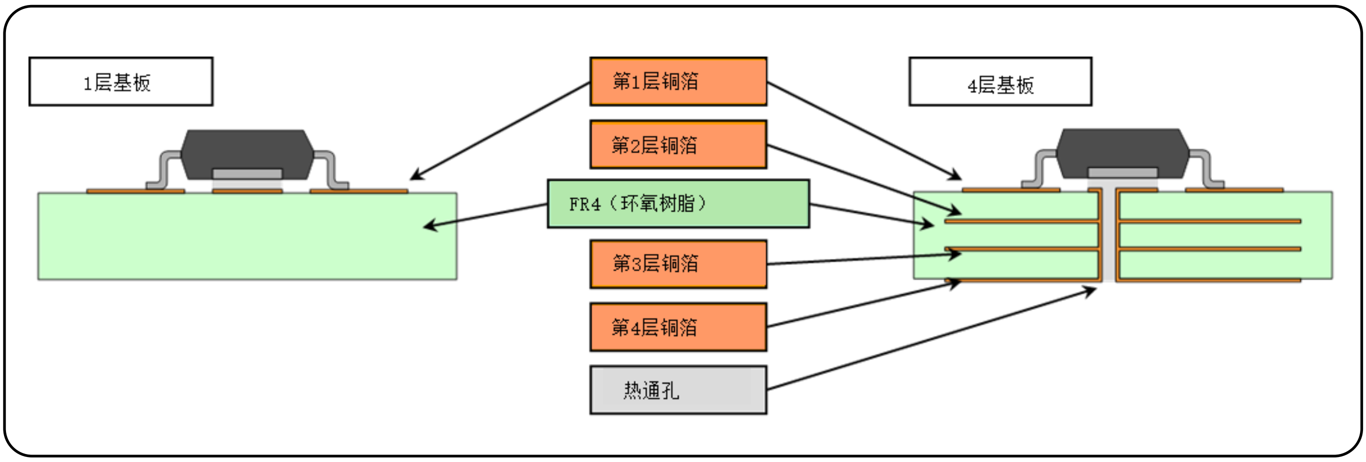


图4．用于热阻测量的基板的截面结构（SMD：带散热器型）

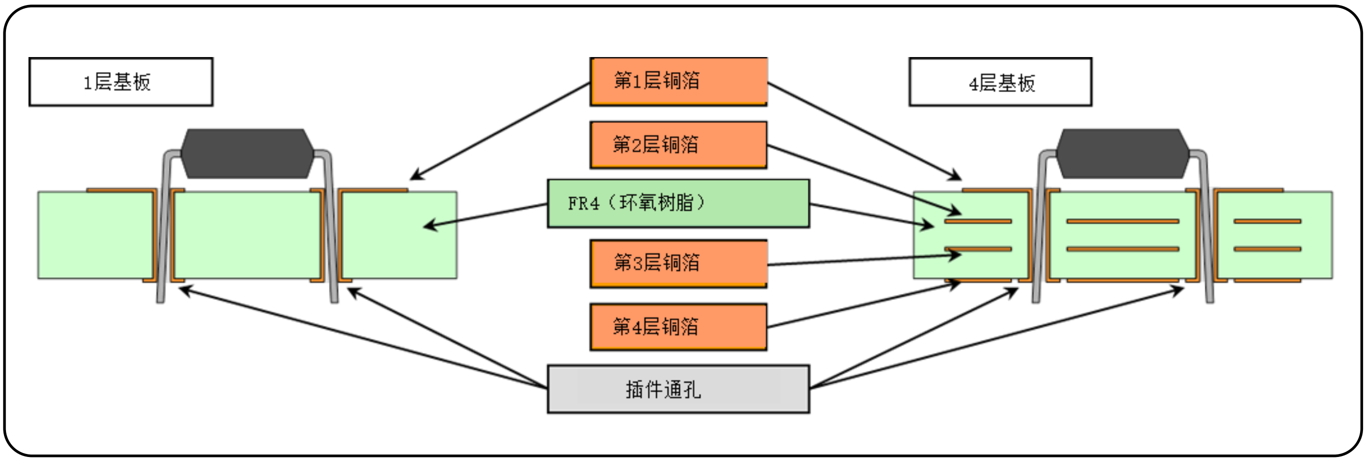


图5．用于热阻测量的基板的截面结构（THD：DIP type）

6. 芯片温度的测量方法

半导体的温度测量方法有以下两种。

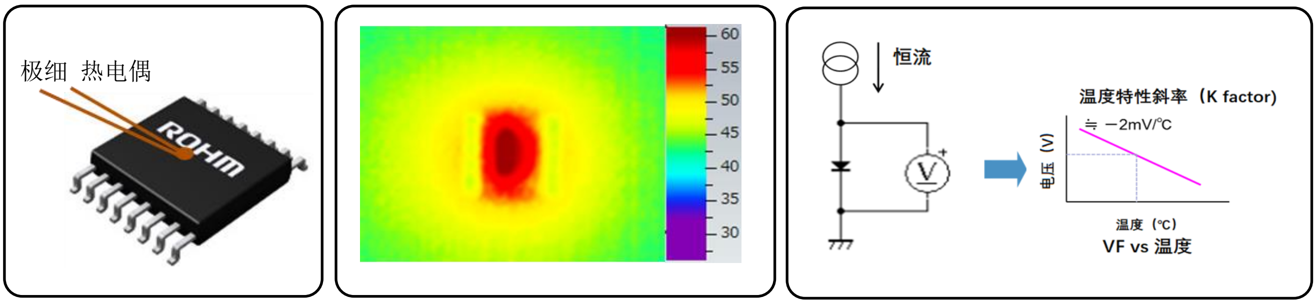
・测量封装表面温度（接触式测量/非接触式测量）

・测量芯片PN结的温度（测量芯片上PN连接的温度）

各自的优点/缺点如表3所示。

表3．不同测量方法的优缺点

测量方法	优点	缺点
测量封装表面温度	容易测量	并不是直接测量结温 容易产生环境误差
测量芯片PN结的温度	直接测量PN结的温度 所以精度很好	在元器件上需要热测量用的端子



测量封装表面温度　　　测量封装表面温度　　　测量芯片PN结的温度

热电偶（接触式）　　　恒温器（非接触式）

图6．各种测量方法图示

通过测量封装表面温度进行半导体的温度测量时，使用热特性参数（ψJT）进行计算。

（※ψJT是表示结温TJ和封装上表面中心温度TT之间的温度差的热特性参数，与罗姆以往记载θJC 是同义词。

只要将热电偶牢固地固定在封装上面中心，就可以高精度地测量封装上面中心温度TT，

可以使用这个热特性参数精确地计算PN结温度。

（但是，热特性参数根据基板的散热性能（层数、铜箔覆盖率、通孔数等）而变化，因此考虑与JEDEC环境的差异。）

$T_J = T_T + \Psi_{JT} * P$　　（T_J：接合温度、T_T：封装上面中心温度、P：消耗功率）

还可以使用热阻（θJA）简单计算PN结温度。

（但是，比起热特性参数，更容易受到与JEDEC环境差异的影响。）

$T_J = T_A + \theta_{JA} * P$　　（T_J：接合温度、T_A：周围环境温度、P：消耗功率）

通过封装表面温度来确认温度限界的裕度的话、可以假设封装表面温度$T_C ≒ T_T$，进行以下计算

$T_{CMAX} = T_{JMAX} - \Psi_{JT} * P$　　（T_{CMAX}：封装表面最高温度、T_{JMAX}：最高结温、P：消耗功率）

从上式可以算出封装表面温度的上限T_{CMAX}。

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