# ADC10080 10-Bit, 80 MSPS, 3V, 78.6 mW A/D Converter

**Check for Samples: ADC10080**

## FEATURES

- **Single +3.0V Operation**
- **Selectable Full-Scale Input Swing**
- **400 MHz −3 dB Input Bandwidth(1)**
- **Low Power Consumption**
- **Standby Mode**
- **On-Chip Reference and Sample-and-Hold Amplifier**
- **Offset Binary or Two's Complement Data Format**
- **Separate Adjustable Output Driver Supply**

## KEY SPECIFICATIONS

- **Resolution: 10 Bits**
- **Conversion Rate: 80 MSPS**
- **Full Power Bandwidth: 400 MHz**
- **DNL: ±0.25 LSB (typ)**
- **SNR ($f_{IN}$ = 10 MHz): 59.5 dB (typ)**
- **SFDR ($f_{IN}$ = 10 MHz): −78.7 dB (typ)**
- **Power Consumption, 80 Msps: 78.6 mW**

## APPLICATIONS

- **Ultrasound and Imaging**
- **Instrumentation**
- **Cellular Base Stations/Communications Receivers**
- **Sonar/Radar**
- **xDSL**
- **Wireless Local Loops**
- **Data Acquisition Systems**
- **DSP Front Ends**

(1) The input bandwidth is limited using a 10 pF capacitor between $V_{IN}^-$ and $V_{IN}^+$.

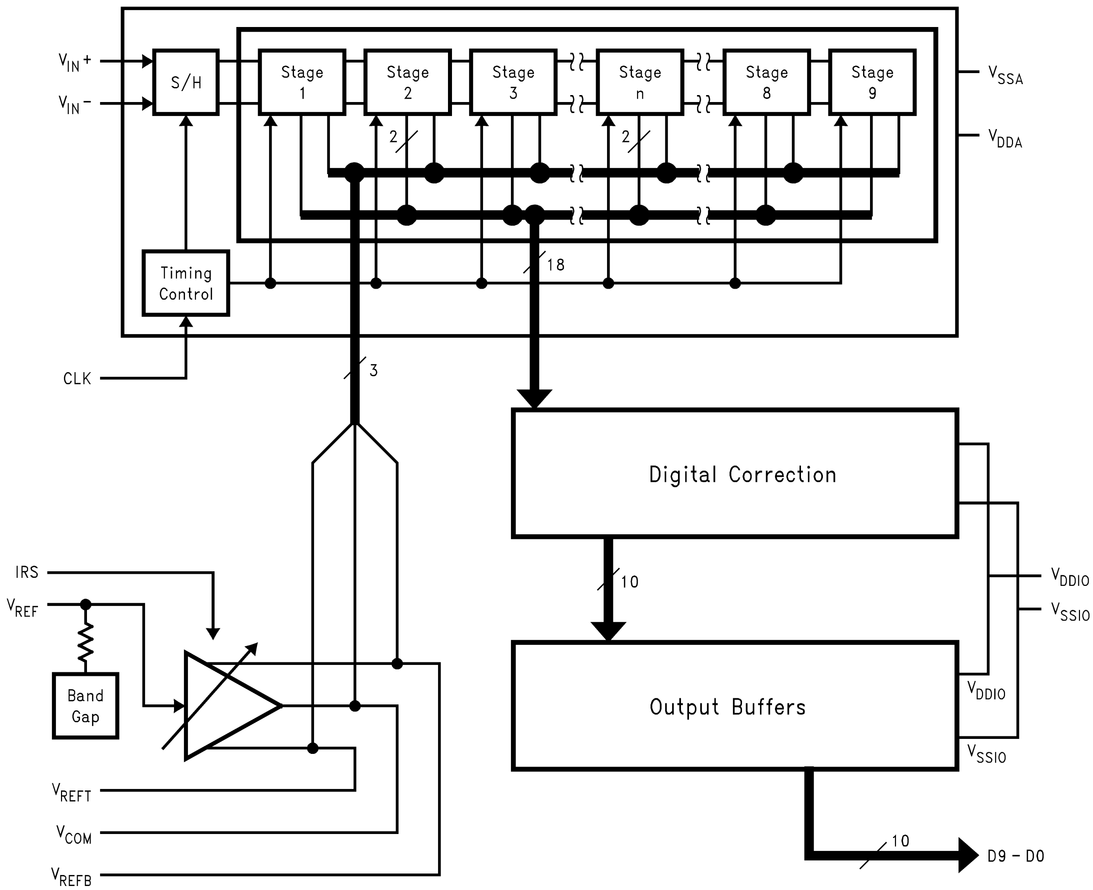
## DESCRIPTION

The ADC10080 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 10-bit digital words at 80 Megasamples per second (MSPS). This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to provide a complete conversion solution and to minimize power consumption, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 400 MHz. Operating on a single 3.0V power supply, this device consumes just 78.6 mW at 80 MSPS, including the reference current. The Standby feature reduces power consumption to just 15 mW.

The differential inputs provide a full scale selectable input swing of 2.0 $V_{P-P}$, 1.5 $V_{P-P}$, 1.0 $V_{P-P}$, with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. An internal +1.2V precision bandgap reference is used to set the ADC full-scale range, and also allows the user to supply a buffered referenced voltage for those applications requiring increased accuracy. The output data format is user choice of offset binary or two's complement.

This device is available in the 28-lead TSSOP package and will operate over the industrial temperature range of −40°C to +85°C.

## BLOCK DIAGRAM




## CONNECTION DIAGRAM

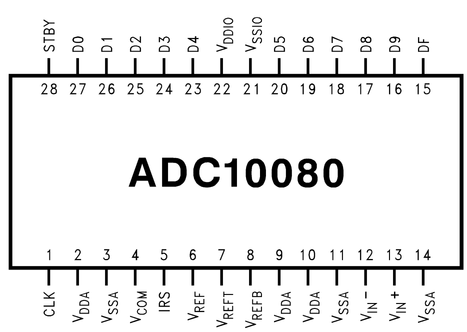
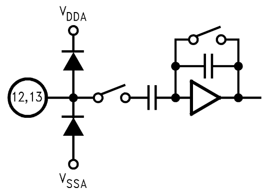
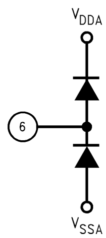
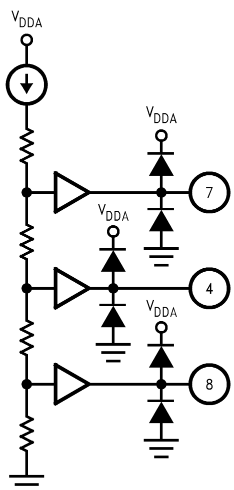
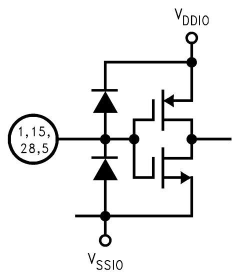
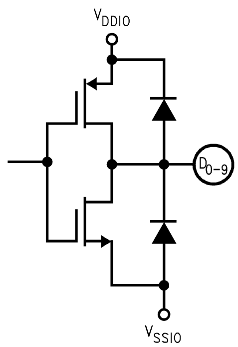



**Figure 1. 28-Lead TSSOP Package Package Number PW**

### Table 1. PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

| Pin No. | Symbol | Equivalent Circuit | Description |
|---|---|---|---|
| **ANALOG I/O** | | | |
| 12 | $V_{IN}^-$ |  | Inverting analog input signal. With a 1.2V reference the full-scale input signal level is a differential 1.0 $V_{P-P}$. This pin may be tied to $V_{COM}$ (pin 4) for single-ended operation. |
| 13 | $V_{IN}^+$ | | Non-inverting analog input signal. With a 1.2V reference the full-scale input signal level is a differential 1.0 $V_{P-P}$. |
| 6 | $V_{REF}$ |  | Reference input. This pin should be bypassed to $V_{SSA}$ with a 0.1 µF monolithic capacitor. $V_{REF}$ is 1.20V nominal. This pin may be driven by a 1.20V external reference if desired. Do not load this pin. |
| 7 | $V_{REFT}$ |  | These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to $V_{SSA}$. These pins should not be loaded. $V_{COM}$ may be used to set the input common input voltage, $V_{CM}$. |
| 4 | $V_{COM}$ | | |
| 8 | $V_{REFB}$ | | |

### Table 1. PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS (continued)

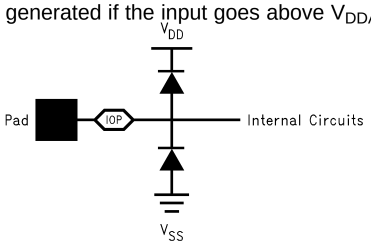
| Pin No. | Symbol | Equivalent Circuit | Description |
|---|---|---|---|
| **DIGITAL I/O** | | | |
| 1 | CLK |  | Digital clock input. The range of frequencies for this input is 20 MHz to 80 MHz. The input is sampled on the rising edge of this input. |
| 15 | DF | | DF = “1” Two’s Complement<br>DF = “0” Offset Binary |
| 28 | STBY | | This is the standby pin. When high, this pin sets the converter into standby mode. When this pin is low, the converter is in active mode. |
| 5 | IRS (Input Range Select) | | IRS = “$V_{DDA}$” 2.0 $V_{P-P}$ differential input range<br>IRS = “$V_{SSA}$” 1.5 $V_{P-P}$ differential input range<br>IRS = “Floating” 1.0 $V_{P-P}$ differential input range<br>If using both $V_{IN}$+ and $V_{IN}$- pins, (or differential mode), then the peak-to-peak voltage refers to the differential voltage ($V_{IN}$+ - $V_{IN}$-). |
| 16–20, 23–27 | D0–D9 |  | Digital output data. D0 is the LSB and D9 is the MSB of the binary output word. |
| **ANALOG POWER** | | | |
| 2, 9, 10 | $V_{DDA}$ | | Positive analog supply pins. These pins should be connected to a quiet 3.0V source and bypassed to analog ground with a 0.1 µF monolithic capacitor located within 1 cm of these pins. A 4.7 µF capacitor should also be used in parallel. |
| 3, 11, 14 | $V_{SSA}$ | | Ground return for the analog supply. |
| **DIGITAL POWER** | | | |
| 22 | $V_{DDIO}$ | | Positive digital supply pins for the ADC10080's output drivers. This pin should be bypassed to digital ground with a 0.1 µF monolithic capacitor located within 1 cm of this pin. A 4.7 µF capacitor should also be used in parallel. The voltage on this pin should never exceed the voltage on $V_{DDA}$ by more than 300 mV. |
| 21 | $V_{SSIO}$ | | The ground return for the digital supply for the output drivers. This pin should be connected to the ground plane, but not near the analog circuitry. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS[(1)(2)(3)]

| | | |
|---|---|---|
| $V_{DDA}$, $V_{DDIO}$ | | 3.9V |
| Voltage on Any Pin to GND | | −0.3V to $V_{DDA}$ or $V_{DDIO}$ +0.3V |
| Input Current on Any Pin | | ±25 mA |
| Package Input Current[(4)] | | ±50 mA |
| Package Dissipation at T = 25°C | | See[(5)] |
| ESD Susceptibility[(6)] | Human Body Model | 2500V |
| | Machine Model | 250V |
| Soldering Temperature Infrared, 10 sec.[(7)] | | 235°C |
| Storage Temperature | | −65°C to +150°C |

(1) All voltages are measured with respect to GND = $V_{SSA}$ = $V_{SSIO}$ = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications
(4) When the voltage at any pin exceeds the power supplies ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($\theta_{JA}$), and the ambient temperature ($T_A$), and can be calculated using the formula $P_D$MAX = ($T_J$max − $T_A$)/$\theta_{JA}$. In the 28-pin TSSOP, $\theta_{JA}$ is 96°C/W, so $P_D$MAX = 1,302 mW at 25°C and 677 mW at the maximum operating ambient temperature of 85°C. Note that the power dissipation of this device under normal operation will typically be about 78.6 mW. The values for maximum power dissipation listed above will be reached only when the ADC10080 is operated in a severe fault condition.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(7) The 235°C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR) the following conditions apply: Maintain the temperature at the top of the package body above 183°C for a minimum of 60 seconds. The temperature measured on the package body must not exceed 220°C. Only one excursion above 183°C is allowed per reflow cycle. The analog inputs are protected as shown below. Input voltage magnitude up to 500 mV beyond the supply rails will not damage this device. However, input errors will be generated if the input goes above $V_{DDA}$ or $V_{DDIO}$ and below $V_{SSA}$ or $V_{SSIO}$.




## OPERATING RATINGS[(1)(2)]

| | |
|---|---|
| Operating Temperature Range | −40°C ≤ $T_A$ ≤ +85°C |
| $V_{DDA}$ (Supply Voltage) | +2.7V to +3.6V |
| $V_{DDIO}$ (Output Driver Supply Voltage) | +2.5V to $V_{DDA}$ |
| $V_{REF}$ | 1.20V |
| $\lvert V_{SSA}–V_{SSIO}\rvert$ | ≤ 100 mV |
| Clock Duty Cycle | 30 to 70 % |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = $V_{SSA}$ = $V_{SSIO}$ = 0V, unless otherwise specified.

## CONVERTER ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO} = 0V$[1][1][2], $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.20V$ (External), $f_{CLK} = 80$ MHz, 50% Duty Cycle, $C_L = 10$ pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$:** all other limits $T_A = 25°C$.[3][1][2]

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC CONVERTER CHARACTERISTICS** | | | | | | |
| | No Missing Codes ensured | | **10** | | | Bits |
| INL | Integral Non-Linearity[4] | $F_{IN}$ = 500 kHz, 0 dB Full Scale | **−1.4** | ±0.5 | **+1.6** | LSB |
| DNL | Differential Non-Linearity | $F_{IN}$ = 500 kHz, 0 dB Full Scale | **−0.9** | ±0.25 | **+1.0** | LSB |
| GE | Gain Error | Positive Error | **−1.6** | +0.5% | **+2.0** | % FS |
| | | Negative Error | **−1.6** | −0.07% | **+2.0** | % FS |
| OE | Offset Error ($V_{IN}$+ = $V_{IN}$−) | | **−1.4** | 0.11 | **1.7** | % FS |
| | Under Range Output Code | | | 0 | | |
| | Over Range Output Code | | | 1023 | | |
| FPBW | Full Power Bandwidth | | | 400 | | MHz |
| **REFERENCE AND INPUT CHARACTERISTICS** | | | | | | |
| $V_{CM}$ | Common Mode Input Voltage | | 0.5 | | 1.5 | V |
| $V_{COM}$ | Output Voltage for use as an input common mode voltage[5] | | | 1.45 | | V |
| $V_{REF}$ | Internal Reference Voltage | | | 1.2 | | V |
| | External Reverence Voltage | | 1.0 | 1.2 | 1.5 | V |
| $V_{REFTC}$ | Internal Reference Voltage Temperature Coefficient | | | ±80 | | ppm/°C |
| $C_{IN}$ | $V_{IN}$ Input Capacitance (each pin to $V_{SSA}$) | | | 4 | | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| $I_{VDDA}$ | Analog Supply Current | STBY = 1 | | 5 | **6.3** | mA |
| | | STBY 0 | | 25 | **32** | mA |
| $I_{VDDIO}$ | Digital Supply Current[6] | STBY = 1, $f_{IN}$= 0 Hz | | 0 | | mA |
| | | STBY 0, $f_{IN}$ = 0 Hz | | 1.2 | **1.4** | mA |
| PWR | Power Consumption[7] | STBY = 1 | | 15 | **18.9** | mW |
| | | STBY = 0 | | 78.6 | **100.2** | mW |

(1) With the test condition for 2 $V_{P-P}$ differential input, the 10-bit LSB is 1.95 mV.
(2) Typical figures are at $T_A = T_J = 25°C$ and represent most likely parametric norms. Test limits are ensured to AOQL (Average Outgoing Quality Level).
(3) To ensure accuracy, it is required that $|V_{DDA}–V_{DDIO}| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.
(4) Timing specifications are tested at TTL logic levels, $V_{IL}$ = 0.4V for a falling edge, and $V_{IH}$ = 2.4V for a rising edge.
(5) $V_{COM}$ is typical value, measured at room temperature. It is not ensured by test. This pin should not be loaded.
(6) $I_{VDDIO}$ is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, $V_{DDIO}$, and the rate at which the outputs are switching (which is signal dependent). $I_{DR} = V_{DR}$ x ($C_0$ x $f_0$ + $C_1$ x $f_1$ + $C_2$ + $f_2$ +....$C_{11}$ x $f_{11}$) where $V_{DR}$ is the output driver supply voltage, $C_n$ is the total load capacitance on the output pin, and $f_n$ is the average frequency at which the pin is toggling.
(7) Power consumption includes output driver power. ($f_{IN}$ = 0 MHz).

## DC AND LOGIC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO}$ = 0V, $V_{DDA}$ = +3.0V, $V_{DDIO}$ = +2.5V, $V_{IN}$ = 2 $V_{P-P}$, STBY = 0V, $V_{REF}$ = 1.20V (External), $f_{CLK}$ = 80 MHz, 50% Duty Cycle, $C_L$ = 10 pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$**: all other limits $T_A$ = 25°C (1)(2)(3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CLK, DF, STBY, SENSE** | | | | | | |
| | Logical “1” Input Voltage | | **2** | | | V |
| | Logical “0” Input Voltage | | | | **0.8** | V |
| | Logical “1” Input Current | | | | **+10** | µA |
| | Logical “0” Input Current | | **−10** | | | µA |
| **D0–D9 OUTPUT CHARACTERISTICS** | | | | | | |
| | Logical “1” Output Voltage | $I_{OUT}$ = −0.5 mA | **$V_{DDIO}$−0.2** | | | V |
| | Logical “0” Output Voltage | $I_{OUT}$ = 1.6 mA | | | **0.4** | V |
| **DYNAMIC CONVERTER CHARACTERISTICS (4)** | | | | | | |
| ENOB | Effective Number of Bits | $f_{IN}$ = 10.0 MHz | 9.3<br>**9.1** | 9.5 | | Bits |
| | | $f_{IN}$ = 39 MHz | 9.3<br>**8.9** | 9.5 | | Bits |
| SNR | Signal-to-Noise Ratio | $f_{IN}$ = 10.0 MHz | 58.5<br>**57.7** | 59.5 | | dB |
| | | $f_{IN}$ = 39 MHz | 58.0<br>**57.0** | 59.2 | | dB |
| SINAD | Signal-to-Noise Ratio + Distortion | $f_{IN}$ = 10.0 MHz | 58.0<br>**56.3** | 59.2 | | dB |
| | | $f_{IN}$ = 39 MHz | 57.6<br>**55.6** | 59.0 | | dB |
| 2nd HD | 2nd Harmonic | $f_{IN}$ = 10.0 MHz | −74.1<br>**−68.7** | −87.0 | | dBc |
| | | $f_{IN}$ = 39 MHz | −69.5<br>**−62.7** | −82 | | dBc |
| 3rd HD | 3rd Harmonic | $f_{IN}$ = 10.0 MHz | −65<br>**−58.6** | −72.3 | | dBc |
| | | $f_{IN}$ = 39 MHz | −64.7<br>**−57.6** | −74.5 | | dBc |
| THD | Total Harmonic Distortion (First 6 Harmonics) | $f_{IN}$ = 10.0 MHz | −65<br>**−58.6** | −72.3 | | dB |
| | | $f_{IN}$ = 39 MHz | −64.7<br>**−57.6** | −74.5 | | dB |
| SFDR | Spurious Free Dynamic Range (Excluding 2nd and 3rd Harmonic) | $f_{IN}$ = 10.0 MHz | −70.8<br>**−68.2** | −78.7 | | dBc |
| | | $f_{IN}$ = 39 MHz | −72<br>**−68** | −78.8 | | dBc |

(1) To ensure accuracy, it is required that $|V_{DDA}–V_{DDIO}|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(2) With the test condition for 2 $V_{P-P}$ differential input, the 10-bit LSB is 1.95 mV.
(3) Typical figures are at $T_A = T_J$ = 25°C and represent most likely parametric norms. Test limits are ensured to AOQL (Average Outgoing Quality Level).
(4) Optimum dynamic performance will be obtained by keeping the reference input at +1.2V.

## AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO}$ = 0V, $V_{DDA}$ = +3.0V, $V_{DDIO}$ = +2.5V, $V_{IN}$ = 2 $V_{P-P}$, STBY = 0V, $V_{REF}$ = 1.20V, (Externally Supplied) $f_{CLK}$ = 80 MHz, 50% Duty Cycle, $C_L$ = 10 pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$:** all other limits $T_A$ = 25°C (1)(2) (3)(4)

| Symbol | Parameter | Conditions | Min (4) | Typ (4) | Max (4) | Units |
|---|---|---|---|---|---|---|
| **CLK, DF, STBY, SENSE** | | | | | | |
| $f_{CLK}1$ | Maximum Clock Frequency | | | | 80 | MHz (min) |
| $f_{CLK}2$ | Minimum Clock Frequency | | | 20 | | MHz |
| $t_{CH}$ | Clock High Time | | | 6.25 | | ns |
| $t_{CL}$ | Clock Low Time | | | 6.25 | | ns |
| | Conversion Latency | | | | **6** | Cycles |
| $t_{OD}$ | Data Output Delay after a Rising Clock Edge | T = 25°C | 2 | 3.5 | 5 | ns |
| | | | **1** | | **6** | ns |
| $t_{AD}$ | Aperture Delay | | | 1 | | ns |
| $t_{AJ}$ | Aperture Jitter | | | 2 | | ps (RMS) |
| | Over Range Recovery Time | Differential $V_{IN}$ step from ±3V to 0V to get accurate conversion | | 1 | | Clock Cycle |
| $t_{STBY}$ | Standby Mode Exit Cycle | | | 20 | | Cycles |

(1) To ensure accuracy, it is required that $|V_{DDA}–V_{DDIO}|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(2) With the test condition for 2 $V_{P-P}$ differential input, the 10-bit LSB is 1.95 mV.
(3) Typical figures are at $T_A = T_J$ = 25°C and represent most likely parametric norms. Test limits are ensured to AOQL (Average Outgoing Quality Level).
(4) Timing specifications are tested at TTL logic levels, $V_{IL}$ = 0.4V for a falling edge, and $V_{IH}$ = 2.4V for a rising edge.

## Specification Definitions

**APERTURE DELAY** is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

**APERTURE JITTER (APERTURE UNCERTAINTY)** is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

**COMMON MODE VOLTAGE ($V_{CM}$)** is the d.c. potential present at both signal inputs to the ADC.

**CONVERSION LATENCY** See PIPELINE DELAY.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB.

**DUTY CYCLE** is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**FULL POWER BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

**GAIN ERROR** is the deviation from the ideal slope of the transfer function. It can be calculated as:

$$\text{Gain Error} = \text{Positive Full-Scale Error} - \text{Negative Full-Scale Error} \quad (1)$$

**INTEGRAL NON LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from negative full scale through positive full scale. The deviation of any given code from this straight line is measured from the center of that code value.

**MISSING CODES** are those output codes that will never appear at the ADC outputs. The ADC10080 is ensured not to have any missing codes.

**NEGATIVE FULL SCALE ERROR** is the difference between the input voltage ($V_{IN}^+ - V_{IN}^-$) just causing a transition from negative full scale to the first code and its ideal value of 0.5 LSB.

**OFFSET ERROR** is the input voltage that will cause a transition from a code of 01 1111 1111 to a code of 10 0000 0000.

**OUTPUT DELAY** is the time delay after the rising edge of the clock before the data update is presented at the output pins.

**PIPELINE DELAY (LATENCY)** is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

**POSITIVE FULL SCALE ERROR** is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

**SIGNAL TO NOISE RATIO (SNR)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

**SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD)** Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

**TOTAL HARMONIC DISTORTION (THD)** is the ratio, expressed in dBc, of the rms total of the first six harmonic levels at the output to the level of the fundamental at the output. THD is calculated as:

$$\mathrm{THD} = 20 \times \log \sqrt{\frac{f_2^2 + f_3^2 + \ldots + f_6^2}{f_1^2}}$$

where

- $f_1$ is the RMS power of the fundamental (output) frequency and $f_2$ through $f_6$ are the RMS power in the first 6 harmonic frequencies. (2)

**Second Harmonic Distortion (2nd Harm)** is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

**Third Harmonic Distortion (3rd Harm)** is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

## Timing Diagram

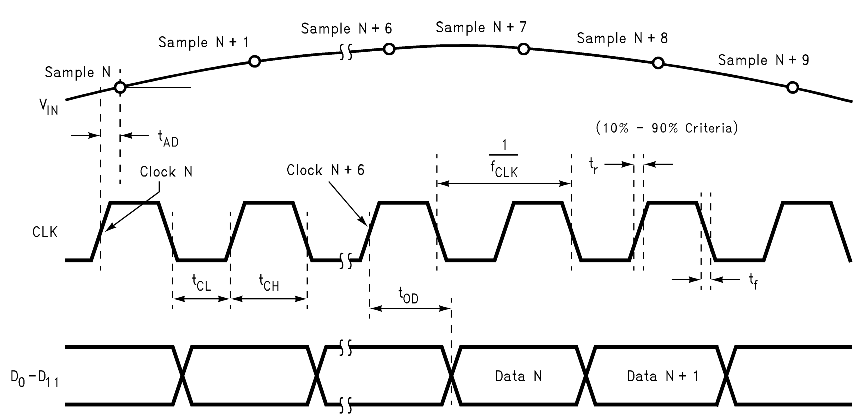



**Figure 2. Clock and Data Timing Diagram**

## Transfer Characteristics

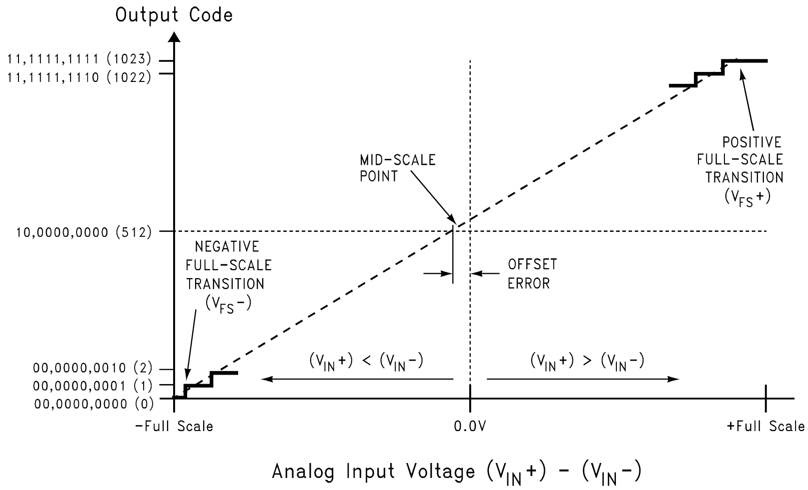



**Figure 3. Input vs. Output Transfer Characteristic**

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.2V$ (External), $f_{CLK} = 80$ MHz, $f_{IN}$ , 39 MHz, 50% Duty Cycle.

**DNL**

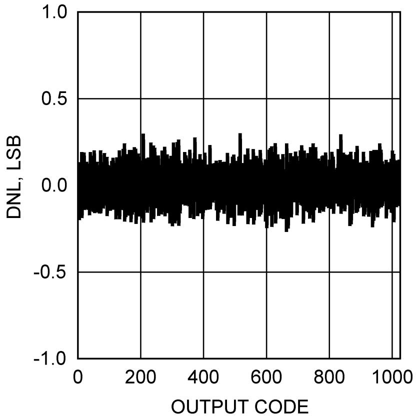



**Figure 4.**

**DNL vs. $f_{CLK}$**

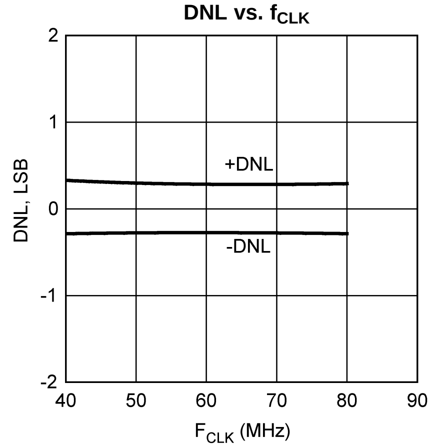



**Figure 5.**

**DNL vs. Clock Duty Cycle (DC input)**

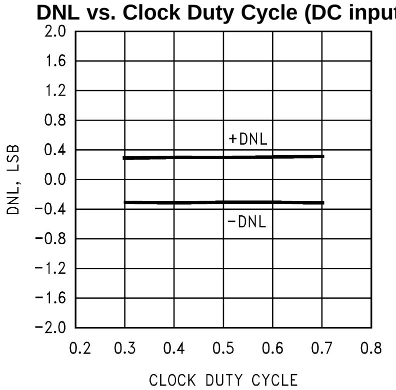



**Figure 6.**

**DNL vs. Temperature**

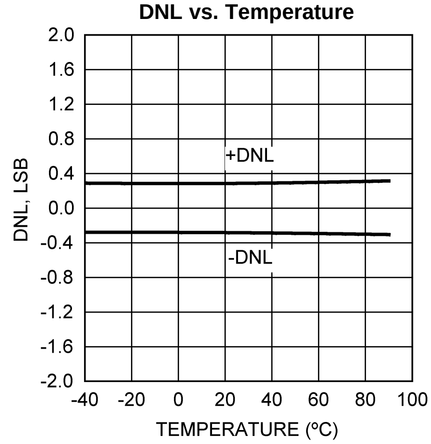



**Figure 7.**

**INL**

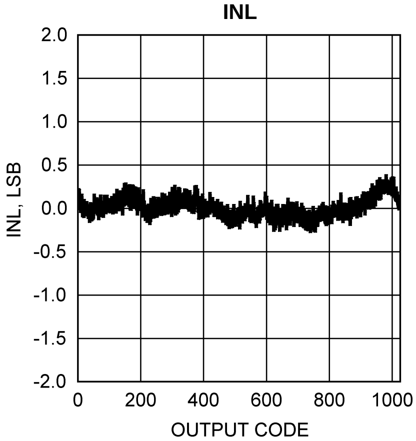



**Figure 8.**

**INL vs. $f_{CLK}$**

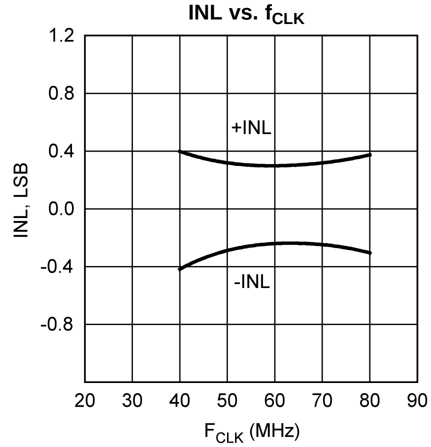



**Figure 9.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.2V$ (External), $f_{CLK} = 80$ MHz, $f_{IN}$ , 39 MHz, 50% Duty Cycle.

**INL vs. Clock Duty Cycle**

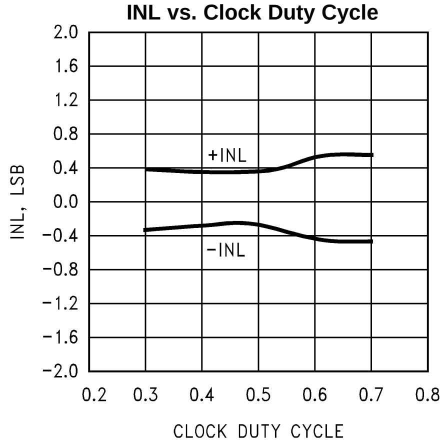



**Figure 10.**

**SNR vs. $V_{DDIO}$**

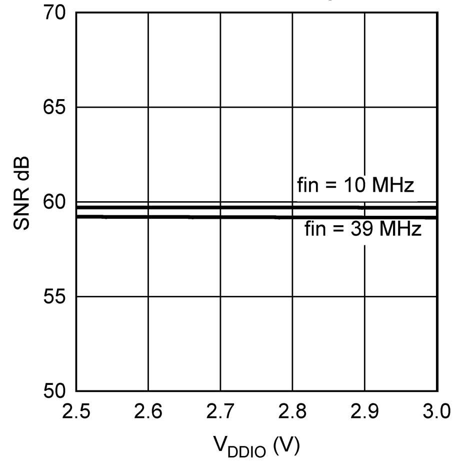



**Figure 11.**

**SNR vs. $V_{DDA}$**

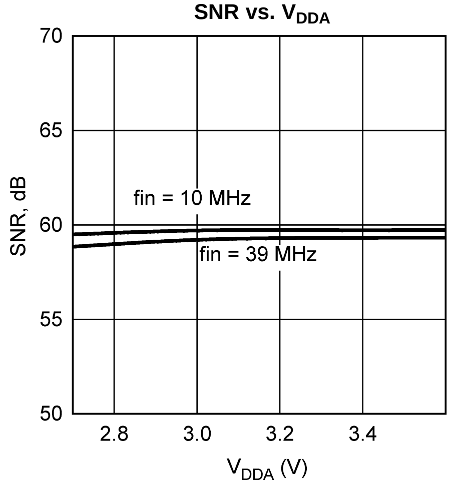



**Figure 12.**

**SNR vs. $f_{CLK}$**

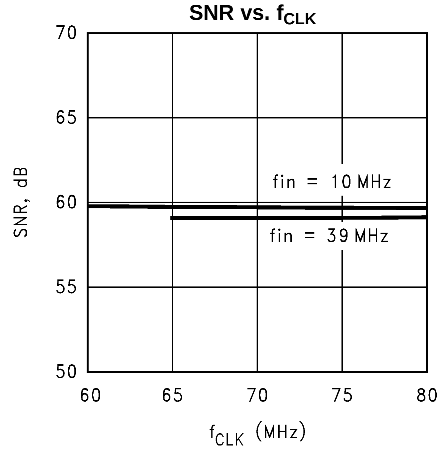



**Figure 13.**

**INL vs. Temperature**

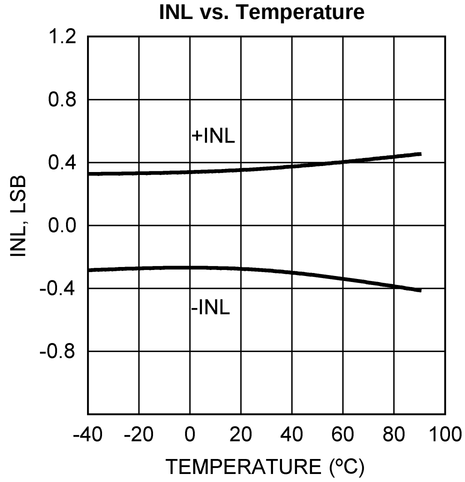



**Figure 14.**

**SNR vs. Clock Duty Cycle**

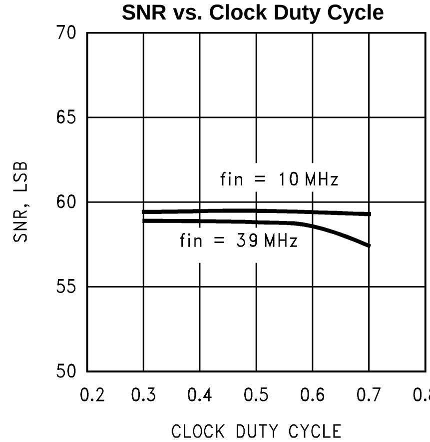



**Figure 15.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO}$ = 0V, $V_{DDA}$ = +3.0V, $V_{DDIO}$ = +2.5V, $V_{IN}$ = 2 $V_{P-P}$, STBY = 0V, $V_{REF}$ = 1.2V (External), $f_{CLK}$ = 80 MHz, $f_{IN}$ , 39 MHz, 50% Duty Cycle.

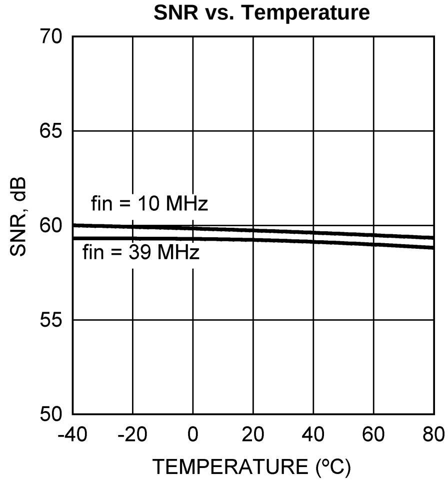



**Figure 16.**

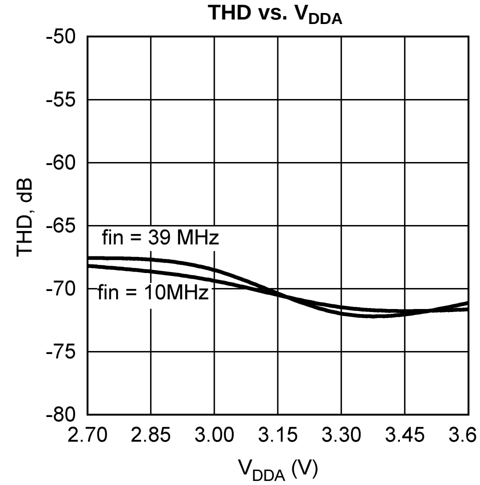



**Figure 17.**

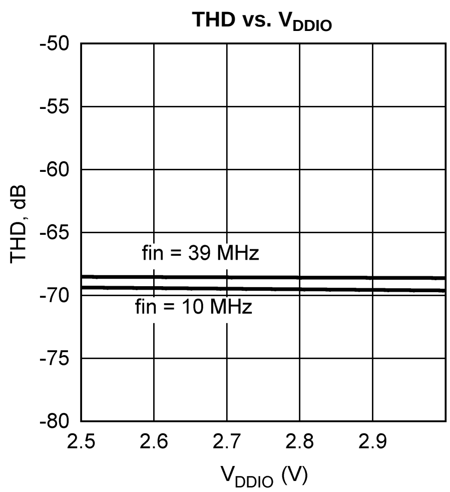



**Figure 18.**

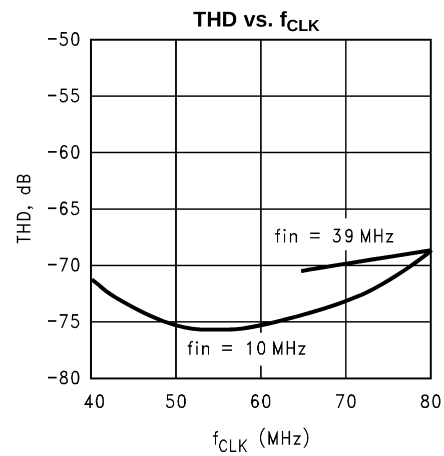



**Figure 19.**

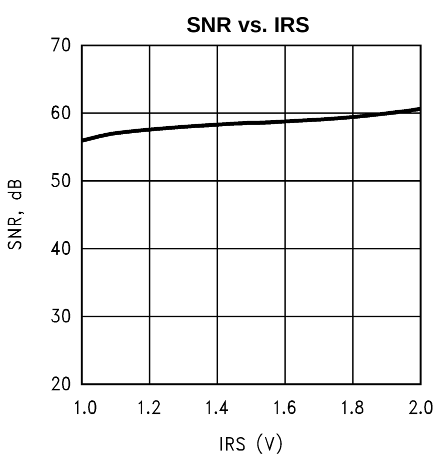



**Figure 20.**

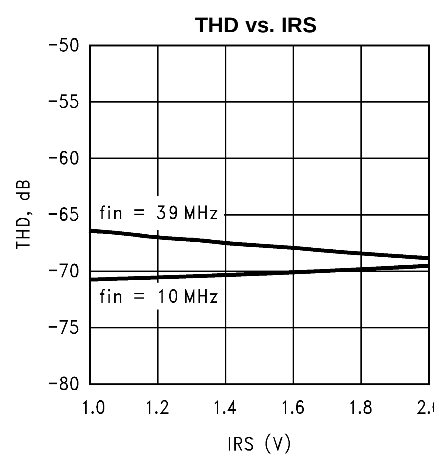



**Figure 21.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.2V$ (External), $f_{CLK} = 80$ MHz, $f_{IN}$ , 39 MHz, 50% Duty Cycle.

**SINAD vs. $V_{DDA}$**

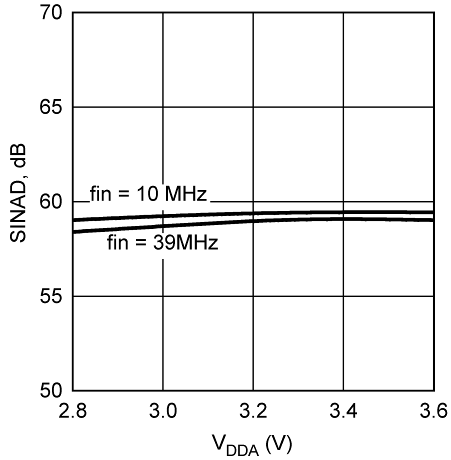



**Figure 22.**

**SINAD vs. $V_{DDIO}$**

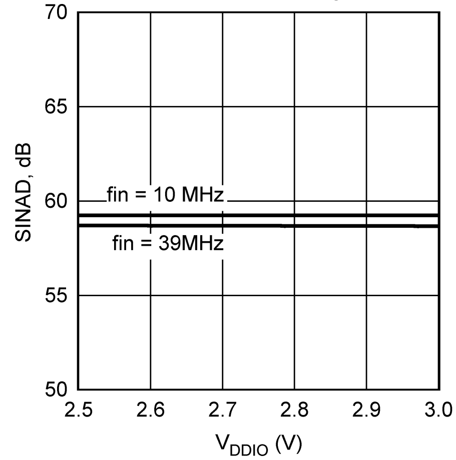



**Figure 23.**

**THD vs. Clock Duty Cycle**

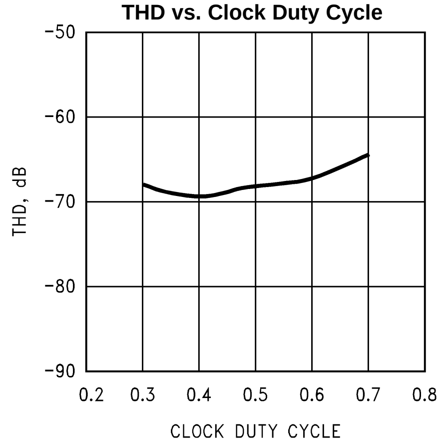



**Figure 24.**

**SINAD vs. Clock Duty Cycle**

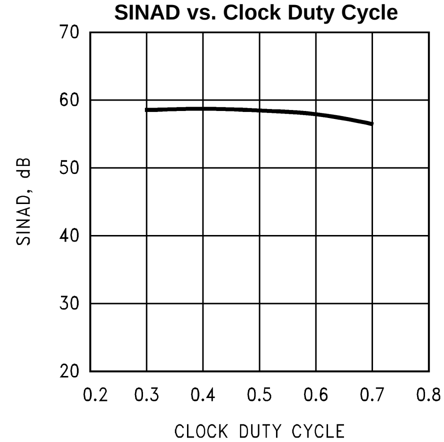



**Figure 25.**

**THD vs. Temperature**

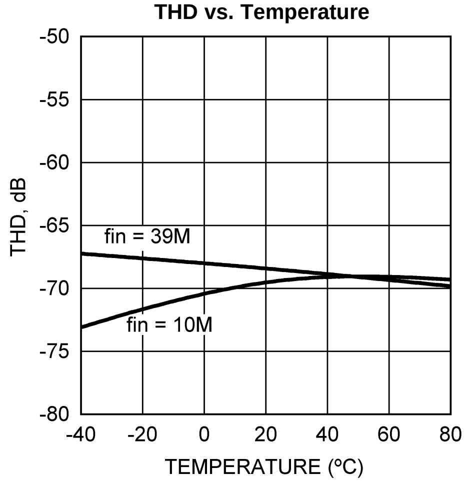



**Figure 26.**

**SINAD vs. Temperature**

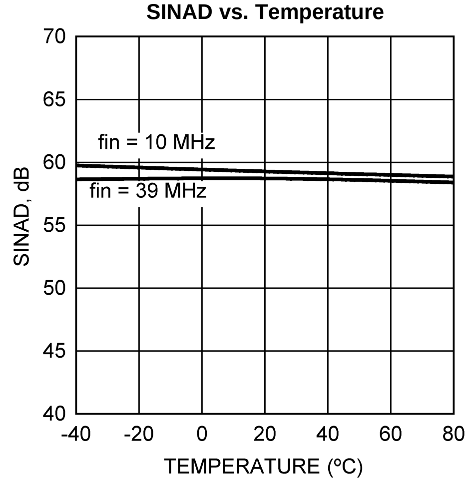



**Figure 27.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.2V$ (External), $f_{CLK} = 80$ MHz, $f_{IN}$ , 39 MHz, 50% Duty Cycle.

**SINAD vs. $f_{CLK}$**

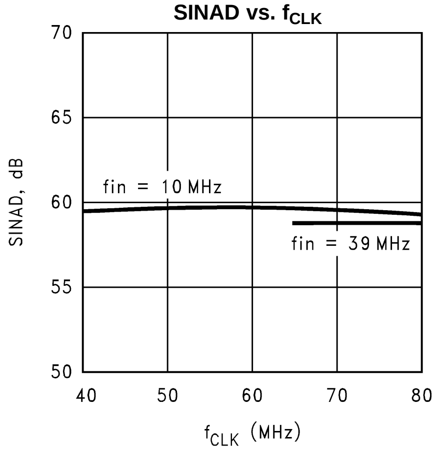



**Figure 28.**

**SFDR vs. $V_{DDIO}$**

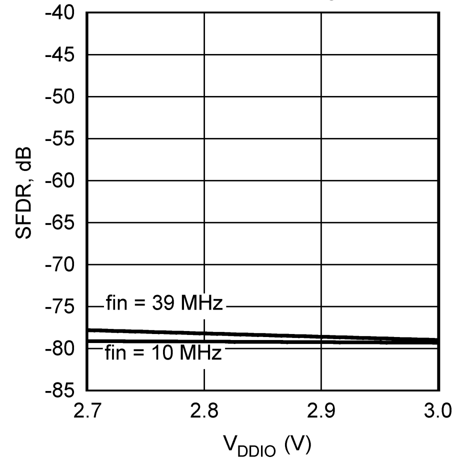



**Figure 29.**

**SINAD vs. IRS**

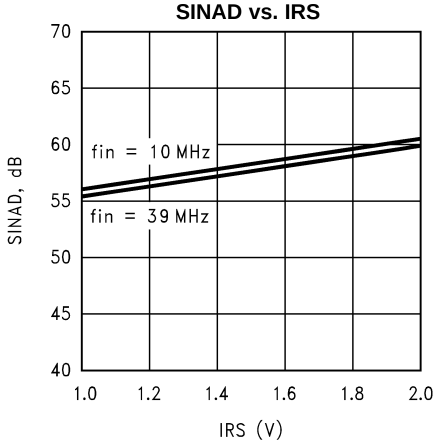



**Figure 30.**

**SFDR vs. $f_{CLK}$**

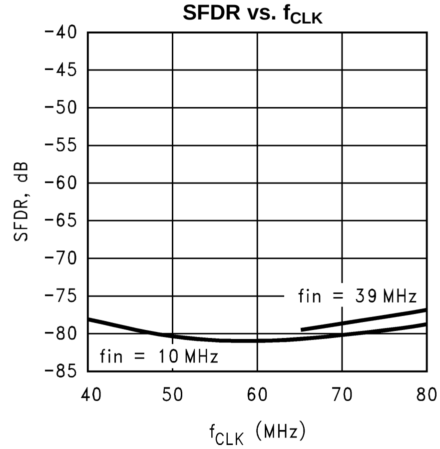



**Figure 31.**

**SFDR vs. $V_{DDA}$**

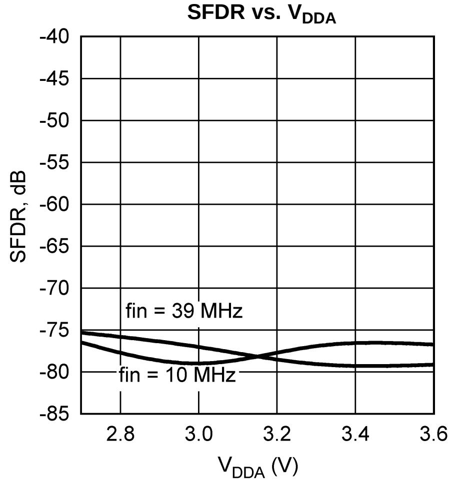



**Figure 32.**

**SFDR vs. IRS**

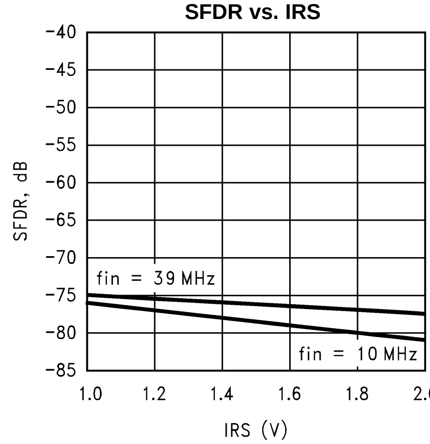



**Figure 33.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2\ V_{P-P}$, STBY = 0V, $V_{REF} = 1.2V$ (External), $f_{CLK} = 80$ MHz, $f_{IN}$ , 39 MHz, 50% Duty Cycle.

**SFDR vs. Clock Duty Cycle**

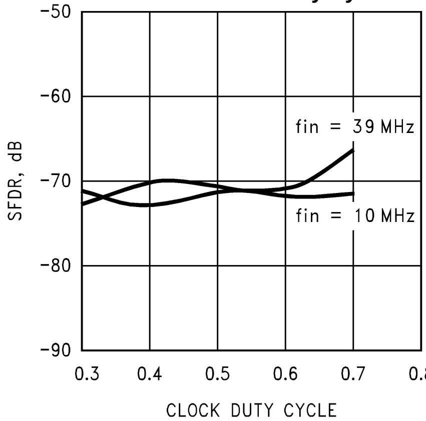



**Figure 34.**

**Spectral Response @ 10 MHz Input**

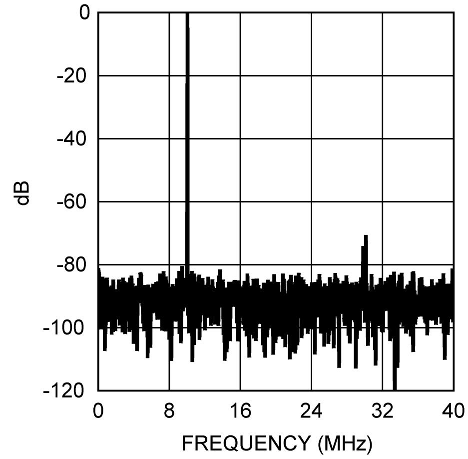



**Figure 35.**

**SFDR vs. Temperature**

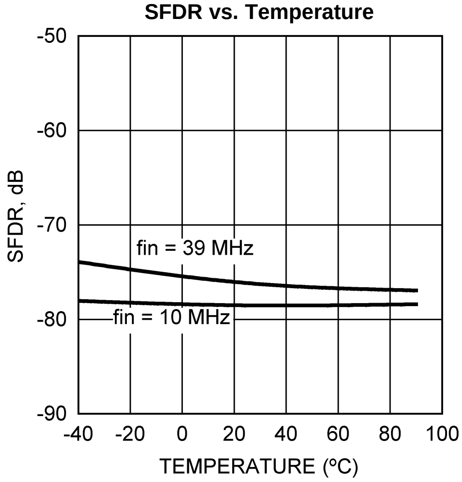



**Figure 36.**

**Spectral Response @ 39 MHz Input**

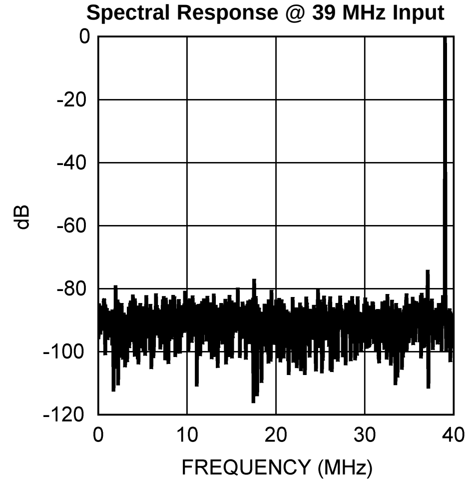



**Figure 37.**

**Power Consumption vs. $f_{CLK}$**

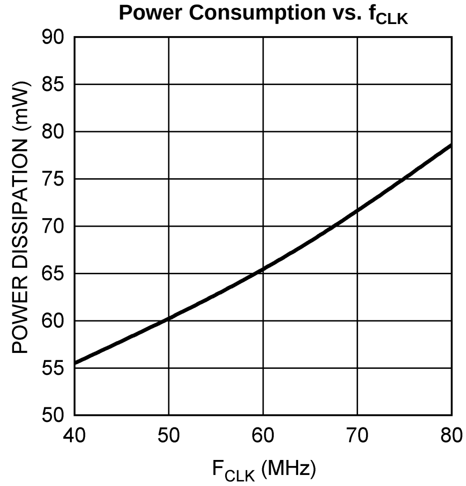



**Figure 38.**

## FUNCTIONAL DESCRIPTION

The ADC10080 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. Differential analog input signals are digitized to 10 bits. In differential mode each analog input signal should have a peak-to-peak voltage equal to 1.0V, 0.75V or 0.5V, depending on the state of the IRS pin (pin 5), and be centered around $V_{CM}$ and be 180° out of phase with each other. If single ended operation is desired, $V_{IN}$- may be tied to the $V_{COM}$ pin (pin 4). A single ended input signal may then be applied to $V_{IN}$+, and should have a mid range value of $V_{COM}$. The signal amplitude should be 2.0V, 1.5V or 1.0V peak-to-peak, depending on the state or the IRS pin (pin 5).

## APPLICATION INFORMATION

### ANALOG INPUTS

The ADC10080 has two analog signal inputs, $V_{IN}$+ and $V_{IN}$−. These two pins form a differential input pair. There is one common mode pin $V_{COM}$ that may be used to set the common mode input voltage.

### $V_{COM}$ PIN

This pin supplies a voltage for possible use to set the common mode input voltage. This pin may also be connected to $V_{IN}$-, so that $V_{IN}$+ may be used as a single ended input. This pin should be bypassed with at least a 0.1 uF capacitor. Do not load this pin.

### SIGNAL INPUTS

The signal inputs are $V_{IN}$+ and $V_{IN}$−. The input signal amplitude is defined as $V_{IN}$+ − $V_{IN}$− and is represented in Figure 39:

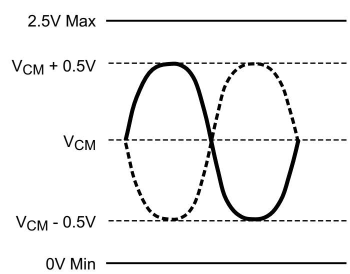



**Figure 39. Input Voltage Waveforms for a 2$V_{P-P}$ Differential Input**

A single ended input signal is shown in Figure 40.

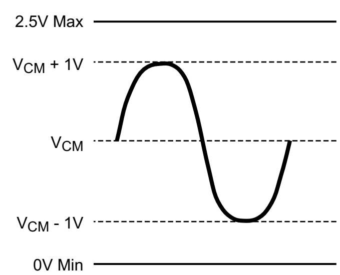



**Figure 40. Input Voltage Waveform for a 2$V_{P-P}$ Single Ended Input**

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To prevent this, use 18Ω series resistors at each of the signal input pins with a 25 pF capacitor across the inputs, as shown in Figure 41. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. The two 18Ω resistors and the 25 pF capacitor form a low-pass filter with a -3 dB frequency of 177 MHz.

### CLK PIN

The CLK signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the frequency range indicated in the AC Electrical Characteristics Table with rise and fall times of less than 2 ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°. The CLK signal also drives an internal state machine. If the CLK is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate. The duty cycle of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC10080 is designed to maintain performance over a range of duty cycles. While it is specified and performance is ensured with a 50% clock duty cycle, performance is typically maintained with minimum clock low and high times indicated in the AC Electrical Characteristics Table. Both minimum high and low times may not be held simultaneously.

### STBY PIN

The STBY pin, when high, holds the ADC10080 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 15 mW. The output data pins are undefined in this mode. Power consumption during power-down is not affected by the clock frequency, or by whether there is a clock signal present. The data in the pipeline is corrupted while in power down.

### DF PIN

The DF (Data Format) pin, when high, forces the ADC10080 to output the 2's complement data format. When DF is tied low, the output format is offset binary.

### IRS PIN

The IRS (Input Range Select) pin defines the input signal amplitude that will produce a full scale output. The table below describes the function of the IRS pin.

**Table 2. IRS Pin Functions**

| IRS Pin | Full-Scale Input |
|---|---|
| $V_{DDA}$ | $2.0V_{P-P}$ |
| $V_{SSA}$ | $1.5V_{P-P}$ |
| Floating | $1.0V_{P-P}$ |

### OUTPUT PINS

The ADC10080 has 10 TTL/CMOS compatible Data Output pins. The offset binary data is present at these outputs while the DF and STBY pins are low. Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through $V_{DDIO}$ and $V_{SSIO}$. These large charging current spikes can cause on-chip noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 10 pF/pin will cause $t_{OD}$ to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance. To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by minimizing load capacitance and by connecting buffers between the ADC outputs and any other circuitry, which will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. Only one driven input should be connected to the ADC output pins.

## APPLICATION SCHEMATICS

The following figures show simple examples of using the ADC10080. Figure 41 shows a typical differentially driven input. Figure 42 shows a single ended application circuit.

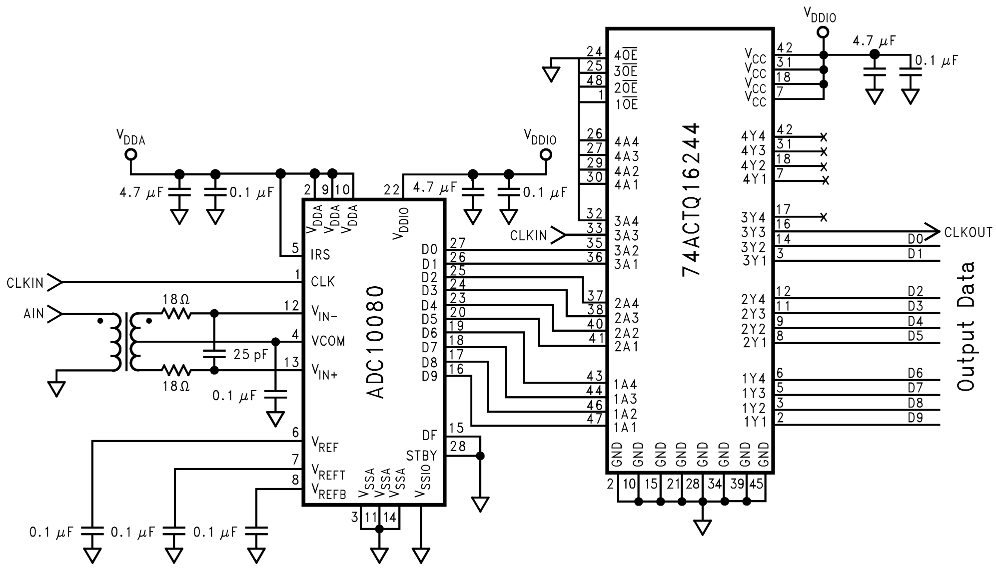



Figure 41. A Simple Application Using a Differential Driving Source

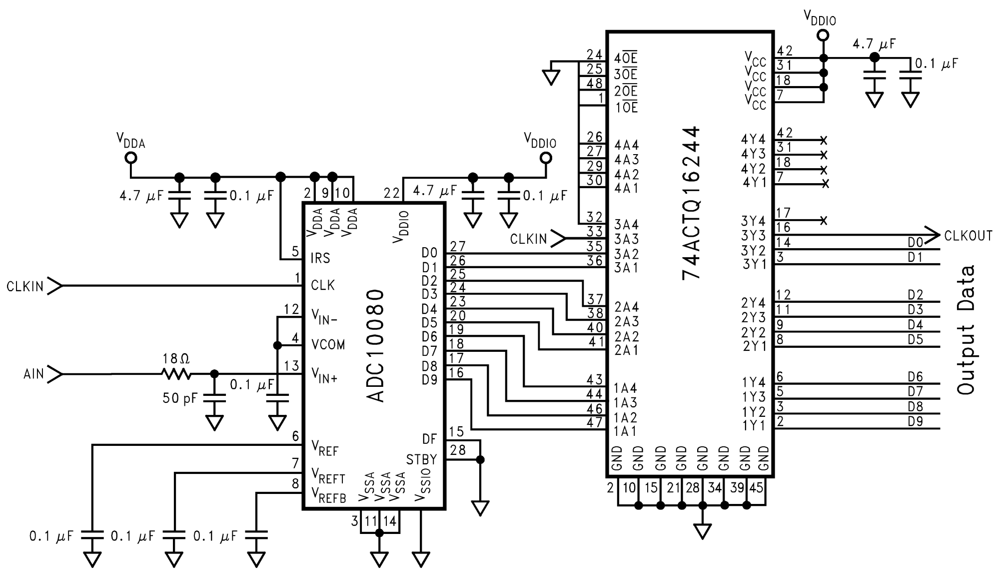



Figure 42. A Simple Application Using a Single Ended Driving Source

# REVISION HISTORY

| Changes from Revision G (March 2013) to Revision H | Page |
| --- | --- |
| • Changed layout of National Data Sheet to TI format | 19 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC10080CIMT/NOPB | ACTIVE | TSSOP | PW | 28 | 48 | Green (RoHS & no Sb/Br) | SN \| CU SN | Level-3-260C-168 HR | -40 to 85 | ADC10080 CIMT | Samples |
| ADC10080CIMTX/NOPB | ACTIVE | TSSOP | PW | 28 | 2500 | Green (RoHS & no Sb/Br) | SN \| CU SN | Level-3-260C-168 HR | -40 to 85 | ADC10080 CIMT | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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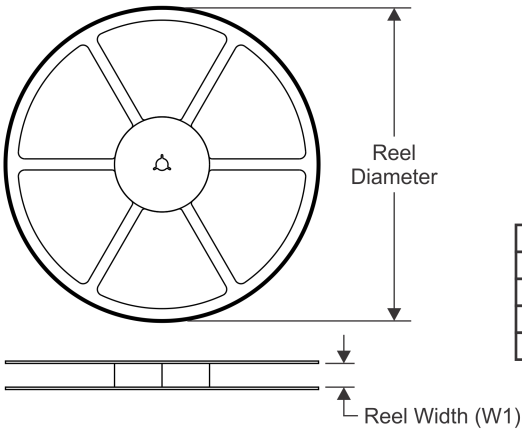
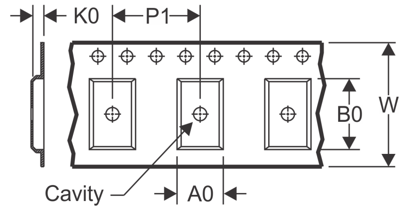
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

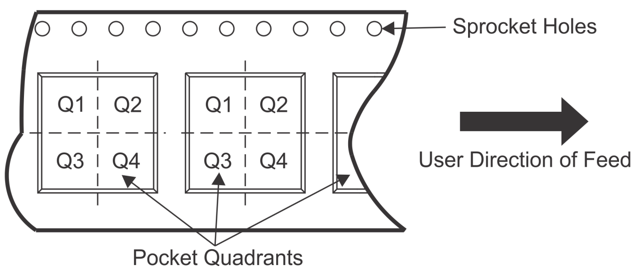



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

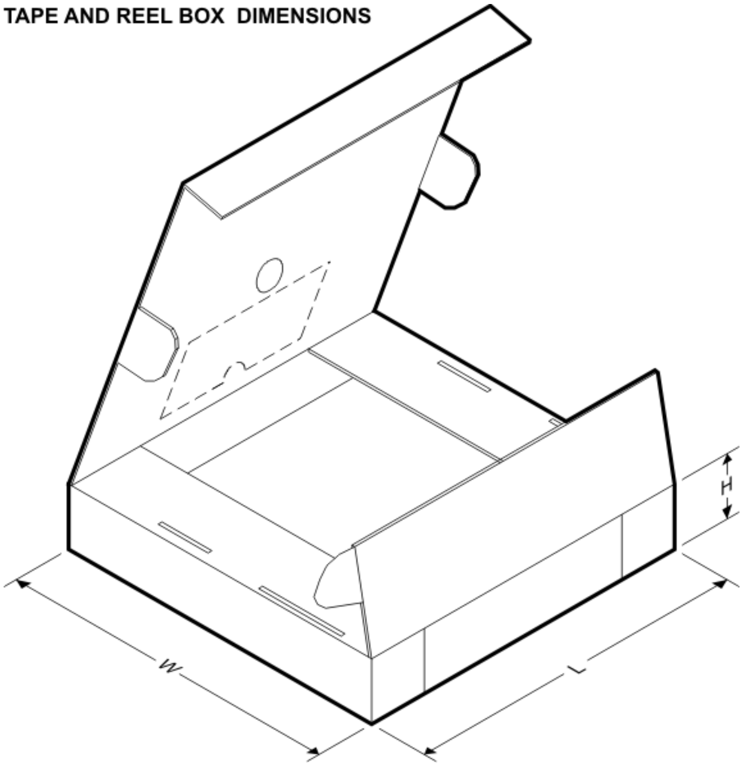
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC10080CIMTX/NOPB | TSSOP | PW | 28 | 2500 | 330.0 | 16.4 | 6.8 | 10.2 | 1.6 | 8.0 | 16.0 | Q1 |

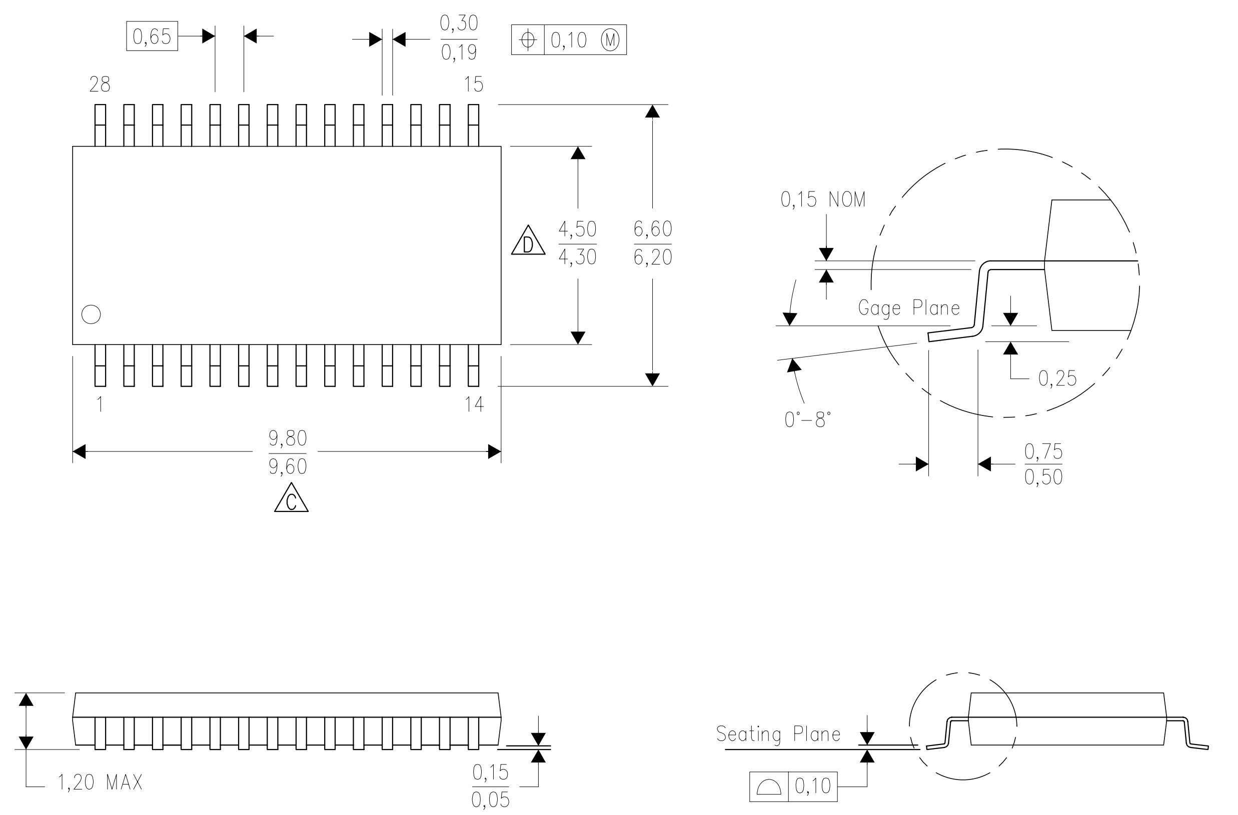
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADC10080CIMTX/NOPB | TSSOP | PW | 28 | 2500 | 367.0 | 367.0 | 38.0 |

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE

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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

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401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
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Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

### ➢ Customer Service :

Email service@ameya360.com

### ➢ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com