TPS6305x Single Inductor Buck-Boost with 1A Switches and Adjustable Soft Start

1 Features

- Real Buck or Boost with Seamless Transition Between Buck and Boost Mode
- 2.5V to 5.5V Input Voltage Range
- 0.5A Continuous Output Current : V_{IN}≥2.5V, V_{OUT}=3.3V
- Adjustable and Fixed Output Voltage Version
- Efficiency >90% in Boost Mode and >95% in Buck Mode
- 2.5MHz Typical Switching Frequency
- Adjustable Average Input Current Limit
- Adjustable Soft Start Time
- Device Quiescent Current Less Than 50µA
- Power Save Mode
- Load Disconnect During Shutdown
- Over-Temperature Protection
- Small 1.6mm x 1.2mm, 12-pin WCSP package

2 Applications

- Cellular Phones, Smart Phones
- Tablets PC
- PC and Smart Phone accessories
- Battery Powered Applications

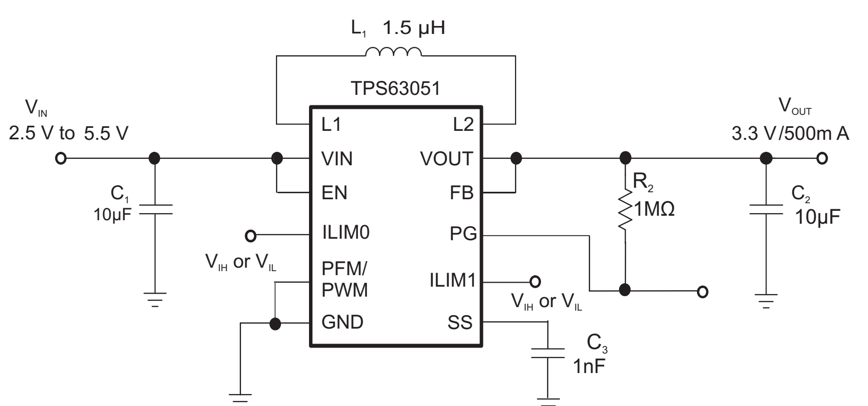
3 Description

The TPS63050/1 are high efficiency, low quiescent current buck-boost converters suitable for applications where the input voltage is higher or lower than the output. Output currents can go as high as 500mA in boost mode and as high as 1A in buck mode. The maximum average current in the switches is limited to a typical value of 1A. The TPS6305x regulates the output voltage over the complete input voltage range by automatically switching between buck or boost mode depending on the input voltage ensuring seamless transition between modes. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain highest efficiency. At low load currents, the converter enters Power Save Mode to maintain high efficiency over the complete load current range. There is a PFM/PWM pin that allows the user to choose between automatic PFM/PWM mode operation and forced PWM operation. During PWM mode a fixed-frequency of typically 2.5MHz is used. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. (The device is packaged in a 12-pin WCSP package measuring 1.6mm × 1.2mm).

Device Information

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
TPS63050YFF	DSBGA (12)	1,56mm x 1,16mm
TPS63051YFF		

4 Simplified Schematic



ILIM0	ILIM1	Current LIMIT set for
Low	Low	0.4*IIN_MAX
High	Low	0.5*IIN_MAX
Low	High	0.65*IIN_MAX
High	High	IIN_MAX

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2013) to Revision A **Page**

- Changed data sheet format to new schema. 1
- Added TPS63050 device specifications and description throughout data sheet.. 1
- Updated Figure 37 - PCB Layout Suggestion 26

Table 1. Ordering Information

T_A	VOUT	PART NUMBER	PACKAGE	ORDERING	PACKAGE MARKING
–40°C to 85°C	Adjustable	TPS63050	WCSP	TPS63050YFF	63050
	3.3 V	TPS63051	WCSP	TPS63051YFF	63051

6 Terminal Configuration and Functions

YFF (12)
(TOP VIEW)

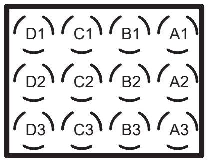


Table 2. Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ILIM0	B2	I	Programmable inrush current limit input works together with I_{LIM1}. See table on page 1. It must not be left floating
SS	D3	I	Adjustable Soft-Start. If connected to ground default soft-start time is set
PG	C3	O	Power good open drain output
FB	D2	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
EN	A3	I	Enable input. (1 enabled, 0 disabled). It must not be left floating
VOUT	D1	O	Buck-boost converter output
VIN	A2	I	Supply voltage for power stage and control stage
L1	A1		Connection for Inductor
GND	B1		Ground for Power stage and Control stage
ILIM1	B3	I	Programmable inrush current limit input works together with I_{LIM0}. See table on page 1. It must not be left floating
PFM/PWM	C2	I	0 for PFM mode 1 for forced PWM mode. It must not be left floating
L2	C1		Connection for Inductor

6.1 Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

		VALUE		
		MIN	MAX	UNIT
Voltage range[(2)]	VIN, L1, L2[(3)], VOUT, EN, FB, PG, ILIM0, ILIM1[(1)]	–0.3	7	V
	SS		3	V
Operating junction temperature range, T_J [(3)]		–40	150	°C
Operating ambient temperature range, T_A		–40	85	°C

(1) DC-voltage Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are DC-voltages with respect to ground terminal.
(3) L2,L1 voltage can exceed ABSMAX ratings during normal operation. As long as the device is operated within recommend operating conditions device reliability is not affected.

6.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
ESD	Human Body Model (HBM) [(1)]		2	kV
	Charged Device Model (CDM)[(1)]		700	V

(1) ESD testing is performed according to the respective JESD22 JEDEC standard.

6.3 THERMAL INFORMATION

THERMAL METRIC[(1)]		TPS6305x	UNITS
		12 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	89.9	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance	0.7	
θ_{JB}	Junction-to-board thermal resistance	43.9	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	43.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
VIN	Input Voltage Range VIN	2.5		5.5	V
L	Inductor Value	1	1.5	2.2	µH
C_{out}	Output Capacitor value[(1)]	10		120	µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating virtual junction temperature	–40		125	°C

(1) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the minimal capacitor required with the dc bias effect for this type of cap. The nominal value given matches a typical capacitor to be chosen to meet the minimum capacitance required.

6.5 Electrical Characteristics

V_{IN}=3.6V, T_A=-40°C to 85°C, typical values are at T_A=25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply							
V_{IN}	Input voltage range			2.5		5.5	V
V_{IN_Min}	Minimum input voltage to turn on in full load		I_{OUT}=500mA		2.7		V
I_{OUT}	Output Current (1)				500		mA
I_Q	Quiescent current	V_{IN}	I_{OUT}=0mA, EN=V_{IN}=3.6V, V_{OUT}=3.3V		43	60	µA
		V_{OUT}				10	µA
I_{sd}	Shutdown current		EN=0V		0.1	1	µA
UVLO	Under voltage lockout threshold		V_{IN} falling	1.6	1.7	1.8	V
	Under voltage lockout hysteresis				200		mV
T_{SD}	Thermal shutdown		Temperature rising		140		°C
	Thermal Shutdown hysteresis				20		°C
Logic Signals EN, I_{LIM0}, I_{LIM1}							
V_{IH}	High Level Input voltage		V_{IN}=2.5V to 5.5V	1.2			V
V_{IL}	Low level voltage Input Voltage		V_{IN}=2.5V to 5.5V			0.3	V
I_{lkg}	Input Leakage current		EN, I_{LIM0}, I_{LIM1}=GND or V_{IN}		0.01	0.1	µA
Power Good							
V_{OL}	Low level voltage		I_{sink}=100µA			0.3	V
I_{PG}	PG sinking current		V=0.3V			0.1	mA
I_{lkg}	Input Leakage current		V_{PG}=3.6V		0.01	0.1	µA
Output							
V_{OUT}	Output Voltage range			2.5		5.5	V
V_{FB}	TPS63050 Feedback regulation voltage				0.8		V
V_{FB}	TPS63050 Feedback voltage accuracy (2)		PWM mode	-1.1%		1.1%	
V_{FB}	TPS63050 Feedback voltage accuracy (2)		PFM mode	-1%		+3%	
V_{OUT}	TPS63051 Output voltage accuracy (2)		PWM mode	3.27	3.3	3.34	V
V_{OUT}	TPS63051 Output voltage accuracy (2)		PFM mode	3.27	3.3	3.39	V
$I_{PWM\text{->}PFM}$	Minimum output current to enter PFM mode		V_{IN} =3V; V_{OUT} = 3.3V		150		mA
I_{FB}	TPS63050 Feedback input bias current		V_{FB} = 0.8V		10	100	nA
$R_{DS(on)}$	Input High side FET on-resistance		I_{SW}=500mA I		145		mΩ
	Output High side FET on-resistance				95		mΩ
	Input Low side FET on-resistance				170		mΩ
	Output Low side FET on-resistance				115		mΩ
I_{IN_MAX}	Input current limit Boost Mode		I_{LIM0}=V_{IH}, I_{LIM1}= V_{IH},V_{IN}=2.7V to 3V, V_{OUT}=3V	480		1240	mA
I_{IN_MAX}	Input current limit Boost Mode		I_{LIM0}=V_{IH}, I_{LIM1}= V_{IH},V_{IN}=2.7V to 3.3V, V_{OUT}=3.3V,	550		1400	mA
I_{IN_MAX}	Input current limit Boost Mode		I_{LIM0}=V_{IH}, I_{LIM1}= V_{IH},V_{IN}=2.7V to 4.5V, V_{OUT}=4.5V,	630		1950	mA
I_{SS_IN}	Programmable inrush current limit (3)		I_{LIM0}=V_{IL}, I_{LIM1}= V_{IL}, V_{IN}=3.0V,V_{OUT}=3.3V		0.4*I_{IN_MAX}		mA
			I_{LIM0}=V_{IL}, I_{LIM1}= V_{IH}, V_{IN}=3.0V,V_{OUT}=3.3V		0.5*I_{IN_MAX}		mA
			I_{LIM0}=V_{IH}, I_{LIM1}= V_{IL}, V_{IN}=3.0V,V_{OUT}=3.3V		0.65*I_{IN_MAX}		mA
			I_{LIM0}=V_{IH}, I_{LIM1}= V_{IH}, V_{IN}=3.0V,V_{OUT}=3.3V		I_{IN_MAX}		mA

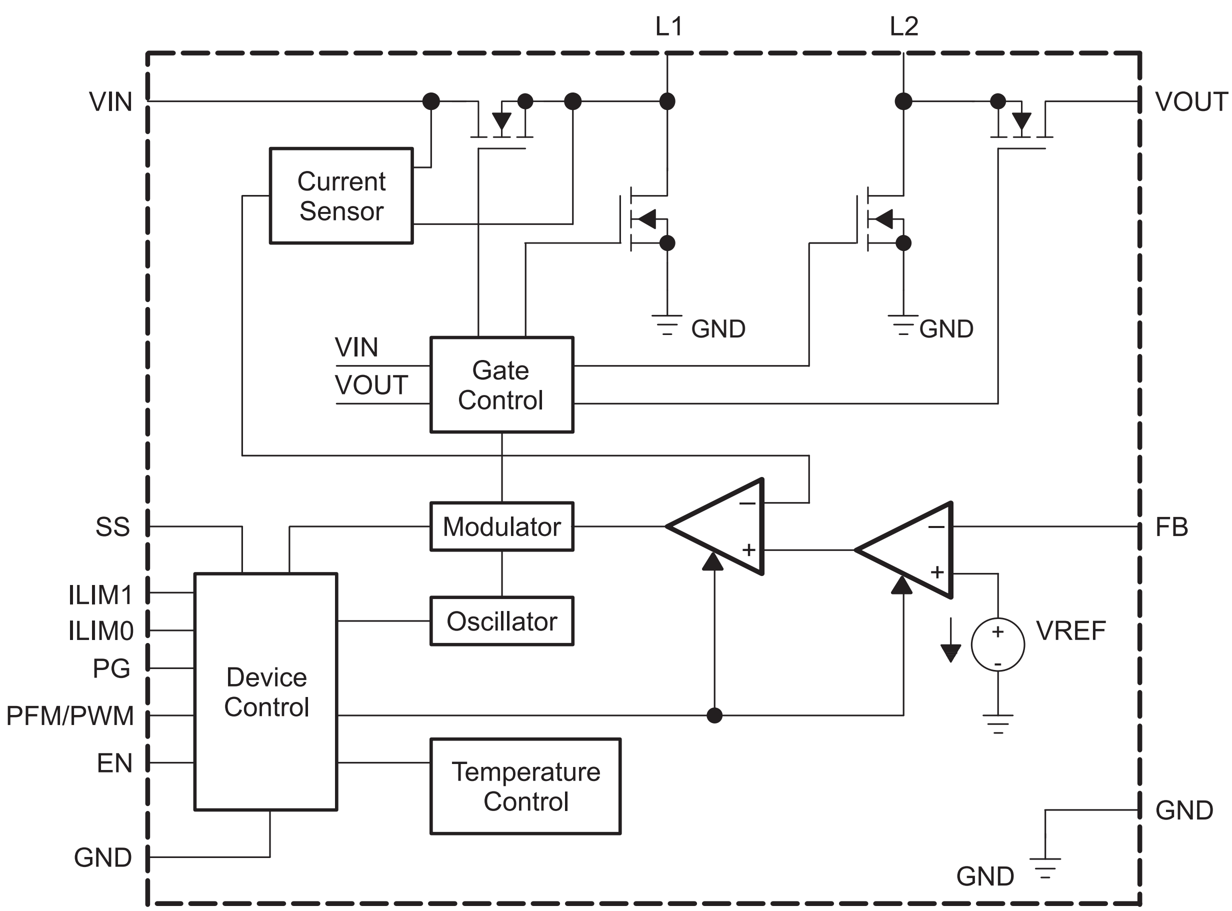
(1) For minimum and maximum output current in a specific working point see Figure 1 and Figure 2; and Equation 1 through Equation 4.
(2) Conditions: f=2.5MHz, L=1.5uH, C_{OUT}=10uF
(3) For variation of this parameter with Input voltage see Figure 5.

Electrical Characteristics (continued)

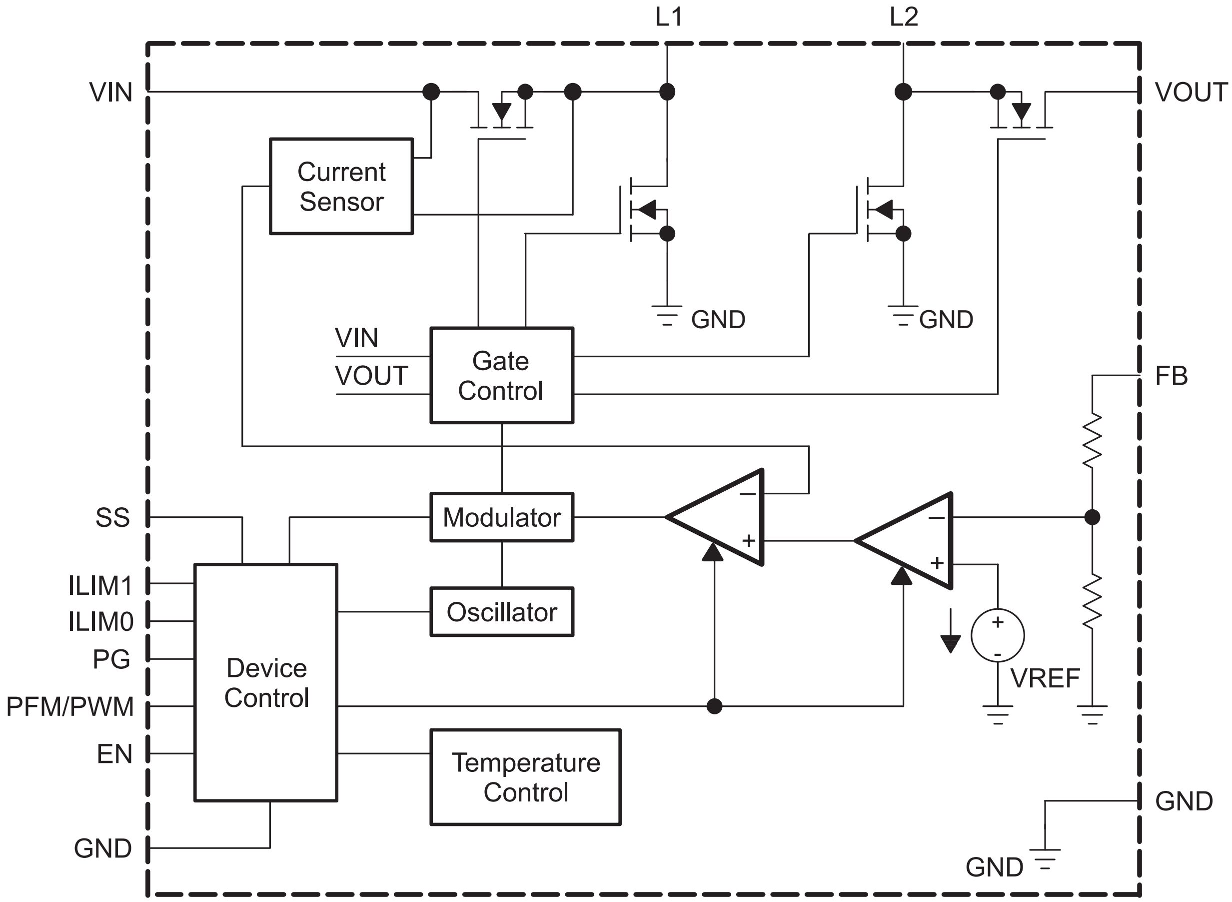
V_{IN}=3.6V, T_A=-40°C to 85°C, typical values are at T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_s	Switching Frequency			2.5		MHz
I_{SS}	Softstart Current TPS63051			1		µA
I_{SS}	Softstart Current TPs63050			3.2		µA
t_{delay}	Start up delay	Time from when EN=high to when device starts switching		100		µs
t_{SS}	Soft-start time	V_{OUT}=EN=low to high, SS=floating, Buck mode Vin=3.6V, Vout=3.3V, Iout=500mA(3)		280		µs
		V_{OUT}=EN=low to high, SS=floating, Boost mode Vin=2.5V, Vout=3.3V, Iout=500mA(3)		600		µs
t_{delay}	Start up delay	Time from when EN=high to when device starts switching		85		µs
	Line regulation	V_{IN}=2.5V to 5.5V, I_{OUT}=500mA, PWM mode		0.963		mV/V
	Load regulation	V_{IN}=3.6V, I_{OUT}=0mA to 500mA, PWM mode		4		mV/A

Functional Block Diagram (TPS63050)



Functional Block Diagram (TPS63051)



7 Typical Characteristics

Table 3. Table of Graphs

DESCRIPTION		FIGURE
Maximum average input current	vs Input voltage (TPS63051, V_{OUT} = 3.3V, T_A={-40°C, 25°C, 85°C})	1
Minimum average input current	vs Input voltage (TPS63051, V_{OUT} = 3.3V, T_A={-40°C, 25°C, 85°C})	2
Average input current limit	vs Input voltage (TPS63050, V_{OUT} = 3V, T_A={-40°C, 25°C, 85°C})	3
	vs Input voltage (TPS63050, V_{OUT} = 4.5V, T_A={-40°C, 25°C, 85°C})	4
Programmable inrush input current limit	vs Input voltage (TPS63051, I_{LIM0}=V_{IL}, I_{LIM1}= V_{IL}; I_{LIM0}=V_{IL}, I_{LIM1}= V_{IH}; I_{LIM0}=V_{IH}, I_{LIM1}= V_{IL}; V_{OUT} = 3.3V)	5
Soft Start Time	vs Input voltage (TPS63051, C_{SS}= Open, I_{OUT}={100µA, 300mA, 500mA})	6
	vs Input voltage (TPS63051, C_{SS}= 1nF I_{OUT}={100µA, 300mA, 500mA})	7
	vs Input voltage (TPS63051, C_{SS}= 1.8nF I_{OUT}={100µA, 300mA, 500mA})	8
	vs Input voltage (TPS63051, C_{SS}= 2.2nF I_{OUT}={100µA, 300mA, 500mA})	9
	vs Input voltage (TPS63051, C_{SS}= 3.3nF I_{OUT}={100µA, 300mA, 500mA})	10
Efficiency	vs Output current (TPS63051, Power Save Enabled, V_{OUT} = 3.3V)	11
	vs Output current (TPS63051, Power Save Disabled, V_{OUT} = 3.3V)	12
	vs Output current (TPS63050, Power Save Enabled, V_{OUT} = 2.5V, V_{OUT} = 4.5V)	13
	vs Output current (TPS63050, Power Save Disabled, V_{OUT} = 2.5V, V_{OUT} = 4.5V)	14
	vs Input voltage (TPS63051, Power Save Enabled, V_{OUT} = 3.3V, I_{OUT} = {10; 500; 620mA})	15
	vs Input voltage (TPS63051, Power Save Disabled, V_{OUT} = 3.3V, I_{OUT} = {10; 500; 620mA})	16
	vs Input voltage (TPS63050, Power Save Enabled, V_{OUT} = 2.5V, I_{OUT} = {10; 500; 620mA})	17
	vs Input voltage (TPS63051, Power Save Disabled, V_{OUT} = 2.5V, I_{OUT} = {10; 500; 620mA})	18
	vs Input voltage (TPS63050, Power Save Enabled V_{OUT} = 4.5V, I_{OUT} = {10; 500; 620mA})	19
	vs Input voltage (TPS63050, Power Save Disabled, V_{OUT} = 4.5V, I_{OUT} = {10; 500; 620mA})	20
Output voltage	vs Output current (TPS63050, V_{OUT} = 2.5V)	21
	vs Output current (TPS63051, V_{OUT} = 3.3V)	22
	vs Output current (TPS63050, V_{OUT} = 4.5V)	23
Waveforms	Output Voltage ripple in Buck-Boost mode and PFM to PWM transition (TPS63051, V_{IN} =3.3V, I_{OUT}=145mA)	24
	Output Voltage ripple in Boost mode and PFM (TPS63051, V_{IN} =2.8V, I_{OUT}=16mA)	25
	Output Voltage ripple in Buck mode and PFM (TPS63051, V_{IN} =4.2V, I_{OUT}=16mA)	26
	Switching waveform in Boost mode and PWM (TPS63051, V_{IN} =2.5V, I_{OUT}=300mA)	27
	Switching waveform in Buck mode and PWM (TPS63051, V_{IN} =4.5V, I_{OUT}=300mA)	28
	Switching waveform in Buck-Boost mode and PWM (TPS63051,V_{IN} =3.4V, I_{OUT}=300mA)	29
	Load transient response (TPS63051, V_{IN} =2.8V, Load change from 0mA to 300mA)	30
	Load transient response (TPS63051, V_{IN}=3.6V, Load change from 0mA to 300mA)	31
	Line transient response (TPS63051, V_{OUT} = 3.3V, I_{OUT} = 500 mA)	32
	Startup after enable (TPS63051, V_{OUT} = 3.3V, V_{IN} = 2.5V, I_{OUT} = 0mA)	33
	Startup after enable (TPS63051, V_{OUT} = 3.3V, V_{IN} = 4.2V, I_{OUT} = 0mA)	34

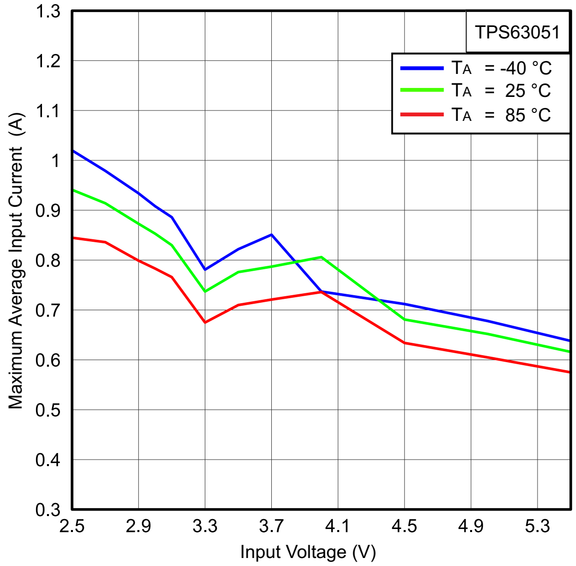


Figure 1. Maximum Average Input Current vs Input Voltage

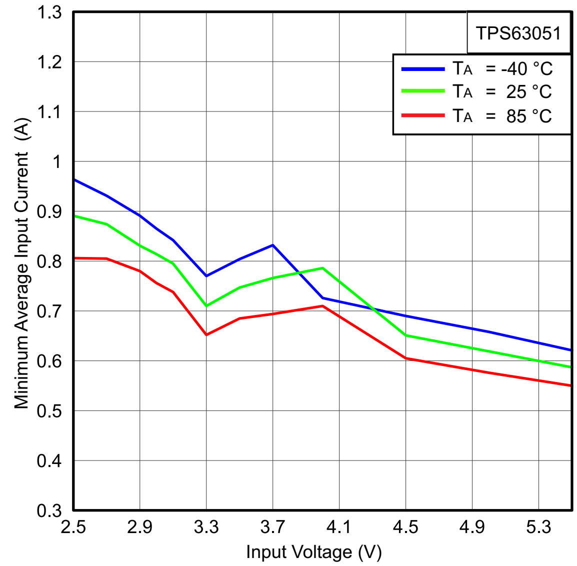


Figure 2. Minimum Average Input Current vs Input Voltage

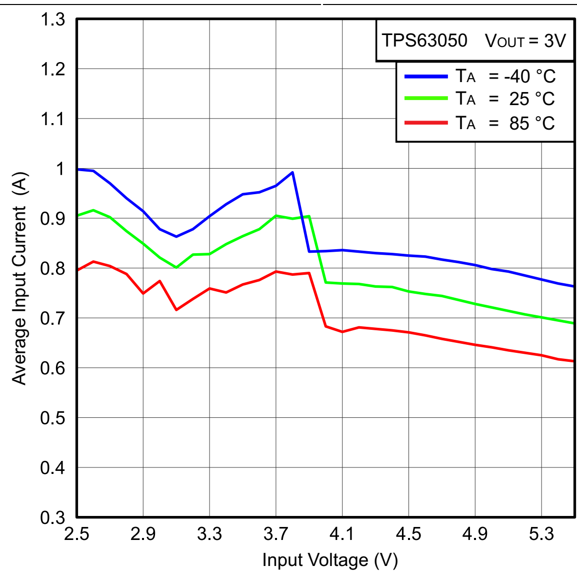


Figure 3. Average Input Current vs Input Voltage

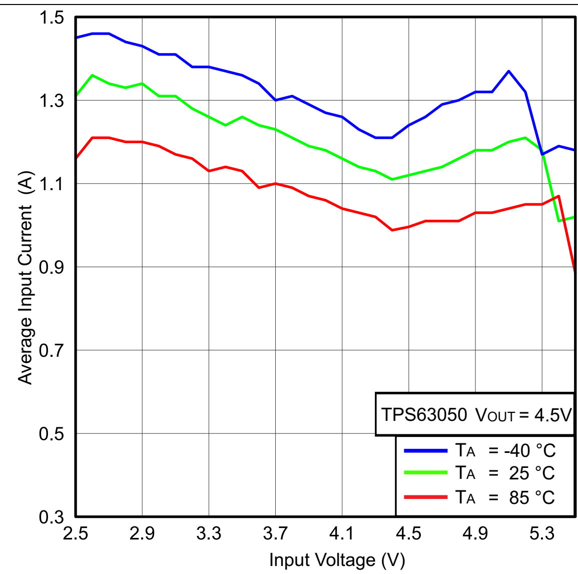


Figure 4. Average Input Current vs Input Voltage

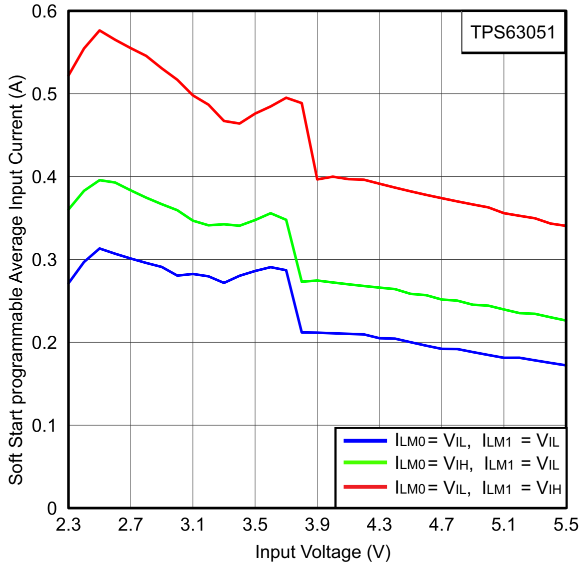


Figure 5. Programmable Inrush Input Current Limit vs Input Voltage

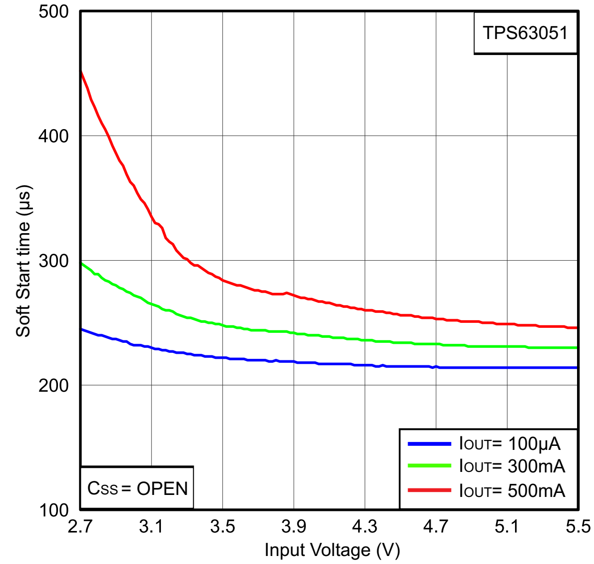


Figure 6. Soft Start Time vs Input Voltage

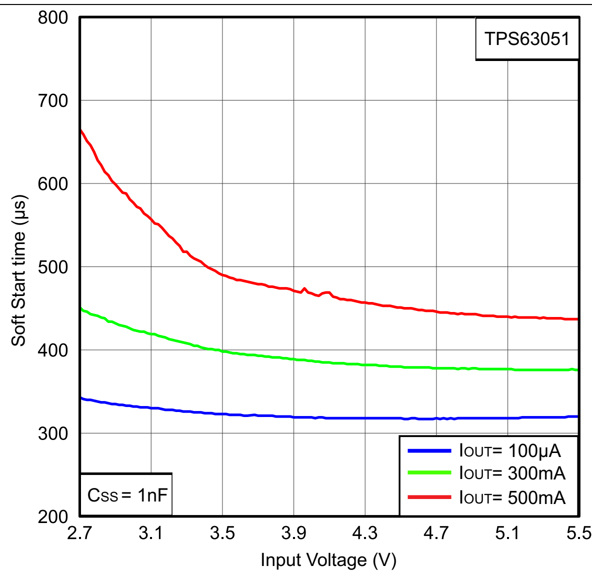


Figure 7. Soft Start Time vs Input Voltage

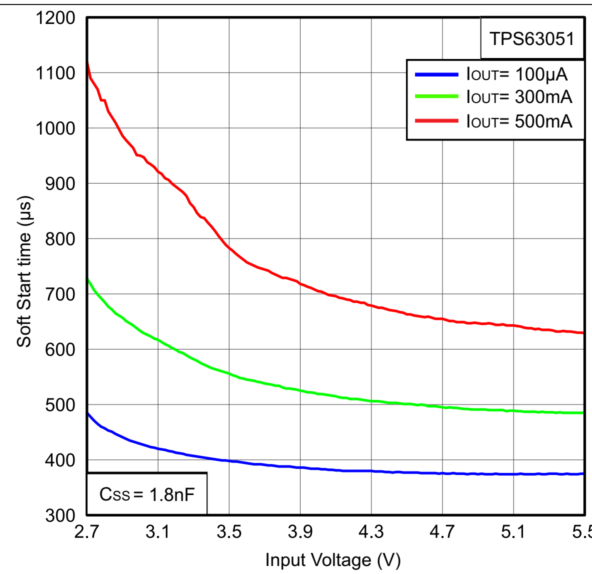


Figure 8. Soft Start Time vs Input Voltage

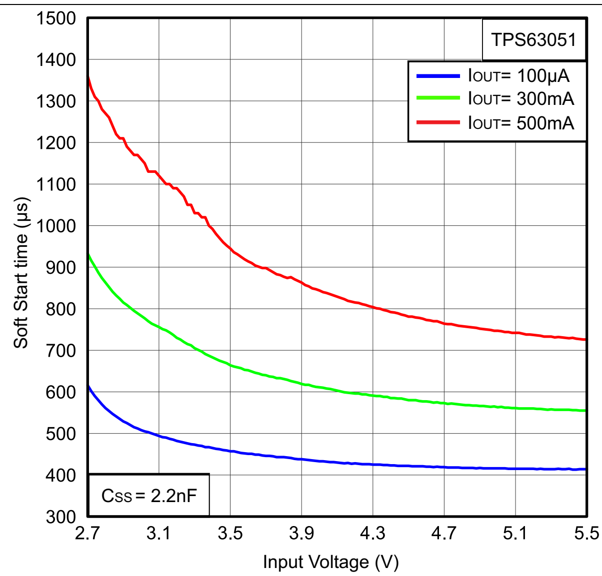


Figure 9. Soft Start Time vs Input Voltage

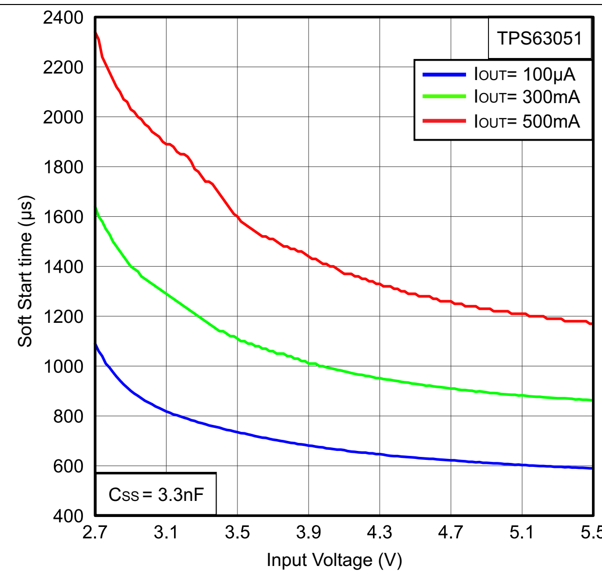


Figure 10. Soft Start Time vs Input Voltage

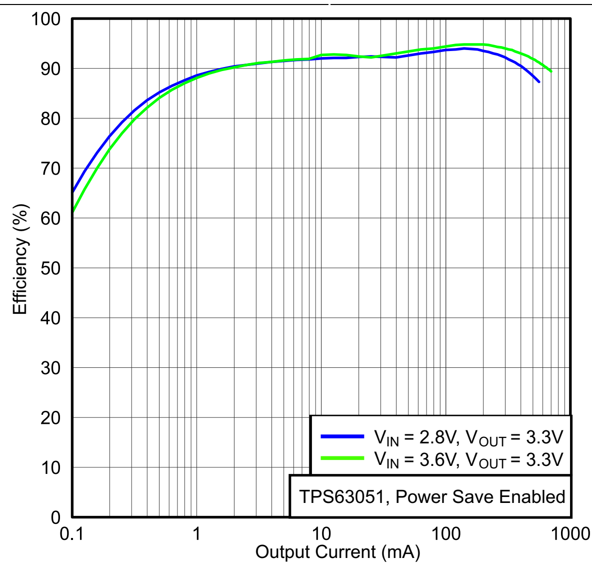


Figure 11. Efficiency vs Output Current

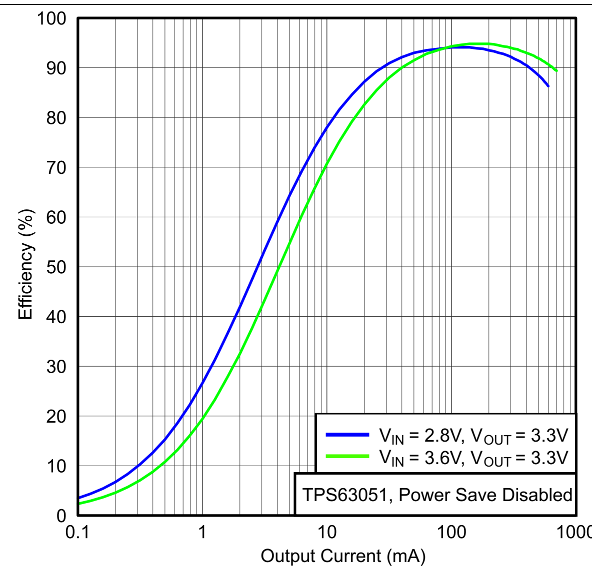


Figure 12. Efficiency vs Output Current

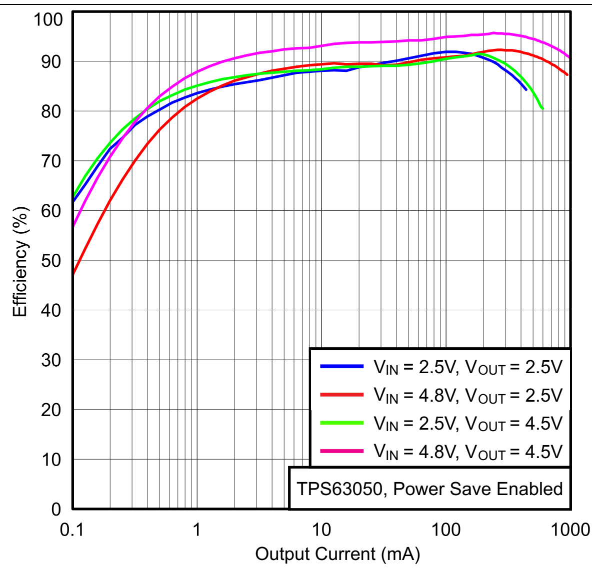


Figure 13. Efficiency vs Output Current

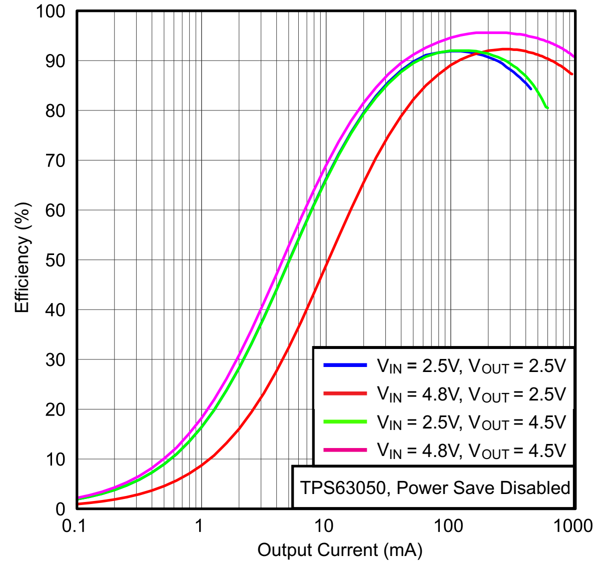


Figure 14. Efficiency vs Output Current

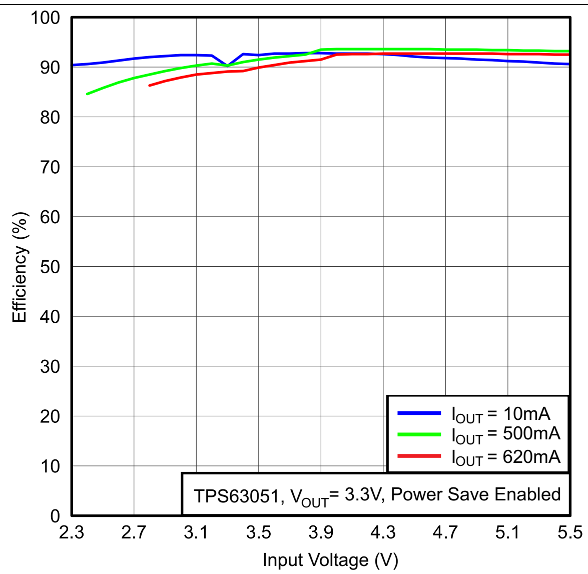


Figure 15. Efficiency vs Input Voltage

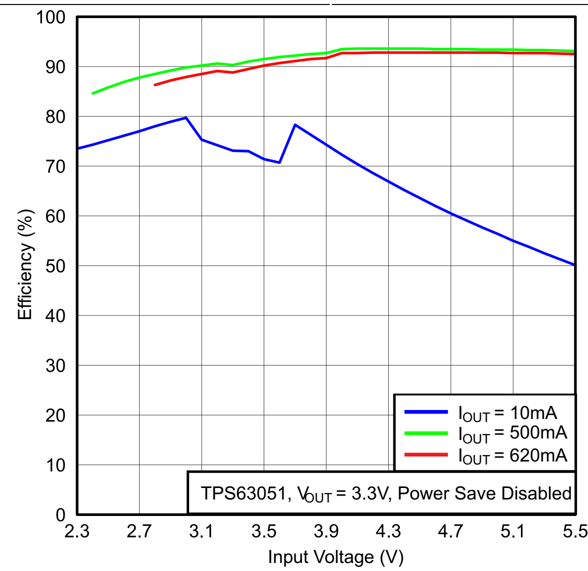


Figure 16. Efficiency vs Input Voltage

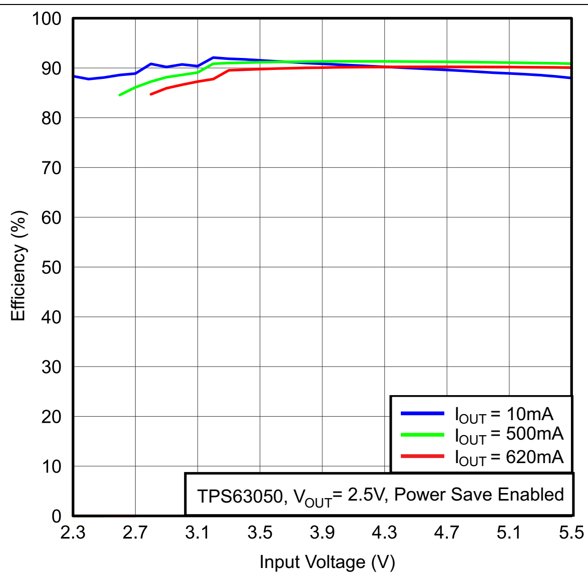


Figure 17. Efficiency vs Input Voltage

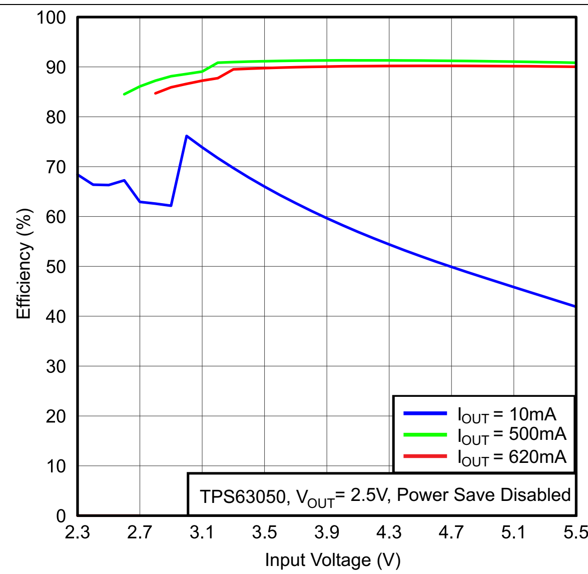


Figure 18. Efficiency vs Input Voltage

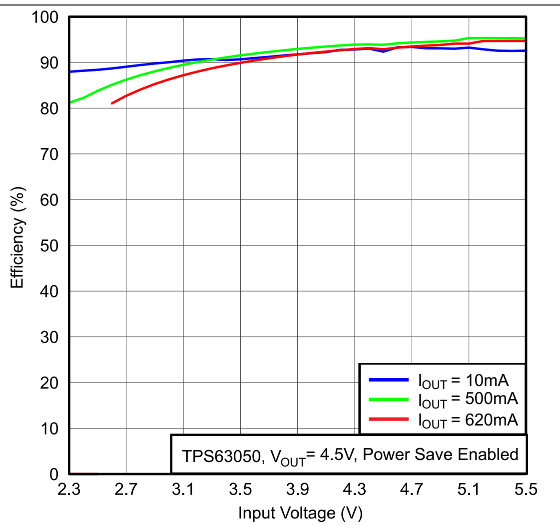


Figure 19. Efficiency vs Input Voltage

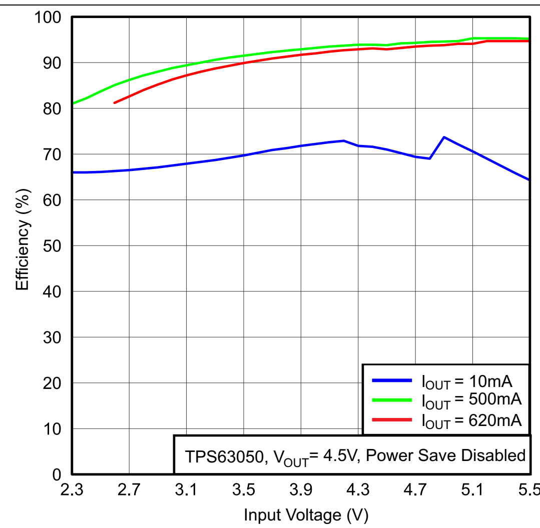


Figure 20. Efficiency vs Input Voltage

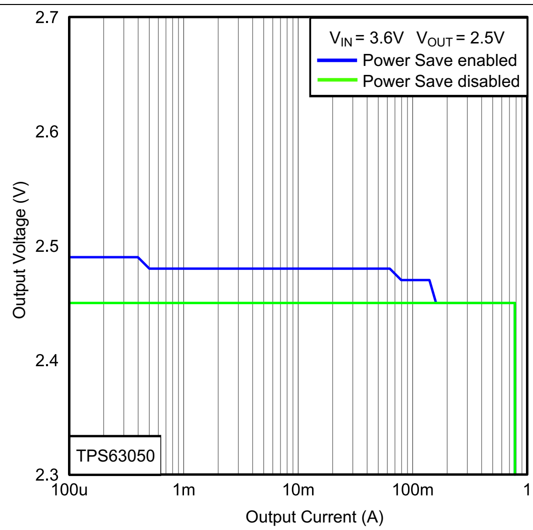


Figure 21. Output Voltage vs Output Current

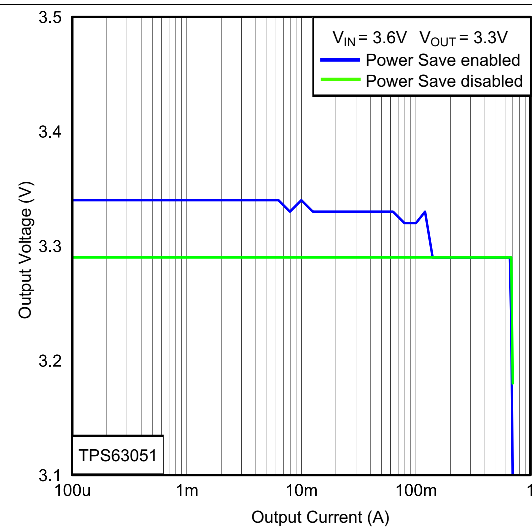


Figure 22. Output Voltage vs Output Current

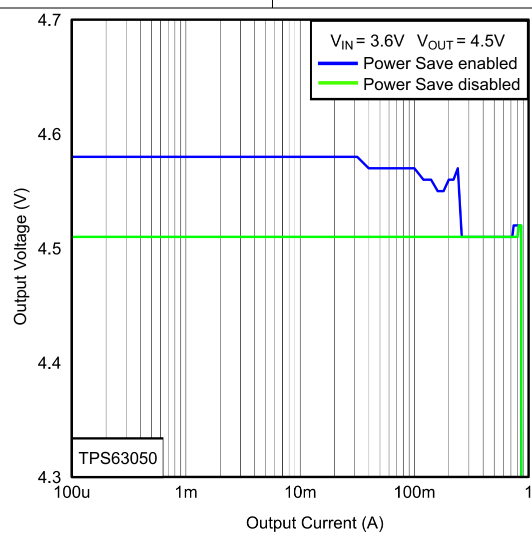


Figure 23. Output Voltage vs Output Current

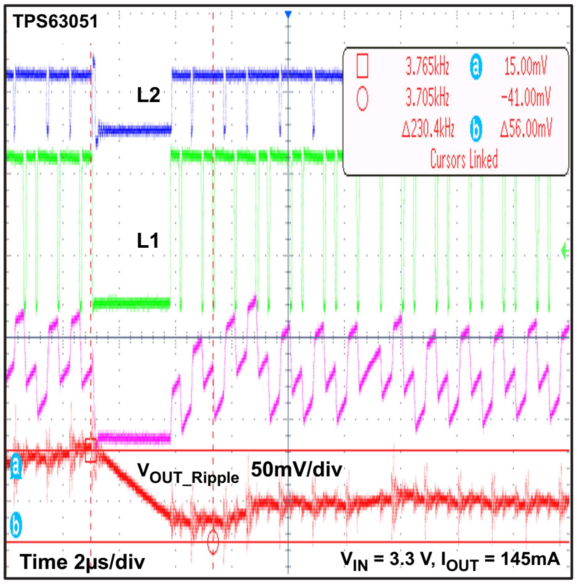


Figure 24. Output Voltage Ripple in Buck-Boost Mode and PFM To PWM Transition

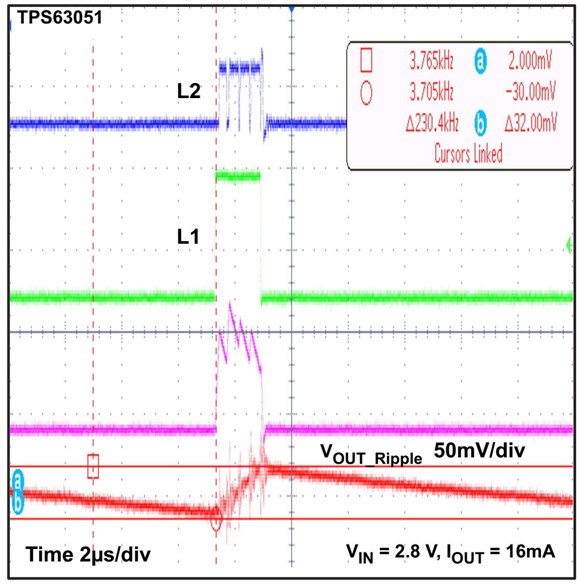


Figure 25. Output Voltage Ripple in Boost Mode and PFM

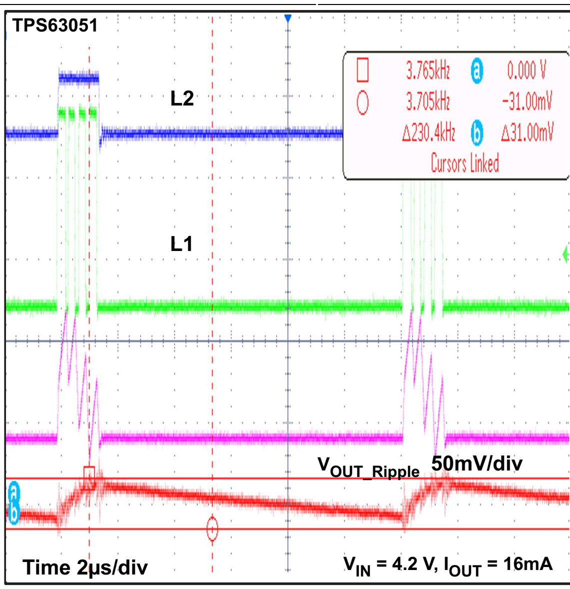


Figure 26. Output Voltage Ripple in Buck Mode and PFM

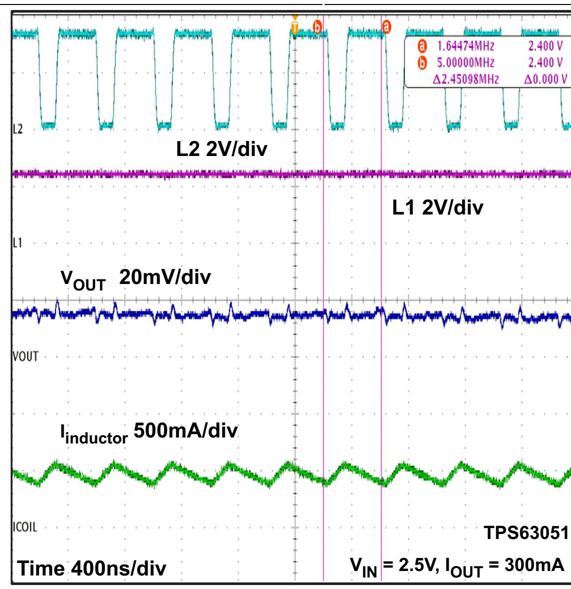


Figure 27. Switching Waveforms Boost Mode and PWM

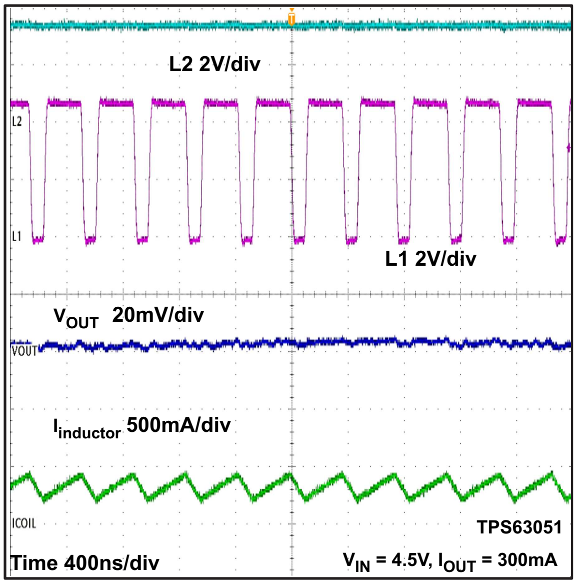


Figure 28. Switching Waveforms Buck Mode and PWM

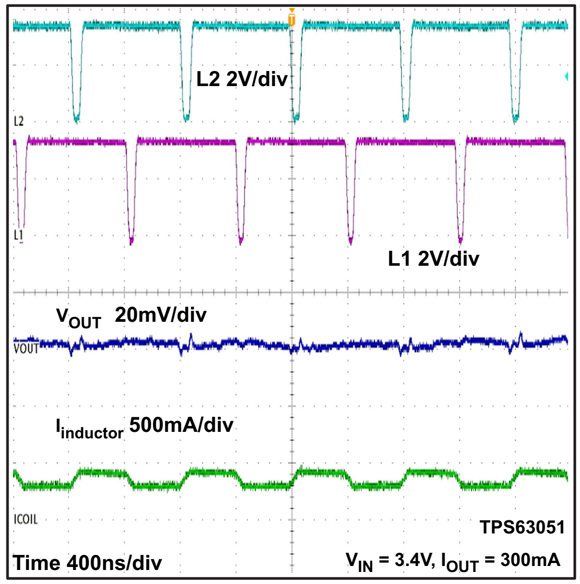


Figure 29. Switching Waveforms Buck-Boost Mode and PWM

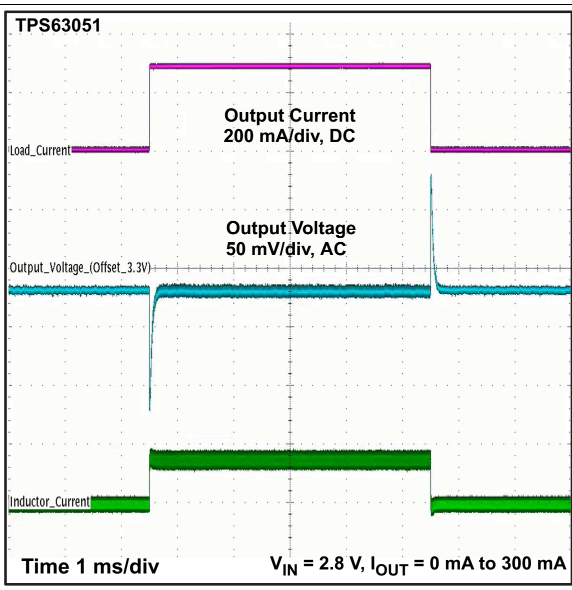


Figure 30. Load Transient Response PWM Mode

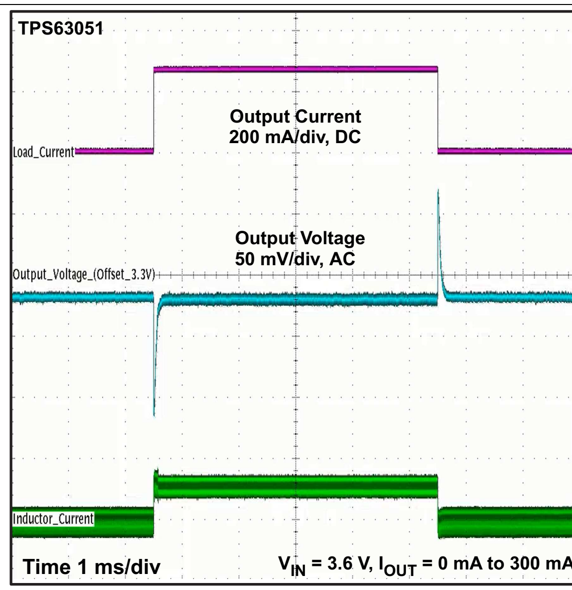


Figure 31. Load Transient Response PWM Mode

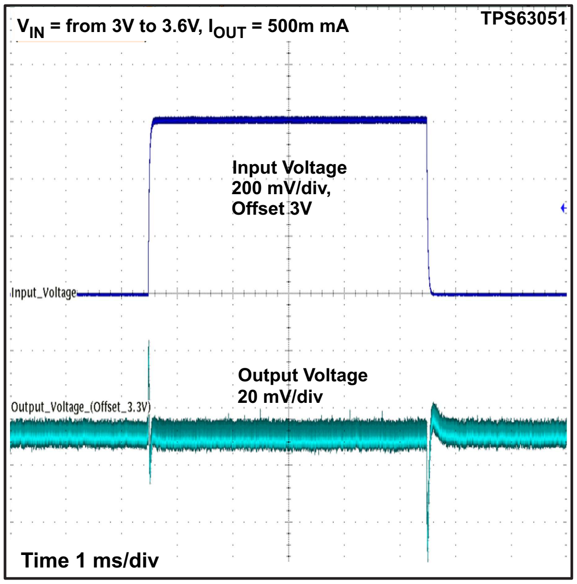


Figure 32. Line Transient Response PWM Mode

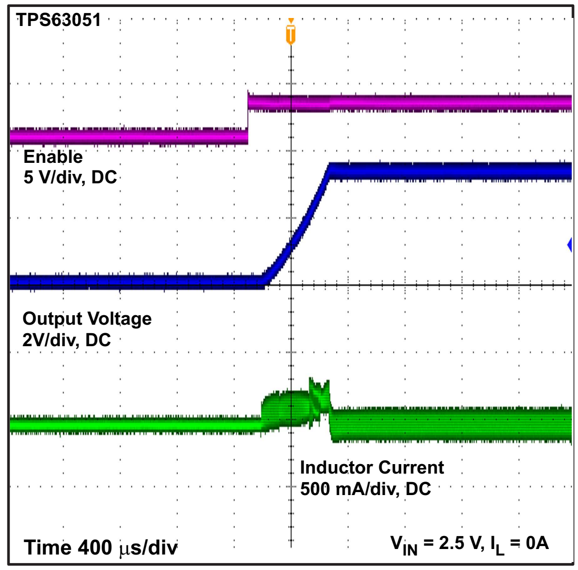


Figure 33. Start Up After Enable

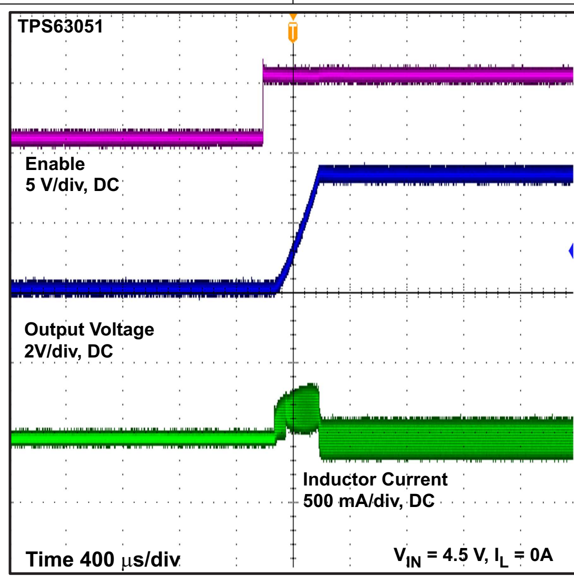


Figure 34. Start Up After Enable

8 Parameter Measurement Information

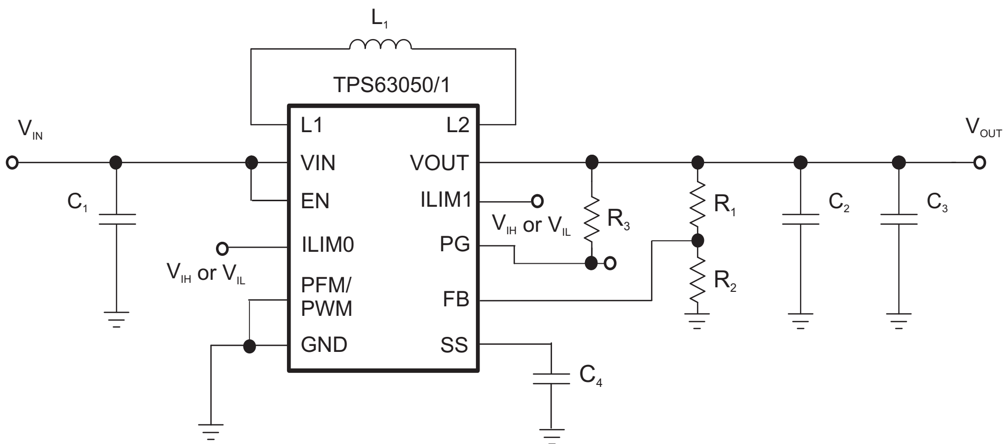


Figure 35. Parameter Measurement Circuit

Table 4. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63050/1	Texas Instruments
L1	1.5µH, 2.1A/108mΩ	1269AS-H-1R5M, TOKO
C1,C2,C3	10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C4	C_{SS} (See Figure 6 through Figure 10)	
R1	Depending on the output voltage of TPS63050, 0 Ω with TPS63051	
R2	Depending on the output voltage of TPS63050, not used withTPS63051	
R3	1 MΩ	

9 Detailed Description

9.1 Buck-Boost Operation

The TPS63050/1 use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over its complete input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch is held on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching at the same time. Keeping one switch on and one switch off eliminates their switching losses. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to keep always higher efficiency.

The device provides a seamless transition from buck to boost or from boost to buck operation.

9.2 Control Loop Description

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. shows the control loop.

The non inverting input of the transconductance amplifier gmv can be assumed to be constant. The output of gmv defines the average inductor current. The inductor current is reconstructed measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the on time of the same MOSFET. During the off time the current is reconstructed internally starting from the peak value reached at the end of the on time cycle. The average current is then compared to the desired value and the difference, or current error, is amplified and compared to the sawtooth ramp of either the Buck or the Boost. Depending on which of the two ramps is crossed by the signal either the Buck MOSFETs or the Boost MOSFETs will be activated. When the input voltage is close to the output voltage one buck cycle is always followed by a boost cycle. In this condition not more than three cycle in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

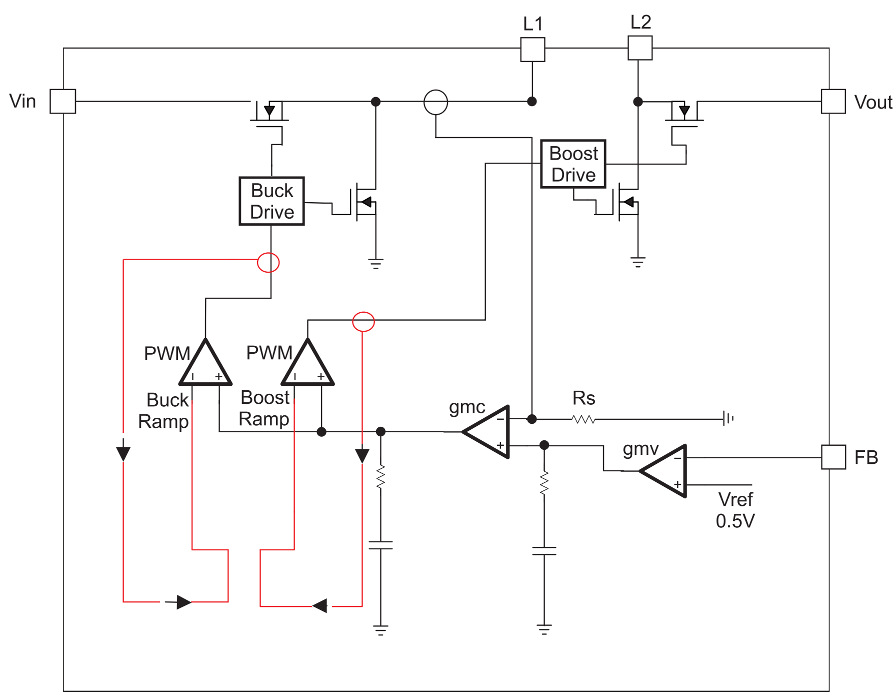


Figure 36. Average Current Mode Control

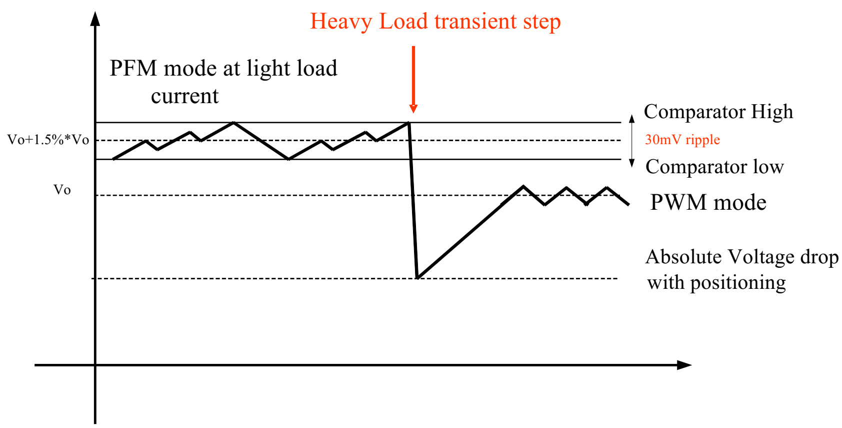
9.3 Power Save Mode Operation

Depending on the load current, in order to provide the best efficiency over the complete load range, the device works in PWM mode at load current of approximately 150mA or higher. At lighter load, the device switches automatically in to Power Save Mode to reduce power consumption and extend battery life. The PFM/PWM pin can be used to select between the two different operation modes. To enable Power Save Mode, the PFM/PWM pin must be set low.

During Power Save Mode, the part operates with a reduced switching frequency and supply current to maintain high efficiency. The output voltage is monitored with a comparator by the threshold comp low and comp high at every clock cycle. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. When the output voltage reaches the comp low threshold, at the next clock cycle the device ramps up the output voltage again, by starting operation. Operation can last for one or several pulses until the comp high threshold is reached. At the next clock cycle, if the load is still lower than about 150mA, the device switches off again and the same operation is repeated. Instead, if at the next clock cycle, the load is above 150mA, the device automatically switches to PWM mode.

In order to keep high efficiency in PFM mode, there is only a comparator active to keep the output voltage regulated. The AC ripple in this condition is increased, compared to the PWM mode. The amplitude of this voltage ripple in the worst case scenario is 50mV pk-pk, (typically 30mV pk-pk), with 10µF effective output capacitance. In order to avoid a critical voltage drop when switching from 0A to full load, the output voltage in PFM mode is typically 1.5% above the nominal value in PWM mode. The Dynamic Voltage Positioning allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transients.

Power Save Mode can be disabled by programming the PFM/PWM pin high.



Dynamic Voltage Positioning

9.4 Adjustable Current Limit

The TPS63050/1 has an internal user programmable current limit that monitors the input current during start-up. This prevents high inrush current protecting the device and the application. During start-up the input current does not exceed the current limit that is set by I_{LIM0} pin and I_{LIM1} pin. Depending on the logic level applied at these two pins, it is possible to switch between 4 different current limit levels. The variation of those values over input voltage and temperature is shown in Figure 1 through Figure 4.

It's possible to further adjust, at turn on, the ramp up time of the current and the output voltage using the Soft-Start capacitor.

The combination of I_{LIM0} and I_{LIM1} leads to the different current limit levels, as described in the current setting table shown here:

Adjustable Current Limit (continued)

ILIM0	ILIM1	Current LIMIT set
Low	Low	$0.4*I_{IN\_MAX}$
High	Low	$0.5*I_{IN\_MAX}$
Low	High	$0.65*I_{IN\_MAX}$
High	High	I_{IN_MAX}

The I_{LIM0}, I_{LIM1} pins may be changed during operation.

The current limit varies depending on the input voltage. The maximum value of average input current is obtained at the lowest input voltage.

Given the curves provided in Figure 1 through Figure 4 it is possible to calculate the output current in the different condition in boost mode using Equation 1 and Equation 2 and in buck mode using Equation 3 and Equation 4.

Duty Cycle Boost $$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

Output Current Boost $$I_{OUT} = \eta \times I_{IN}(1-D) \quad (2)$$

Duty Cycle Buck $$D = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Output Current Buck $$I_{OUT} = (\eta \times I_{IN}) / D \quad (4)$$

With,

η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
I_{IN}=Minimum average input current (Figure 2 to Figure 4)

9.5 Short Circuit Protection

The TPS63050/1 provides short circuit protection to protect itself and the application. When the output voltage does not increase above 1.2V, the device assumes a short circuit at the output and keeps the input current limit low to protect itself and the application. In short circuit, the input current limit is kept at 1.5A

9.6 Soft Start

To minimize inrush current during start up, the device implements soft start. At turn on, the input current is raised in a controlled manner until the output voltage reached regulation. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output.

The TPS63051 charges the soft start capacitor, at the SS pin, with a constant current of typically 1 µA. The input current follows the current used to charge the capacitor connected at the SS pin. The soft start operation is completed once the voltage at the SS pin has reached typically 1.3V. Figure 6 through Figure 10 list the value of the soft start capacitor needed to obtain a specific soft start time. The soft start time is defined as the time from when the EN pin is asserted to when the output voltage has reached 90% of it's nominal value. The time also depends on the load current; see the schematic described in Parameter Measurement Information section. If the amount of output capacitor is different, then the soft start time will be different from the one shown in the plots.

Soft Start (continued)

Thanks to its innovative soft start circuit the device ramps up the output voltage even if a large capacitor is connected at the output at the same time as the load current. This specific case is never confused with a short circuit condition. The inductance current is able to decrease and always ensure soft start unless a real short circuit is applied at the output terminals.

9.7 Device Enable

The device is put into operation when EN pin is set high. It is put into a shutdown mode when EN is set to low. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that during shutdown the output voltage can drop below the input voltage.

9.8 Power Good

The device has a built in power good function to indicate whether the output voltage operates above appropriate levels. By monitoring the status of the current control loop, the power good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react. The power good is operable as long as the converter is enabled and VIN is present.

The PG pin goes low in UVLO (as long as Vin is above typically 0.5V) and in thermal shutdown.

If the device is in current limit and the output voltage has not reached the regulated condition, the PG pin is held low. If the regulated condition is reached, PG is open drain.

When the PG pin is open drain, its logic function can be adjusted to any voltage level the connected logic is using, via a pull up resistor to the supply voltage of the logic. PG follows the voltage which it is connected to, which can be the output of the TPS63050/1 or another external voltage.

If EN is pulled low and one of the pins I_{LIM0} or I_{LIM1} is high, then the PG pin is low. If both pins, I_{LIM0} and I_{LIM1} are low, the PG is open drain. In this case the PG pin, follows its pull-up voltage. If this is not desired, one of the two pins I_{LIM0} or I_{LIM1}, must be set high. The PG pin table describes the PG pin functionality.

Power Good Settings

EN	ILIM1	ILIM0	PG
1	X	X	0 or Open Drain
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	Open Drain

9.9 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. In case it reaches the overvoltage threshold (typically 6.7V) the voltage amplifier regulates the output voltage to this value.

9.10 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VIN is lower than approximately its threshold (see electrical characteristics table). When in operation, the device automatically enters the shutdown mode if the voltage on VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

9.11 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

10 Application Information

10.1 Design Procedure

The TPS63050/1 series of buck-boost converters has internal loop compensation. Therefore, the external L-C filter has to be selected according to the internal compensation. Nevertheless, it's important to consider that the effective inductance, due to inductor tolerance and current derating can vary between 20% and -30%. The same for the capacitance of the output filter: the effective capacitance can vary between +20% and -50% of the specified datasheet value, due to capacitor tolerance and bias voltage. For this reason, Output Filter Selection shows the nominal capacitance and inductance value allowed.

Table 5. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	20	44	66	100
1.0	√	√	√	√	√
1.5	√	√(3)	√	√	√
2.2			√	√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check marks indicates recommended filter combinations

10.2 Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 6. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{5}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{6}$$

Where,

D =Duty Cycle in Boost mode
f = Converter switching frequency (typical 2.5MHz)
L = Selected inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated from Equation 6. The following inductors are recommended for use:

Inductor Selection (continued)

Table 6. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
1 µH	TOKO 1286AS-H-1R0M	2x1.6x1.2	2.1A/68mΩ
1.5µH	TOKO, 1286AS-H-1R5M	2x1.6x1.2	2.5A/ 95mΩ
1.5µH	TOKO, 1269AS-H-1R5M	2.5x2x1	2.1A/90mΩ
2.2µH	TOKO 1286AS-H-2R2M	2x1.6x1.2	2A/160mΩ

The inductor value also affects the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inversely proportional to the inductor value and the load current. This means the higher the value of inductance and load current, the more the right half plane zero moves to a lower frequency. This could degrade the phase margin of the feedback loop. It is recommended to choose the inductor's value in order to have the frequency of the right half plane zero >400kHz. The frequency of the RHPZ is calculated using Equation 7.

$$f_{RHPZ} = \frac{(1 - D)^2 \times Vout}{2\pi \times Iout \times L} \quad (7)$$

With,

D =Duty Cycle in Boost mode

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

If the operating conditions results in a frequency of the RHPZ of less than 400kHz, then more output capacitance should be added to reduce the cross over frequency.

10.3 Capacitor selection

10.3.1 *Input Capacitor*

At least a 10µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

10.3.2 *Output Capacitor*

For the output capacitor, use of a small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. The recommended typical output capacitor value is 10µF with a variance as outlined in Output Filter Selection.

There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

10.4 Setting the Output Voltage

When the adjustable output voltage version TPS63050 is used, the output voltage is set by the external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 800mV. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.1µA, and the voltage across the resistor between FB and GND, R_2, is typically 800 mV. Based on these two values, the recommended value for R2 should be lower than 200kΩ, in order to set the divider current at 3µA or higher. It is recommended to keep the value for this resistor in the range of 200kΩ. The value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 8:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (8)$$

10.1 Layout Considerations

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. See Figure 39 for reccomended layout.

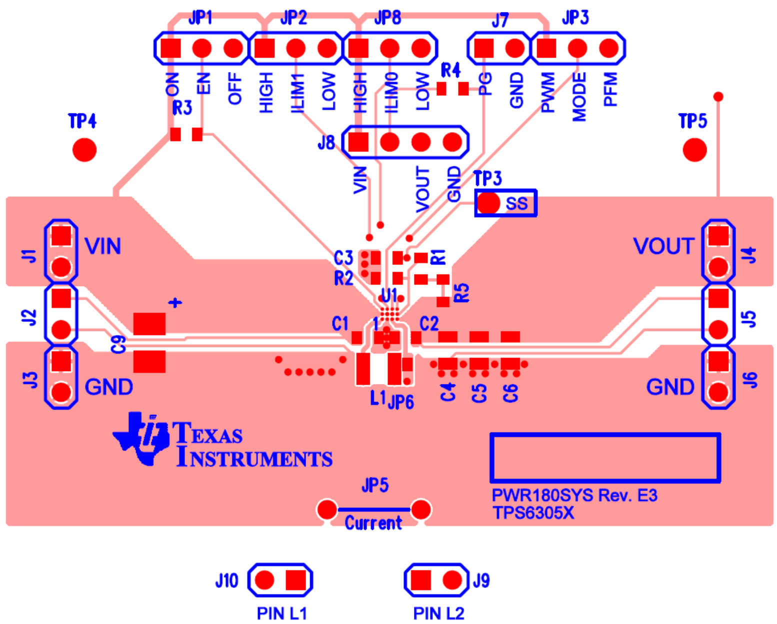


Figure 37. PCB Layout Suggestion

10.2 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and IC Package Thermal Metrics Application Note (SPRA953).

11 Device and Documentation Support

11.1 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.2 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63050YFFR	ACTIVE	DSBGA	YFF	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63050	Samples
TPS63050YFFT	ACTIVE	DSBGA	YFF	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63050	Samples
TPS63051YFFR	ACTIVE	DSBGA	YFF	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63051	Samples
TPS63051YFFT	ACTIVE	DSBGA	YFF	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63051	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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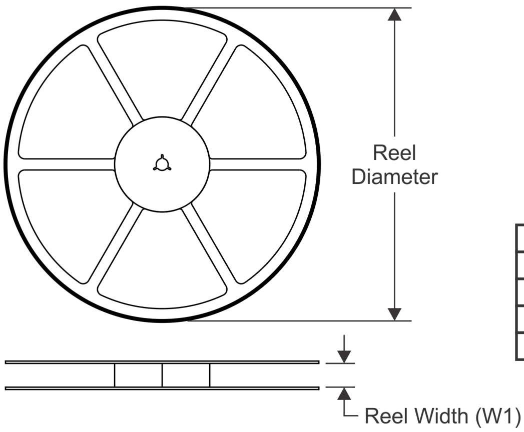
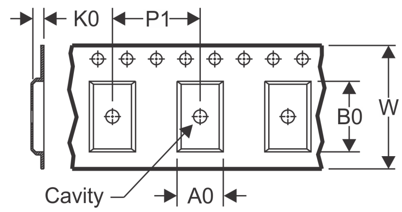
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

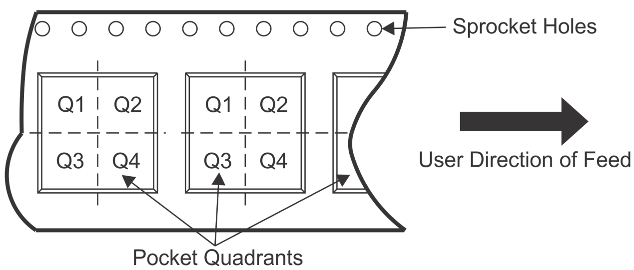


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

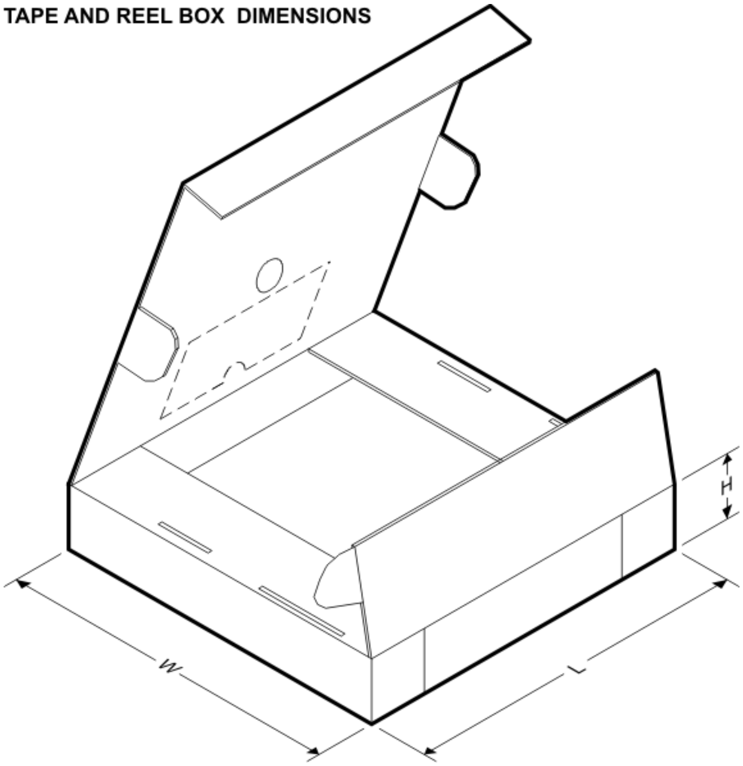
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63050YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1
TPS63050YFFT	DSBGA	YFF	12	250	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1
TPS63051YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1
TPS63051YFFT	DSBGA	YFF	12	250	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1

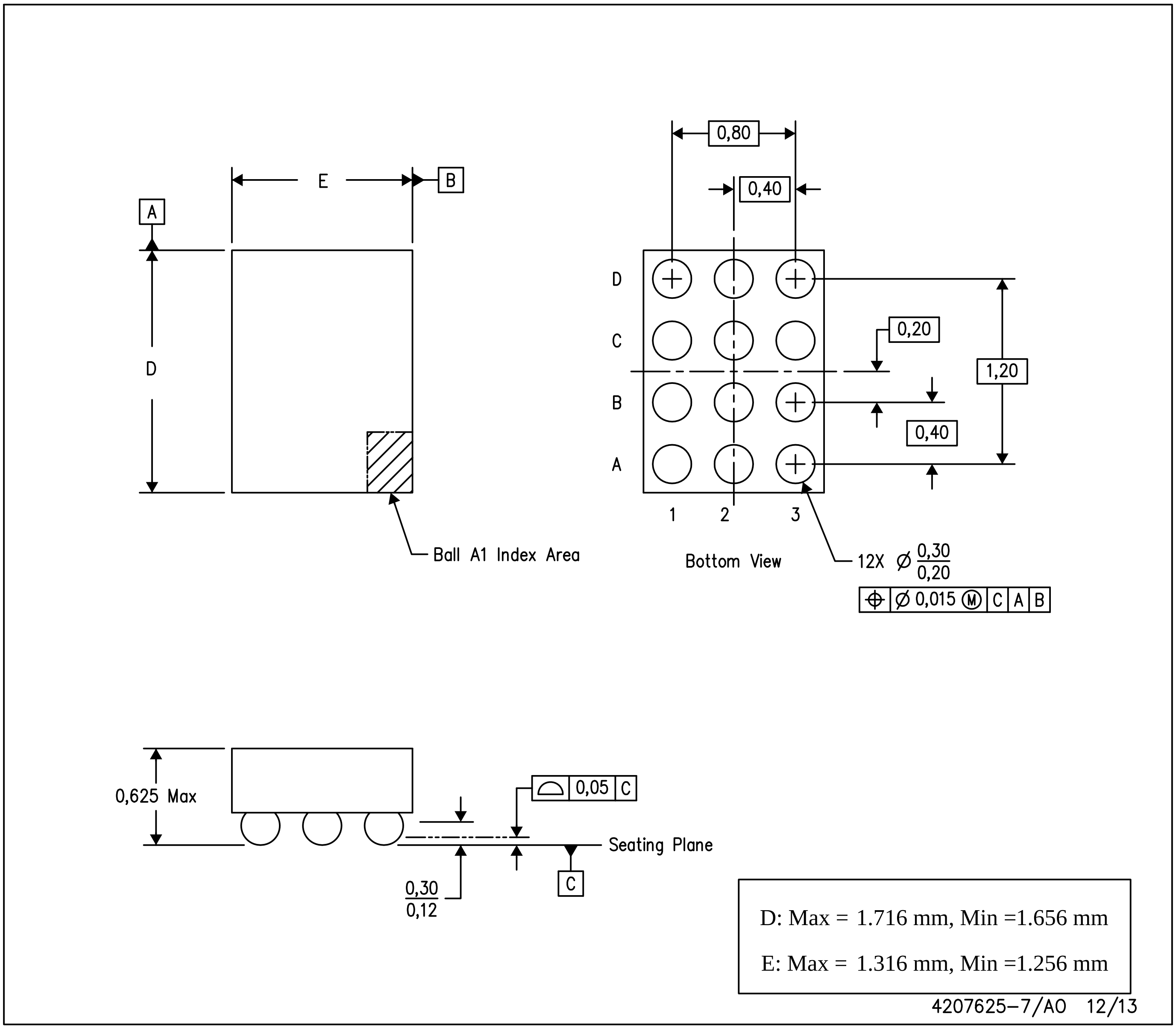
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63050YFFR	DSBGA	YFF	12	3000	182.0	182.0	17.0
TPS63050YFFT	DSBGA	YFF	12	250	182.0	182.0	17.0
TPS63051YFFR	DSBGA	YFF	12	3000	182.0	182.0	17.0
TPS63051YFFT	DSBGA	YFF	12	250	182.0	182.0	17.0

YFF (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

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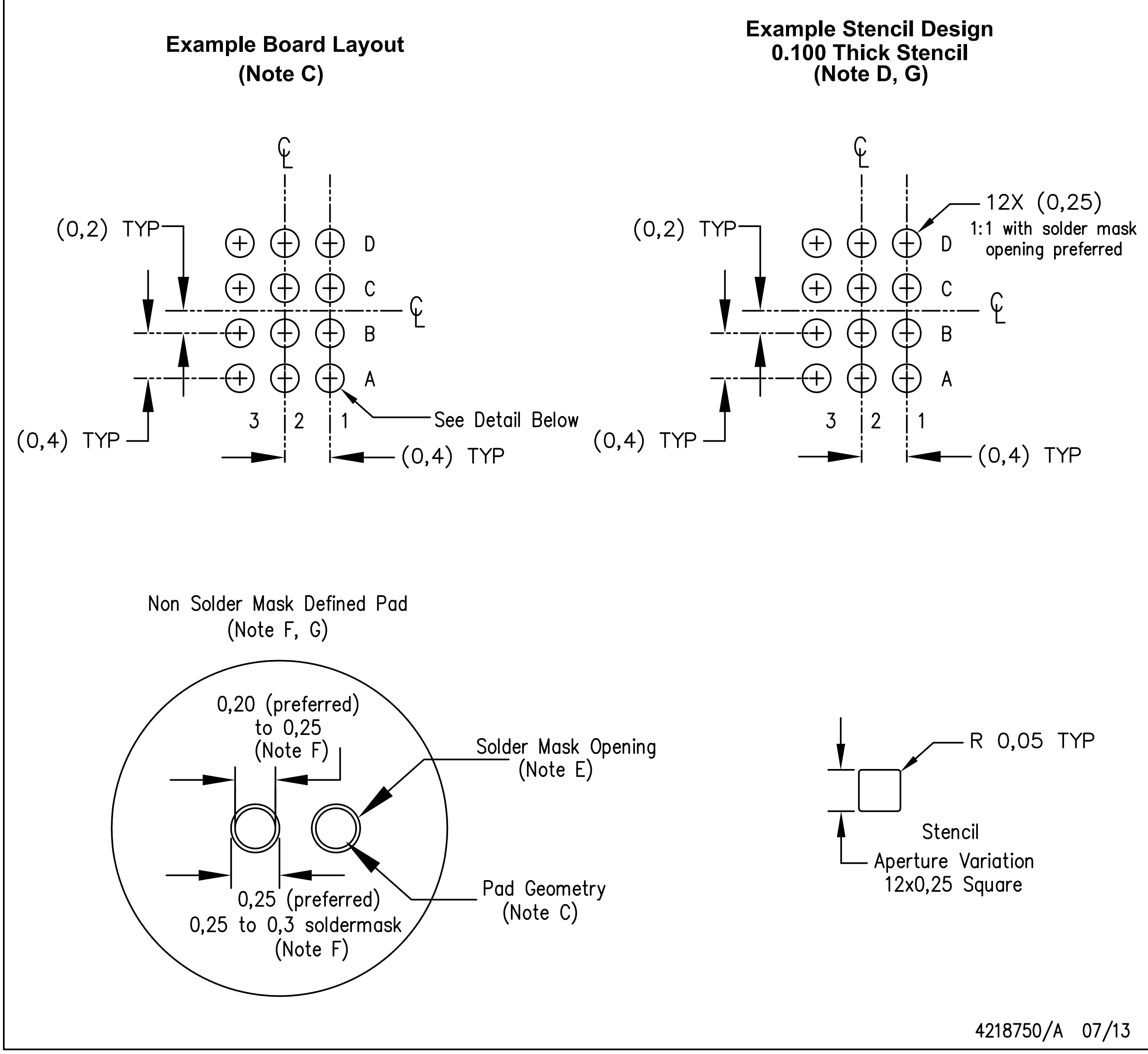
YFF (R-DSBGA-N12) **DIE-SIZE BALL GRID ARRAY**

(Pb—Free Solder Spheres)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC—7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Wafer Chip Scale Packages, Texas Instruments Literature No. SBVA017 and also the Product Data Sheet for specific thermal information, via requirements, and recommended routing guidelines. These documents are available at www.ti.com <http: //www.ti.com>.
- G. Placement force during assembly must be kept below 30g per solder sphere.

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