

March 2013

FQPF11P06

P-Channel QFET® MOSFET

-60 V, -8.6 A, 175 m Ω

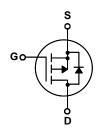
Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -8.6 A, -60 V, $R_{DS(on)}$ =175 $m\Omega(Max.)$ @ V_{GS} =-10 V, I_{D} =-4.3 A
- Low Gate Charge (Typ. 13 nC)
- Low Crss (Typ. 45 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings T_C = 25°C unless otherwise noted

3 °					
Symbol	Parameter		FQPF11P06	Unit	
V _{DSS}	Drain-Source Voltage		-60	V	
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		-8.6	Α	
			-6.08	Α	
I _{DM}	Drain Current - Pulsed	(Note 1)	-34.4	Α	
V _{GSS}	Gate-Source Voltage		± 25	V	
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	160	mJ	
I _{AR}	Avalanche Current	(Note 1)	-8.6	Α	
E _{AR}	Repetitive Avalanche Energy	(Note 1)	3.0	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-7.0	V/ns	
P_{D}	Power Dissipation (T _C = 25°C)		30	W	
	- Derate above 25°C		0.2	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C	
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C	
. L			300		

Thermal Characteristics

Symbol	Parameter	Тур	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		5.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		62.5	°C/W

Symbol	Parameter	Test Conditions		Min	Тур	Max	Unit
Off Cha	aracteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-60			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, Referenced	to 25°C		-0.07		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -60 V, V _{GS} = 0 V				-1	μΑ
		V _{DS} = -48 V, T _C = 150°C				-10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -25 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = 25 V, V _{DS} = 0 V				100	nA
On Cha	racteristics						
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$		-2.0		-4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -4.3 A			0.14	0.175	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = -30 \text{ V}, I_{D} = -4.3 \text{ A}$	(Note 4)		4.75		S
C _{iss}	Input Capacitance Output Capacitance	$V_{DS} = -25 \text{ V, } V_{GS} = 0 \text{ V,}$ f = 1.0 MHz			420 195	550 250	pF pF
C _{rss}	Reverse Transfer Capacitance				195 45	60	pF pF
100							
Switchi	ing Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30 V, I_{D} = -5.7 A, R_{G} = 25 Ω (Note 4, 5)			6.5	25	ns
t _r	Turn-On Rise Time				40	90	ns
t _{d(off)}	Turn-Off Delay Time				15	40	ns
t _f	Turn-Off Fall Time				45	100	ns
Qg	Total Gate Charge	V_{DS} = -48 V, I_{D} = -11.4 A, V_{GS} = -10 V (Note 4, 5)			13	17	nC
Q_{gs}	Gate-Source Charge				2.0		nC
Q_{gd}	Gate-Drain Charge				6.3		nC
Drain-S	Source Diode Characteristics ar	nd Maximum Ratings					
I _S	Maximum Continuous Drain-Source Dic	<u>_</u>				-8.6	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current					-34.4	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -8.6 A				-4.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = -11.4 A,			83		ns
	1	1	L				

- **Notes:**1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 2.5mH, I_{AS} = -8.6A, V_{DD} =-25V, R_{G} = 25 Ω , Starting T_{J} = 25°C 3. $I_{SD} \le$ -11.4A, di/dt \le 300A/µs, $V_{DD} \le$ BV $_{DSS}$, Starting T_{J} = 25°C 4. Pulse Test : Pulse width \le 300µs, Duty cycle \le 2% 5. Essentially independent of operating temperature

Typical Characteristics

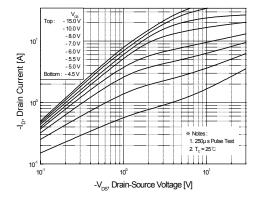


Figure 1. On-Region Characteristics

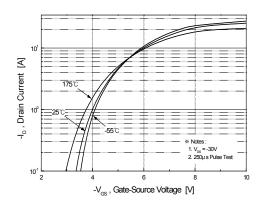


Figure 2. Transfer Characteristics

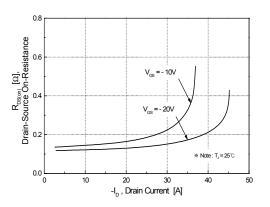


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

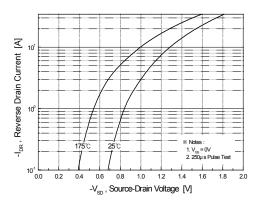


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

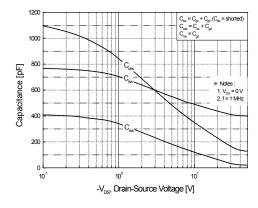


Figure 5. Capacitance Characteristics

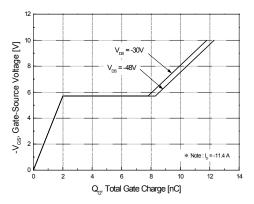
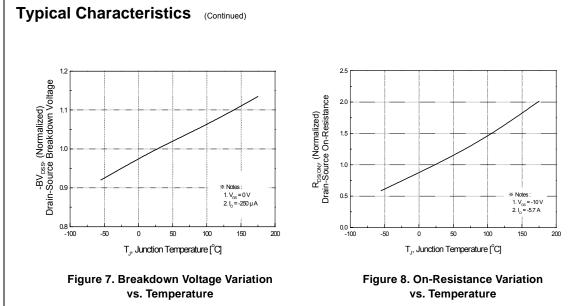


Figure 6. Gate Charge Characteristics



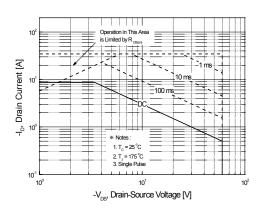


Figure 9. Maximum Safe Operating Area

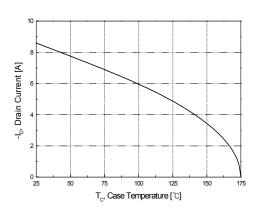


Figure 10. Maximum Drain Current vs. Case Temperature

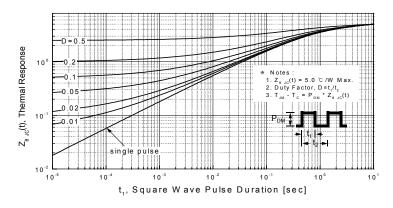
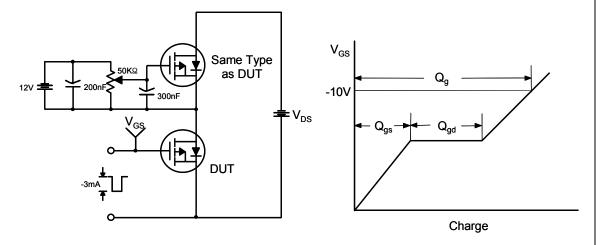
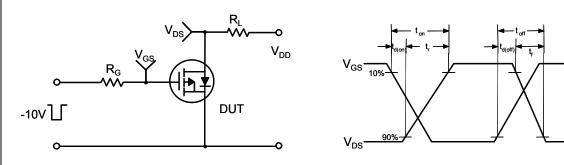


Figure 11. Transient Thermal Response Curve

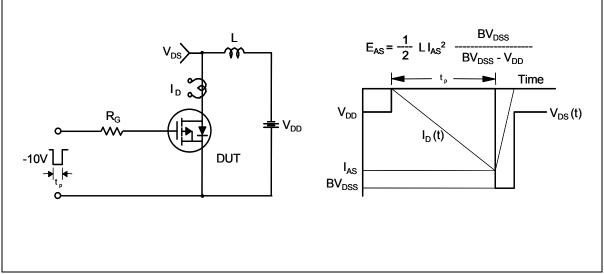
Gate Charge Test Circuit & Waveform



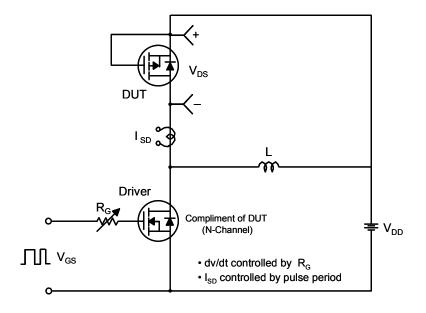
Resistive Switching Test Circuit & Waveforms

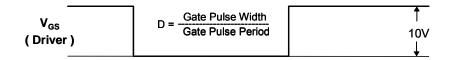


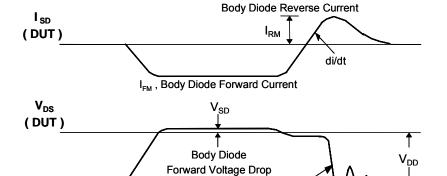
Unclamped Inductive Switching Test Circuit & Waveforms



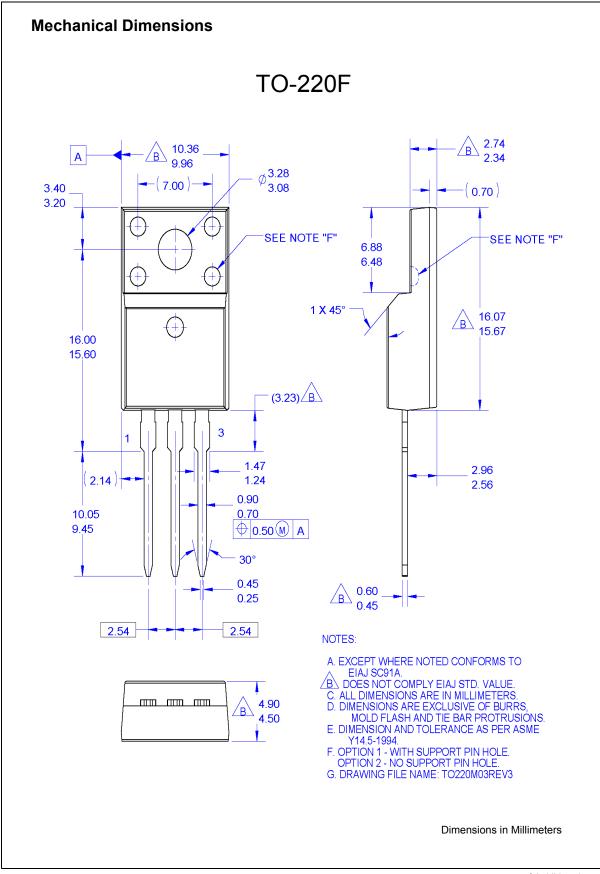
Peak Diode Recovery dv/dt Test Circuit & Waveforms







Body Diode Recovery dv/dt







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Contact Us:

> Address:

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd Minhang District, Shanghai , China

> Sales:

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

Customer Service :

Email service@ameya360.com

Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com