

March 2015

74VHC14 Hex Schmitt Inverter

Features

- High Speed: t_{PD} = 5.5 ns (Typ.) at V_{CC} = 5 V
- Low Power Dissipation: $I_{CC} = 2 \mu A$ (Max.) at $T_A = 25$ °C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- · Power down protection is provided on all inputs
- Low Noise: V_{OLP} = 0.8 V (Max.)
- Pin and Function Compatible with 74HC14

General Description

The VHC14 is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the VHC04 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitterfree output signals, thus providing greater noise margin than conventional inverters.

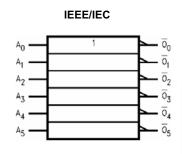
An input protection circuit ensures that 0 V to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

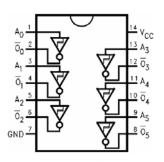
Ordering Information

Part Number	Top Mark	Package	Packing Method
74VHC14M	74VHC14	SOIC 14L	Rail
74VHC14MX	74VHC14	SOIC 14L	Tape and Reel
74VHC14SJX	VHC14	SOP 14L	Tape and Reel
74VHC14MTC	V14	TSSOP 14L	Rail
74VHC14MTCX	V14	TSSOP 14L	Tape and Reel

Logic Symbol/s

Connection Diagram/s





Pin Descriptions

Pin Names	Description
A _n	Inputs
\overline{O}_{n}	Outputs

Truth Table/s

Α	0
L	Н
н	L

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	±20	mA
I _{OUT}	DC Output Current	±25	mA
I _{CC}	DC V _{CC} / GND Current	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (Soldering 10 seconds)	260	°C

Note:

1. Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The data book specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Recommended Operating Conditions(2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	2.0	5.5	V
V _{IN}	Input Voltage	0	5.5	V
V _{OUT}	Output Voltage	0	V _{CC}	V
T _{OPR}	Operating Temperature Range	-40	85	°C

Note:

2. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

0		.,		T _A = 25°0	C	T _A = -40 to 85°C				1141
Symbol	Parameter	V _{CC}	Min.	Тур.	Max.	Min.	Max.	Unit	Conditions	
		3.0			2.20		2.20			
V_{P}	Positive Threshold	4.5			3.15		3.15	V		
	Voltage	5.5			3.85		3.85			
	7	3.0	0.90			0.90				
V_N	Negative	4.5	1.35			1.35		V		
	Threshold Voltage	5.5	1.65			1.65				
		3.0	0.30		1.20	0.30	1.20			
V_{H}	Hysteresis Voltage	4.5	0.40		1.40	0.40	1.40	V		
	,	5.5	0.50		1.60	0.50	1.60			
	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V		
		3.0	2.9	3.0		2.9			l., .,	I _{OH} = -50 μA
V_{OH}		4.5	4.4	4.5		4.4			$V_{IN} = V_{IL}$	I _{OH} = -4 mA
		3.0	2.58			2.48				
		4.5	3.94			3.80	2			$I_{OH} = -8 \text{ mA}$
		2.0		0.0	0.1		0.1			
		3.0		0.0	0.1		0.1		., .,	I _{OL} = 50 μA
V_{OL}	LOW Level Output	4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$	
	Voltage	3.0			0.36		0.44			$I_{OL} = 4 \text{ mA}$
ı		4.5			0.36		0.44			$I_{OL} = 8 \text{ mA}$
I _{IN}	Input Leakage Current	0 - 5.5			±0.1		±1.0	μА	V _{IN} = 5.5	V or GND
I _{CC}	Quiescent Supply Current	5.5			2.0		20.0	μА	V _{IN} = V _{CC}	or GND

Noise Characteristics(2)

Symbol	Parameter	V _{CC}	T _A = 25°C		Unit	Conditions	
	i arameter		Тур.	Max.			
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	0.4	0.8	V	C _L = 50 pF	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.4	0.8	V	C _L = 50 pF	
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C _L = 50 pF	
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C _L = 50 pF	

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V	T _A = 25°C			T _A = -40 to 85°C		Unit	Conditions
		v _{cc}	Min.	Тур.	Max.	Min.	Max.	Offic	Conditions
				8.3	12.8	1.0	15.0		C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay Time	3.3 ± 0.3		10.8	16.3	1.0	18.5	nc	C _L = 50 pF
		5.0 ± 0.5		5.5	8.6	1.0	10.0	ns	C _L = 15 pF
		5.0 ± 0.5		7.0	10.6	1.0	12.0		C _L = 50 pF
C _{IN}	Input Capacitance			4	10		10	pF	V _{CC} = Open
C _{PD}	Power Dissipation Capacitance			21				pF	(3)

Note:

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the opening current consumption without load.

Average operating current can be obtained by the equation: I_{CC} (Opr) = C_{PD} * V_{CC} * f_{IN} + I_{CC} /6 (per Gate)

Physical Dimensions

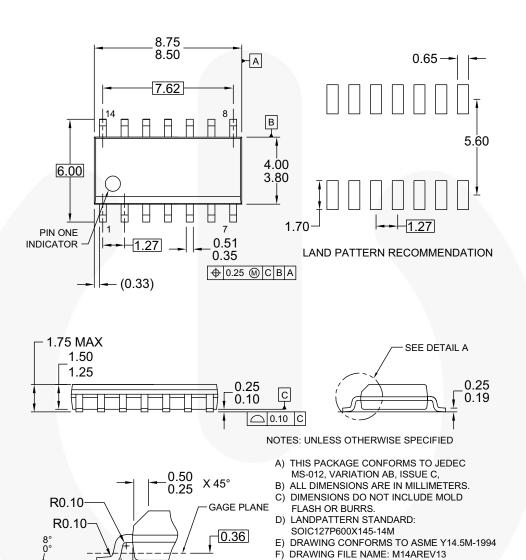


Figure 1. 14-LEAD, SOIC, JEDEC MS-012, 0.150 INCH, NARROW BODY

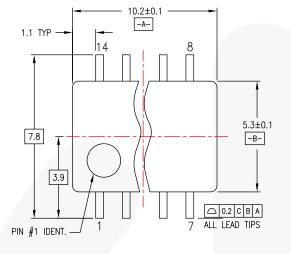
SEATING PLANE

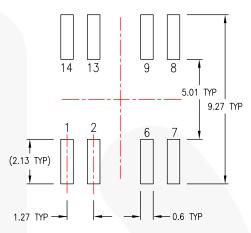
DETAIL A

0.90

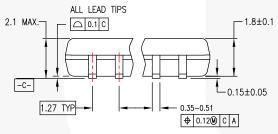
0.50 (1.04)

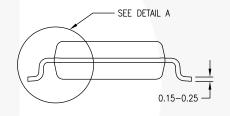
Physical Dimensions (Continued)





LAND PATTERN RECOMMENDATION

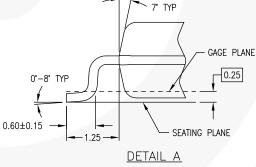




DIMENSIONS ARE IN MILLIMETERS

NOTES:

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



M14DREVC

Figure 2. 14-LEAD, SOP, EIAJ TYPE II, 5.0 MM WIDE

Physical Dimensions (Continued) 0.65 5.00±0.10 В 6.4 4.40±0.10 6.10 3.2 1.65 0.2 C B A ALL LEAD TIPS PIN#1 IDENT_/ TOP VIEW SEE DETAIL A -1.2 MAX 0.90^{+0.15} 0.10±0.05 0.30 0.19 ALL LEAD TIPS ○ 0.1 C ⊕ 0.13M A BS CS 0.65 12.00° TOP & BOTTOM FRONT VIEW 0.09 MIN NOTES: GAGE PLANE A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6 B. DIMENSIONS ARE IN MILLIMETERS. 0.25 0.09 M C. DIMENSIONS ARE EXCLUSIVE OF BURRS, -0.6±0.1 MOLD FLASH, AND TIE BAR EXTRUSIONS SEATING PLANE D. DIMENSIONING AND TOLERANCES PER ANSI DETAIL A Y14.5M, 2009. E. LANDPATTERN STANDARD: SOP65P640X110-14M. F. DRAWING FILE NAME: MKT-MTC14rev7.

Figure 3. 14-LEAD, TSSOP, JEDEC MO-153, 4.4 MM WIDE





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